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Hemant Bishnoi

Jason Whiles

Pius Ng

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/972

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Development and Validation of a Microcontroller Model for EMC

Shaohua Li[(1)], Hemant Bishnoi[(1)], Jason Whiles[(2)], Pius Ng[(3)], Haixiao Weng[(2)], David Pommerenke[(1)] and Daryl Beetner[(1)]

[(1)]EMC lab, Missouri University of Science & Technology, Rolla, Missouri,
Email: {slp4f, hbn74, davidjp, daryl}@mst.edu
[(2)]Texas Instruments, Houston, Texas, Email: {jwhiles, haixiao.weng}@ti.com
[(3)]Pius Ng, Apache Design Solutions, Plano, Texas, Email: piusng@apache-da.com

Abstract—**Models of integrated circuits (ICs) allow printed circuit board (PCB) developers to predict radiated and conducted emissions early in board development and allow IC manufactures insight into how to build their ICs better for electromagnetic compatibility (EMC). A model of the power delivery network, similar to the ICEM or LECCS model, was developed for a microcontroller running a typical program and used to predict the noise voltage between the power and return planes of a PCB. The IC and package model was generated using the Apache tool suite. A model of the PCB was created using an electromagnetic cavity model and lumped-element models of components on the board. Values of predicted and measured impedance looking into the IC and PCB matched within a few dB from a few 10s of MHz up to 1 GHz. Measured and predicted values of noise voltage matched within about 6 dB at clock harmonics up to 600-700 MHz.**

Keywords-integrated circuit design; modeling; power integrity; electromagnetic compatibility; decoupling; emissions.

I. Introduction

While ICs are not typically large enough to be efficient sources of radiated emissions by themselves below a few GHz, ICs are often the root source driving emissions is a PCB or system and are often the main cause or main victim of in-system interference. In recent years, designers have increasingly focused on reducing EMC problems at the IC level rather than relying entirely on board-level fixes. One method for better understanding the impact of ICs on EMC is through models of the power delivery network like the ICEM or LECCS specifications [1, 2]. Previous research has shown the promise of these models in several scenarios, including prediction of the conducted emissions from ICs [3,4], of clock jitter [3], of the influence of decoupling capacitors on conducted emissions [3-5], and of substrate noise in mixed-signal designs [6].

Models of the power delivery network are composed of two sub-models: a (typically passive) model of the power network impedance and a model of the switching activity of the IC, typically modeled as a current sink. Models of the IC may be obtained either through measurement or by using IC development tools that can extract resistive, capacitive and inductive values associated with the IC core and package, as well as the time-domain current consumed by the core [3-7]. Models of the PCB are typically found through measurement or are only predicted at low frequencies, though methods of predicting the high-frequency impedance characteristics of PCBs are available [8].

In this paper, models of the IC core, the package, and the printed circuit board are developed using modeling tools and are used to predict the noise voltage between the power and return planes. Unlike many models published in the literature, the model used here includes multiple switching current sources driving a distributed power delivery network through multiple power/return pins. The PCB is characterized using a cavity model [8], which allows the self and transfer impedance of the board to vary with location. The expectation is that this modeling approach will lead to better prediction of power integrity issues and better estimation of near-field emissions from the IC, for example to a TEM cell, since the PCB impedance and package currents are better defined.

The following text explains the development of the IC, PCB, and PCB-component (e.g. decoupling capacitor) models in detail. Passive models of impedance are verified through measurement and simulation of the impedance looking into the IC, PCB, and the PCB components and through simulation and measurement of the transfer impedance from one location on the PCB to another. The models of current sources in the IC are then used to predict noise voltage between the power and return planes of the PCB. The noise voltage simulations are then compared to measurements.

II. IC Model

A. Development

The model of the IC activity and impedance was generated using Apache's RedHawk/Sentinal-CPM tool

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suite. Apache's RedHawk/Sentinel-CPM can generate a compact SPICE compatible Chip Power Model (CPM) of a System-On-Chip (SOC). This model is composed of the current demand waveforms along with the resistance-capactiance-inductance network per pin or pin group. These data give a representation of the electrical behavior of the SOC, including the time-domain and frequency-domain information of the noise source.

RedHawk/Sentinel-CPM can simulate the dynamic current behavior of the entire, given the layout of a SOC along with the timing of its components and its analog and transistor-based blocks. The current demand of each component is modeled using SPICE to create the Apache Power Library (APL) which is responsive to the power supply variation of each component along with the input transition time and output loading condition. The intrinsic and output loading capacitance of each component, the intentional decoupling capacitance, and the parasitic capacitance of the power/ground network are taken into account. On-chip inductance can also be considered in the simulation, though was not included in this study. Apache's power/ground network extraction engine includes inter-power-domain coupling to simulate power noise propagation from one domain to another. Although a vector-based stimulus such as VCD is preferred, a realistic simulation can be achieved with behavioral specification such as full-chip/block/instance toggle rate and power consumption. Once the simulation is complete, the current signature waveforms can be captured at each pin or pin group.

In order to capture the effective resistance and capacitance per pin or pin group, RedHawk/Sentinel-CPM performs a frequency domain analysis and synthesizes the frequency response using SPICE passive elements with an error tolerance of less than 0.2 % compared to the original frequency response. Effectively, it reduces a network of millions of electrical nodes into a compact network of hundreds or thousands. Finally, RedHawk/Sentinel-CPM packages this synthesized network along with the current signature per pin or pin groups into a compact SPICE compatible CPM.

The final IC model generated by Redhawk/Sentinel-CPM included 9 power and return pin pairs, 17 noise current sources, and many elements to represent the internal power bus impedance. The current sources were generated for an IC running a typical test program.

The IC package model was generated using Apache's 3D quasi-static finite element modeling tool PakSi-E. The tool generates a S-parameter or SPICE model of the package including resistance, self inductance, and self-capacitance of the lead-frame and bonding wires over a return plane as well as the mutual inductance and capacitance between pins. While a model was developed for the entire package, only the elements associated with the 9 power/return pin pairs were used for the following simulations. Once developed, the package model was incorporate along with the model of the IC core and the two were treated together for the remainder of the analysis.

B. *Validation*

Models of the IC power delivery network and package were validated by measuring and simulating the impedance looking into individual power pin pairs. Impedance was measured using a network analyzer and a microprobing station as shown in Fig. 1. Two VSS and VSSIO pins were soldered together to reduce the connection impedance between the two power domains, as would occur on the PCB, and to allow easier bias of each domain. The reset pin was set low by connecting it to a Vss pin in order to minimize chip activity while the IC was biased and to minimize the corresponding influence of that activity on the impedance measurement. Since values of decoupling capacitance will vary with voltage and proper bias of P-N junctions is required for accurate measurements, VCC and VSS pins were biased with 1.5 V DC and VCCIO and VSSIO were biased with 3.3 V DC. The impedance looking into a power/return pin pair was found by placing the signal and return pins of the probe station across the pins and measuring S_{11} with the network analyzer.

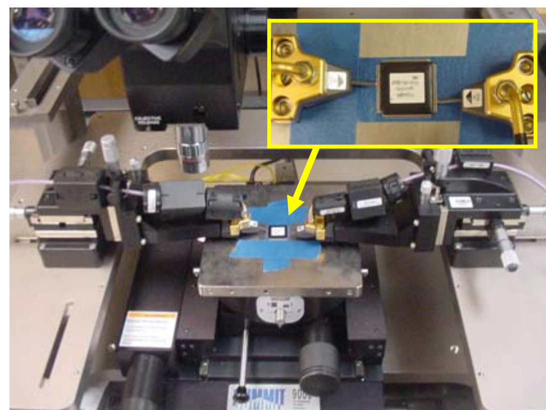

Figure 1. Measurement of the impedance of the IC.

Measured and simulated values of the impedance looking into one power/return pin pair are shown in Fig. 2. Simulated values were found using HSPICE. The chip is capacitive below 10 MHz, is primarily inductive above 10 MHz, and is resistive at the resonant point. The simulation and measurement match well beyond approximately 1 GHz. There is some discrepancy in measured and simulated values at a few 100 of kHz. This problem is likely due to parasitic currents in the biased IC that are (correctly) not included in the passive model. Increasing the signal power of the network analyzer reduces the difference between the measured and simulated curves at low frequencies, which supports this hypothesis. There is also some difference in the measured and simulated values of impedance around 10 MHz, though this difference is not expected to significantly influence prediction of the PCB noise voltage as the clock frequency of the IC is around 70 MHz. Measured

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and simulated values of IC capacitance and package inductance between 50 MHz and 1 GHz match well. Above 1 GHz, the package capacitance becomes important and causes a resonance at a few GHz. The discrepancies in the model resistance at 10 MHz and the resonance at a few GHz are apparently due to problems with the package model and differences between the model and the measurement setup. Improved package models are under development; however for this project we are only interested in noise below 1 GHz, so the high-frequency resonance at a few GHz is not important. Despite difference, we expect the model to work well below 1 GHz. The comparison of measured and simulated impedance at other pin pairs yielded similar results.

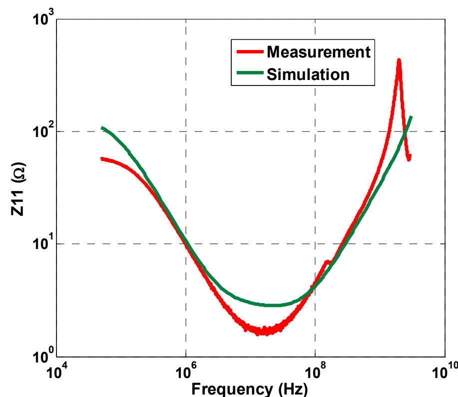

Figure 2. Measured and simulated values of impedance looking into the IC.

III. PCB MODEL

The PCB model includes a model of the power and return planes and of the "other" components attached to the planes, like the decoupling capacitors. The self- and transfer-impedance of the power and return planes was found using a cavity model to allow impedance to vary with location and to allow more accurate prediction at high frequencies. The IC, decoupling capacitors, and other components connected to the power planes were connected together in simulation through this power plane model.

A. Power Planes

A model of the power plane impedance was found using a program called EZPP (Easy Power Plane) developed at the University of Missouri – Rolla (now called the Missouri University of Science and Technology). The program uses a cavity model [7,8] to find the transfer parameters of a bare PCB. One can add decoupling capacitors at any location on the PCB and simulate to see their effect on Z and S parameters. The software also produces an equivalent SPICE model for the PCB impedance between specific port (i.e. connection) locations.

The test board is shown in Fig. 3. It is 3.88 inches on each side, 28 mils in thickness, and has a dielectric constant of 4.7. Simulated and measured values of the impedance looking into this board at port 1 are shown in Fig. 4. Impedance was measured using a network analyzer. The two curves match well below 1 GHz. The peak difference occurs between 600 MHz and 1 GHz and is less than 5 dB. This difference is primarily due to losses in the board that were not included in the model.

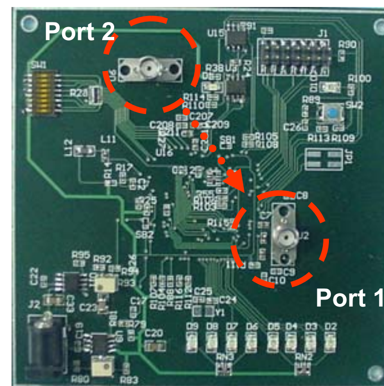

Figure 3. The test board.

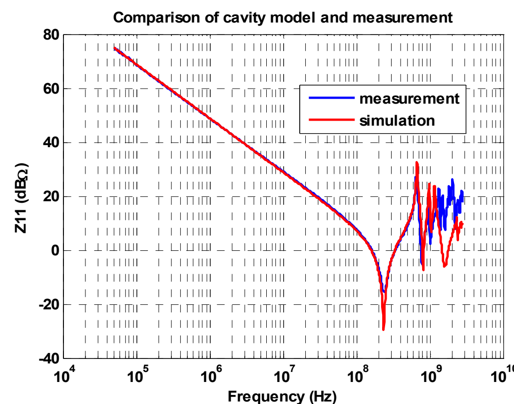

Figure 4. Comparison of cavity model impedance simulation and measurement for the bare PCB.

B. Decoupling Capacitors

On the test board, seven X7R ceramic decoupling capacitors, one 10 μF decoupling capacitor, and six 33 nF decoupling capacitors were directly connected to the power and return planes of the PCB. The decoupling capacitors were characterized using a series RLC model as shown in Fig. 5. Differences in the measured and simulated values of S parameters matched within less than a dB up to several GHz. Additional inductance was added to these capacitors in the PCB model to model the connection to the power and return planes.

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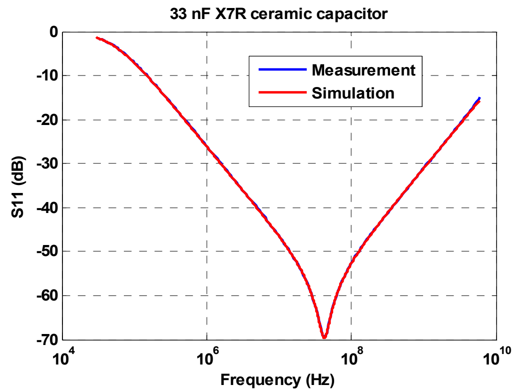

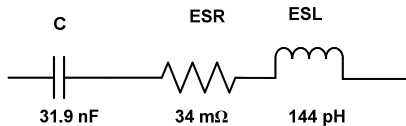

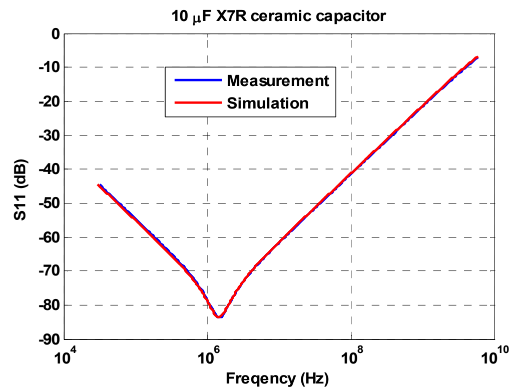

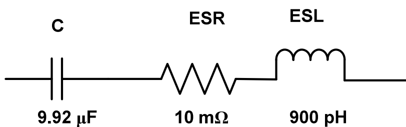

Figure 5. Decoupling capacitor models.

A. *Overall PCB Model Validation*

EZPP was used to produce a SPICE model of the PCB with 18 ports shown in Fig. 5. Nine of these ports were for the microcontroller's 9 pairs of VCC and VSS, 7 ports were for the 7 decoupling capacitors, and the remaining 2 ports were for SMA connectors as shown in Fig. 3. The models for the IC and for the decoupling capacitors were connected to these ports in the SPICE simulation.

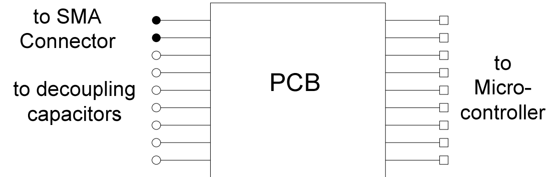

Figure 6. Block model of PCB power/return planes.

The model of the board with all connected components (including decoupling capacitors, voltage regulators, communications ICs, etc) was validated by simulating and measuring the impedance looking into the board at the port locations as well as the transfer impedance between port 1 and port 2 on the PCB (as shown in Fig. 3). Some discrepancy between the simulated and measured values occurred around 400 MHz, where there was a resonance between the approximately 540 pF of capacitance between the power and return planes and the approximately 400 pH of connection inductance to the decoupling capacitors. This difference of approximately 10 dB at the resonant point is most likely caused by parasitic inductance/capacitance/resistance in the components like the communications ICs that were not modeled, as the PCB model matches well when all other components but these are added to the board. Accounting for these components using a simple RLC model with an L around 2 nH, C between 10 pF and 80 pF, and R between 200 mΩ and 1000 mΩ resulted in the transfer impedance curve shown in Fig. 7.

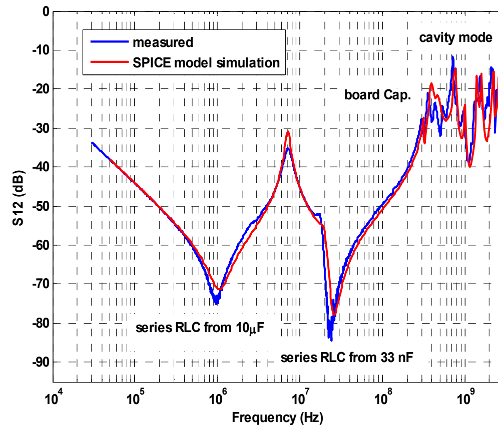

Figure 7. Measured and simulated values of S_{12} between SMA ports 1 and 2 on the PCB.

The first resonance in the transfer impedance at 1 MHz is mainly due to the 10 μF bulk decoupling capacitor. The second resonance at 7 MHz is due to the six 33 nF local decoupling capacitor resonating with the connection inductance to the bulk decoupling capacitor. The third resonance at 20 MHz is the local decoupling capacitors resonating with their connection inductance.

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Beyond 600 MHz the resonant modes of the boards begin to dominate. The final simulated transfer impedance matches the measurement within 6 dB or less up to about 2 GHz.

IV. Power Bus Noise

The noise voltage between the power and return planes was predicted once the passive IC, package, and PCB models were verified. The components were connected as indicated in Fig. 8. The active current sources were inserted into the IC and the resulting power bus voltage was found in the frequency domain using the transfer impedance between the current sources and the measurement location. Fig. 9 shows the measured and simulated noise voltage at port 2 on the PCB (see Fig. 3) as produced by the active IC. The simulation did a good job of predicting the noise voltage at harmonics of the clock up to 600-700 MHz, finding the correct value within 0 to 6 dB.

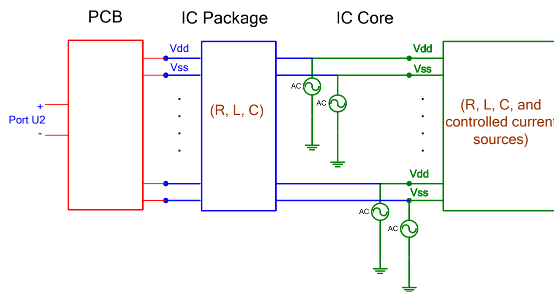

Figure 8. Block diagram of IC/package/PCB model.

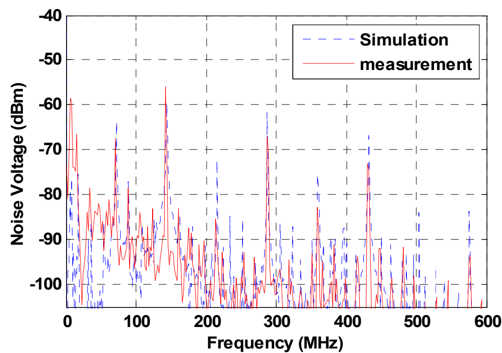

Figure 9. Simulated and measured power bus voltage noise spectrum.

V. Discussions and Conclusions

In this paper, models of the IC power delivery network and switching currents, IC package, and PCB power bus were developed and validated from measurement. Passive impedance models matched measurements well up to 1 GHz. The simulation model was able to produce good estimates of power bus noise voltage at harmonics of the clock to 600-700 MHz. The limitation in the maximum frequency may be associated with the tool used to predict the current sources, which was only designed to work to a few hundred MHz. A newer version of this tool is expected to work well beyond 1 GHz. Overall, this modeling approach appears to be promising for determining potential power integrity and associated emissions problems in the PCB early in the design.

A significant challenge with this work was the complexity of the IC and PCB model that were used. Other studies have typically used simple or measured models of the PCB. Instead of using only a single noise source delivering current to a single pair of power and return pins for the core, our model used 17 independent noise sources and 9 power and return pin pairs. The complexity of this model often made it difficult to determine the true cause of simulation errors. This same complexity, however, has the potential to yield improved prediction of noise at high frequencies and to deliver better estimates of near electric and magnetic field coupling from the ICs.

One challenge uncovered through this study was accounting for the characteristics of the many components attached to the PCB when estimating power bus noise. While the main contributors to PCB impedance are the power and return planes and the decoupling capacitors, other components may contribute significantly to the impedance as well, particularly at resonance. In this study, these components changed the transfer impedance at resonance by about 10 dB. While these changes can be well predicted if these other components are well characterized, such a characterization may not always be available.

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