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Common-Mode Current Due to a Trace Near a PCB Edge and Its Suppression by a Guard Band

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***Abstract*—The common-mode (CM) current due to a trace near a printed circuit board (PCB) edge, and its suppression by a guard band have been studied experimentally and with finite-difference time-domain (FDTD) modeling. As the guard band, copper tape is connected along the entire edge of the ground plane. First, a PCB electromagnetic interferenc (EMI) coupling path that results from the nonzero impedance of the PCB ground plane is discussed. As the trace is moved closer to the PCB edge, the CM current increases. Then, the effect of the guard band on the CM current is detailed. A guard band parallel to and near a trace is most effective in suppressing the CM current. The cross-sectional magnetic field distribution at center of the PCB with and without the guard band is also calculated with FDTD modeling. The guard band decreases the magnetic field distributed on the reverse side of a PCB. These results indicate the guard band is effective in suppressing CM current. Finally, an empirical formula to quantify the relationship between the position of a trace and CM current for the case with a guard band is proposed. Calculated results using the empirical formula and FDTD modeling are in good agreement, which indicates this empirical formula should be useful for developing EMI design guidelines.**

***Index Terms*—Common-mode (CM) current, electromagnetic interference (EMI), finite-difference time-domain (FDTD) method, guard band, printed circuit board (PCB).**

I. Introduction

COMMON-MODE (CM) radiation from cables attached to a printed circuit board (PCB), as well as CM radiation from the PCB itself, is a common electromagnetic interference (EMI) problem. It is necessary to suppress the CM current to reduce radiation. Previous studies on electromagnetic noise radiated from a PCB have been published [1]–[8]. The need to consider and model a CM current in order to predict adequately, the radiation from a PCB has been emphasized and demonstrated in [1], [2]. CM radiation from cables attached to PCBs will be largest near a resonance frequency of the effective "EMI antenna," one portion of which is the attached cable, such as an I/O line [3]. Mechanisms by which differential-mode (DM) signals are converted to CM noise sources resulting in EMI have been demonstrated, and two classes of coupling mechanisms are voltage driven and current driven [4]. But, in the considered frequency range, the current-driven mechanism is of particular importance for a trace near a PCB edge, and reviewed herein for this application.

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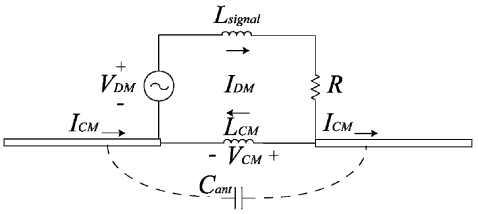

Fig. 1. Equivalent circuit illustrating the current driven mechanism.

An equivalent model for a PCB with a trace, which illustrates the physics of the current-driven mechanism, is shown in Fig. 1 [4]. The EMI coupling physics at lower frequencies is dominated by the magnetic field. For an infinite ground plane, there is no magnetic flux below the plane, and, hence, all the magnetic flux wraps the signal trace. Consequently, there is no inductance associated with the ground plane, and in this ideal case, the impedance of the ground plane is zero. However, for real PCB designs, in which the ground plane will have finite width, and has magnetic flux lines that close below the plane, the ground plane will have a nonzero impedance [2], [4]–[7]. The voltage drop $V_{\rm CM}$ across the nonzero impedance of the ground plane can result in CM radiation [8]. When the ohmic resistance of the ground plane is much smaller than the nonzero impedance, the CM current $I_{\rm CM}$ at frequencies below the radiator resonances is approximately

$$I_{\rm CM} \approx -\omega^2 C_{\rm ant} L_{\rm CM} \frac{V_{\rm DM}}{R} \tag{1}$$

where $V_{\rm DM}$ is the source voltage, $C_{\rm ant}$ is the capacitance between the two extensions of the lower conductors, R is the terminating resistor, and $L_{\rm CM}$ is the inductance between two portions of extended ground. $L_{\rm CM}$ is an inductance of signal return path and then, it is considered as a geometrical source which generates the CM current [4]. Changing the geometry of a PCB causes a change in the magnetic flux which wraps the ground plane, and hence, the CM radiation. The width of the ground plane, the width and height of the trace, and the position of the trace all affect the CM radiation.

The finite-difference time-domain (FDTD) method [9], [10] is well suited to modeling EMI resulting from PCB geometries to estimate EMI problems in high-speed electronic designs. It is helpful to be able to anticipate at the design stage the resonance of such PCB configurations where the EMI can peak. Also, by modeling the PCB geometry with EMI coupling paths, and

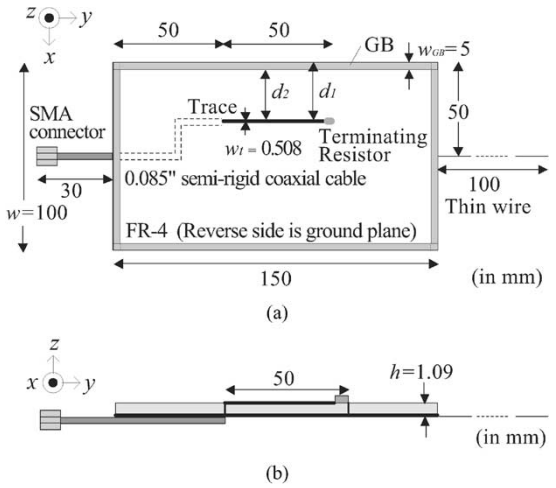

Fig. 2. Geometry of the PCB layout used in the experimentation. (a) Top view. (b) Side view.

knowing the CM current and the electromagnetic field distribution around the PCB, EMI design guidelines can be developed.

So far, EMI resulting from a trace near a PCB edge has been investigated theoretically, experimentally, and by numerical methods [11]–[14]. In the results, as the trace is moved closer to the PCB edge, the CM current increases, due to a higher CM inductance L_{CM} (Fig. 1). However, a full FDTD modeling of the PCB with an attached cable has not been implemented, which allows to study possible means for suppressing CM current.

In this paper, the CM current due to a trace near a PCB edge and its suppression by a guard band is investigated experimentally and with FDTD modeling. A guard-band copper tape, is connected along the entire edge of the ground plane. First, a PCB EMI coupling path that results from the nonzero impedance of the PCB ground plane is discussed to determine the necessary "keep-out" area on the PCB edge for high-speed trace routing. Second, the effect of the guard band on CM current is discussed. In order to understand the effect of the guard band, the magnetic field distribution is calculated with the FDTD method. Finally, an empirical formula to quantify the relationship between the position of a trace and CM current for the case with a guard band is proposed.

II. Experimental and Modeling Methods

A. PCB Geometry

The geometry of the PCB layout studied is illustrated in Fig. 2. The PCB had two layers, with the upper layer for a signal trace and the lower for the reference (ground) plane. A thin wire of 100-mm length with 0.6-mm diameter, used to mimic the extended electrical length of the board with an attached cable, was connected to the edge of a 100-mm × 150-mm ground plane. The trace, with 0.508-mm width and 50-mm length, was centered lengthwise on a 1.09-mm thick dielectric substrate with $\varepsilon_r = 4.5$. Several different configurations in which the distance d_1 between the trace and the PCB edge, as shown in Table I, were prepared for the measurements. Although the characteristic impedance of the trace was calculated as approximately 92 Ω[15], the impedance of the "center" case and the

TABLE I
PCBs Under Test

	d_1 [mm]	$d_1/\left(\frac{w}{2}\right)$	guard band width [mm]	Terminating resistor [Ω]
d50	1.27 (50 mil)	0.025	without GB	100
d100	2.54 (100 mil)	0.051	without GB	100
d250	6.35 (250 mil)	0.127	without GB	100
d250GB			w_{GB}=5	
d300	7.62 (300 mil)	0.152	without GB	91
d400	10.16 (400 mil)	0.203	without GB	91
d400GB			w_{GB}=5	
d600	15.24 (600 mil)	0.305	without GB	91
d600GB			w_{GB}=5	
center	49.75	0.995	without GB	91
centerGB			w_{GB}=5	

(d_1: distance between the trace and the PCB edge, h: thickness of the dielectric substrate, and w_{GB}: width of the guard band)

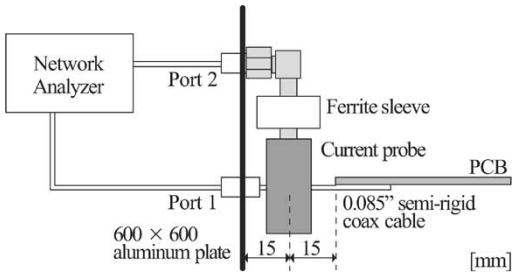

Fig. 3. Experiment setup for CM current measurements.

case when the trace was near a PCB edge $(d_1 \leq 6.35\ \mathrm{mm})$ was approximately 90 and 98 Ω as measured with a time-domain reflectometry (TDR), respectively. In order to match the impedance, the trace was terminated with either 91- or 100-Ω surface-mount technology (SMT) resistor, as shown in Table I.

The same configuration of PCBs with a guard band were also prepared, except the cases of "d50," "d100," and "d300". As the guard-band copper tape was used and connected along the entire edge of the ground plane to the upper layer through the side of the PCB. The width w_{GB} of the guard band was 5 mm. TDR measurements were worked to compare the characteristic impedance for the cases with and without a guard band, and the results were nearly the same.

The PCB was driven by a 0.085-in semi-rigid coaxial cable running along the center of the PCB on the reverse side. The cable ran the length of the PCB to the feed point of the driven trace, and was soldered to the ground plane along its entire length. The center conductor of the semi-rigid coaxial cable was extended beyond the outer shield and penetrated the PCB through the ground plane to connect to the trace on the top side. The coaxial cable extended 30 mm beyond the PCB edge, and a shape memory alloy connector was located at the end of the cable.

B. Experimental Method

The CM current on the outer shield of the feed cable was measured using a current probe (Fischer F-2000), and a network analyzer (HP 8753D), as shown in Fig. 3 [11], [16]. A 600-mm × 600-mm aluminum plate was used to isolate the PCB from the cable dressing leading to the network analyzer. The current probe is mounted adjacent to the aluminum plate and encircled the feeding cable, as shown in Fig. 3. A ferrite sleeve

(100 Ω at 100 MHz) is mounted around the probe connector to reduce coupling to the current probe. The $|S_{21}|$ with the location of Port 1 (the voltage source for the signal trace) and Port 2 (current probe on the semi-rigid cable) was measured in the frequency range from 50 MHz to 1 GHz. Port 1 was connected to the 0.085-in coaxial cable to drive the signal line, and Port 2 was connected to the current probe.

The calibration of the network analyzer and removal of the frequency response of the current probe were done by using a shorted copper ring [11], [16]. A copper ring was wrapped tightly around the current probe and connected to Port 1 during calibration. The current I_{Port1} in the copper ring, at frequencies where the source impedance is significantly greater than the calibration ring loop inductance, is given by $I_{\mathrm{Port1}} \approx V_S/50$, where V_S is the RF source voltage of the network analyzer, and the source impedance of the network analyzer is 50 Ω. The voltage V_2^- at Port 2 is given by $V_2^- = 50 I_{\mathrm{Port2}}$, where I_{Port2} is the current sensed by the current probe. The currents at Port 1 and Port 2 are related by the transfer function of the current probe $H_T(f)$, therefore $I_{\mathrm{Port2}} = H_T(f) I_{\mathrm{Port1}}$. Since the 50-Ω source impedance is matched to the characteristic impedance of the cable, the voltage at Port 1 is given by $|V_1^+| = V_S/2$. Therefore, $|S_{21}|$ is given by

$$|S_{21}| = \left|\frac{V_2^-}{V_1^+}\right| = \left|\frac{50 H_T(f) \cdot \frac{V_S}{50}}{\frac{V_S}{2}}\right| = |2H_T(f)|. \qquad (2)$$

On the other hand, when a PCB is connected to Port 1, I_{CM} on a semi-rigid coaxial cable is sensed by the current probe, therefore $I_{\mathrm{Port2}} = H_T(f) I_{\mathrm{CM}}$. $|S_{21}|$ before the calibration is given by

$$|S_{21}| = \left|\frac{50 H_T(f) \cdot I_{\mathrm{CM}}}{\frac{V_S}{2}}\right|. \qquad (3)$$

The calibration procedure removes the factor $2H_T(f)$ from (3). Consequently, the relationship between $|S_{21}|$ and the CM current I_{CM} is given by

$$|S_{21}| = \left|\frac{50 I_{\mathrm{CM}}}{V_S}\right|. \qquad (4)$$

Equation (4) is used to compare experimental and numerical results.

C. FDTD Modeling

The FDTD method [9], [10] was used for simulating the CM current on the PCB. The FDTD modeling details were determined by varying the number of cells for trace width, substrate thickness, and the distance between PCB and perfectly matched layers (PMLs) [17]. Eight PML layers were used for the absorbing boundary. The measured and simulated results were in good agreement when the meshing of the trace and the substrate was greater than two cells, and the distance between the PCB and the PML layers was greater than $\lambda/120$, where λ was the maximum wavelength of the lowest frequency. Therefore, the cell size was $\Delta x = 0.254$, $\Delta y = 2.5$ and $\Delta z = 0.546$ mm. The total computational domain was $491 \times 154 \times 183$ cells, in the x, y, and z dimensions, respectively. The time step was $\Delta t = 6.35 \times 10^{-13}$ s from the Courant stability condition [10].

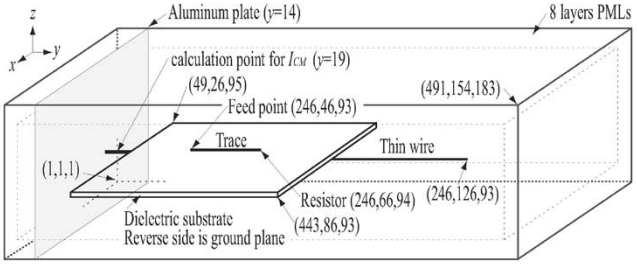

Fig. 4. Computational domain for the FDTD simulation, with a centered trace.

Fig. 4 shows the computational domain for the FDTD simulation in the case where the trace is centered, as a typical example. The trace was modeled as a perfect electric conductor (PEC), two-cell wide. The ground plane, thin wire, and aluminum plate were also modeled as an PEC. The aluminum plate used in the experiments was included as an infinite ground plane. An SMT resistor was modeled as a one-cell lumped element in the PCB substrate. The PCB substrate was modeled as a dielectric, two-cell deep, with relative permittivity $\varepsilon_r = 4.5$. A sinusoidally modulated Gaussian pulse was used as the source with source resistance 50 Ω. The CM current was calculated by the loop integral of the magnetic field around the cable at the current probe position.

To shorten the calculation time, the vector and parallel computation method for a super computer NEC SX-4 (Tohoku University Information Synergy Center) was used in FORTRAN 90, where IF-THEN operations in a vector loop were eliminated [18]. The memory required to calculate the model of Fig. 4 was 1.2 GB, and it takes longer than 150 min for the vector and parallel computation with 8 CPUs (16 GFlops) on the super computer that has a maximum performance of 256 GFlops.

III. CM Current Due to Trace Near Edge of PCB Without Guard Band

The PCB EMI coupling path source that results from the nonzero impedance of the PCB ground plane is discussed in this section. The $|S_{21}|$ related to CM current shown in Fig. 5(a) and (b) are for the cases with and without a thin wire, respectively. In both cases, as the trace is moved closer to the PCB edge, $|S_{21}|$ increases. Further, the curve is shifted nearly uniformly in magnitude over the considered frequency range. The difference between the case of "center" and "d600" is approximately 3 dB, and that between "center" and "d50" is approximately 12 dB. At lower frequencies, the CM current follows a slope of 12 dB/Octave [4]. This is consistent with an EMI coupling path dominated by the magnetic field [7]. The calculated and measured results are in good agreement in both cases. Comparing the case with and without a thin wire, the difference is only at the second resonance frequency which is due to an antenna type resonance. It is suggested that the second resonance is related to the total length of PCB. The case without a thin wire is discussed below.

In FDTD simulation, the case used a conductor with the resistivity of copper, instead of PEC, as the ground plane was also calculated. The result is the same as the case of PEC. This indicates that the partial inductance L'_{CM} of the ground plane dominates the increase of I_{CM}. A formula for the per-unit-length

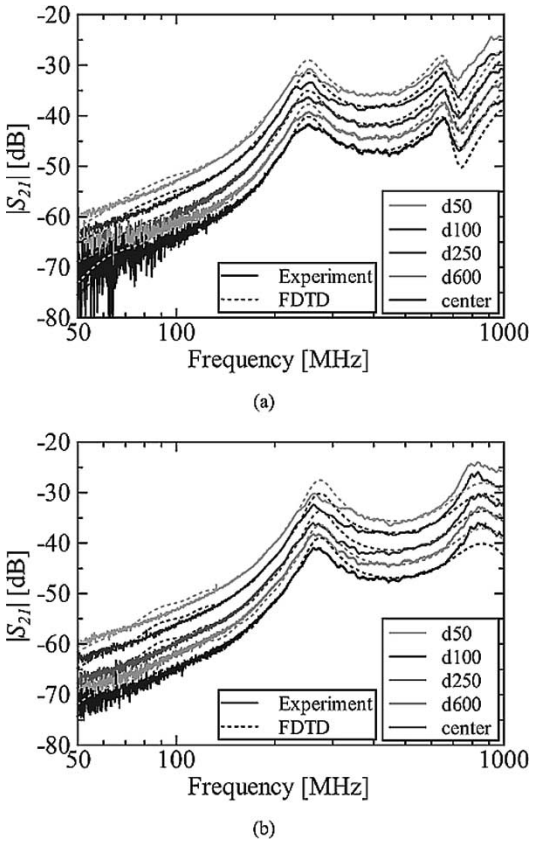

Fig. 5. Comparison of measured and simulated $|S_{21}|$ frequency responses for the PCBs under test (see Table I). (a) PCB with a thin wire. (b) PCB without the thin wire.

CM inductance $L'_{\rm CM}$ in nanohenry per centimeter of the PCB ground plane, has been derived analytically, as

$$L'_{\rm CM} = 4\frac{h}{w}\frac{1}{\sqrt{1-4\left(1-2\frac{h}{w}\right)\left(\frac{s}{w}\right)^2}} \tag{5}$$

where w is the width of the PCB, h is thickness of the dielectric substrate, s is the distance between the center of the PCB and the center of the trace ($s = w/2 - w_t/2 - d_1$), w_t is the width of trace, and d_1 is distance between the trace and the PCB edge [14]. This is the case without a guard band in the present study. Using (1) and (5), $|S_{21}|_{\rm norm}$ in decibels, which is the normalized value to the "$h = h_{\rm ref}$, centered trace ($s = 0$) and without GB" (center) case, is given by

$$\begin{aligned}|S_{21}|_{\rm norm} &= |S_{21}|_s^h - |S_{21}|_{s=0}^{h=h_{\rm ref}} \\ &= 20\log_{10}\left(\frac{\frac{h}{h_{\rm ref}}\frac{R_{\rm ref}}{R}}{\sqrt{1-4(1-2\frac{h}{w})(\frac{s}{w})^2}}\right)\end{aligned} \tag{6}$$

where $h_{\rm ref}$ is the reference thickness, i.e., 1.09 mm in this study, R is terminating resistance, and $R_{\rm ref}$ that of the "center" case with $h_{\rm ref}$. Results of the measured, FDTD calculated, and (6) of $|S_{21}|_{\rm norm}$ are shown in Fig. 6. The $|S_{21}|_{\rm norm}$ for the measured and FDTD calculated results is approximately constant over the considered frequency range, and is almost the same as that calculated with (6). Therefore, $|S_{21}|_{\rm norm}$, the average of $|S_{21}|$ in the considered frequency range, is used.

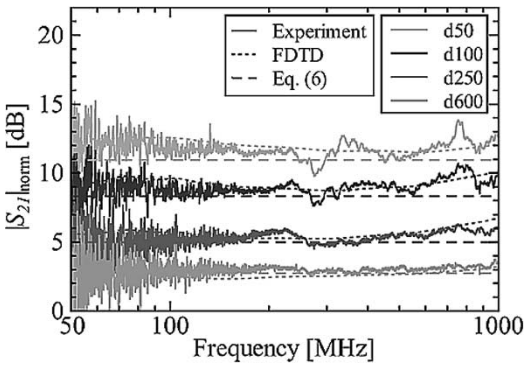

Fig. 6. $|S_{21}|_{\rm norm}$ versus frequency.

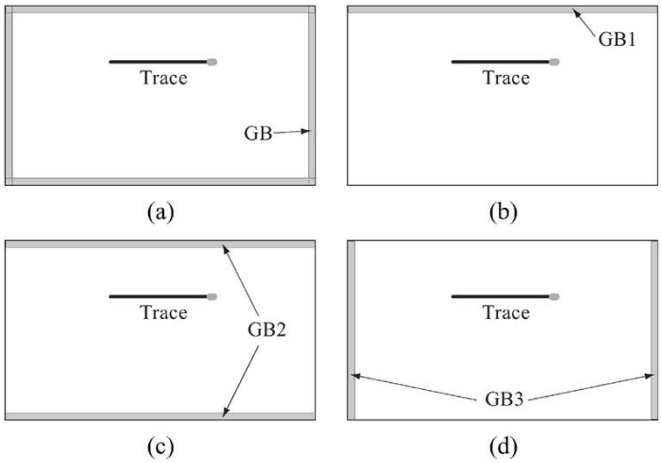

Fig. 7. Position of the guard band on the PCB (top view of the PCB). (a) GB. (b) GB1. (c) GB2. (d) GB3.

A common maxim for PCB design is to keep high-speed traces on the interior of the PCB whenever possible, and a distance between high-speed traces and the PCB edge is often specified in terms of the width of the PCB. This distance d_1 can be estimated by (6). As an example, when the difference $|S_{21}|_{\rm norm}$ to the "center" case is required to be smaller than 3 dB, the $d_1/(w/2)$ ratio must be no less than 0.28. One problem with a rule like this is that as the PCB design density continues to increase, designers can no longer afford the space on the PCB to follow this guideline, and traces are placed closer to the PCB edge.

IV. Effect of Guard Band on CM Current Suppression

The effect of a guard band on the CM current in the case of a PCB without an attached thin wire was investigated experimentally and with FDTD modeling. Specifically, the focus was on the CM current when routing traces near the edge of the PCB with a guard band. The relationship between the position of the signal trace and CM current is quantified.

A. Effect of Position of Guard Band

Using PCBs shown in Fig. 2 and Table I, the effect of the guard band (GB) is compared with the case without the guard band by measurement and FDTD modeling. In order to study the effect of the guard band position, four configurations with GB, GB1, GB2, and GB3, as shown in Fig. 7, were modeled

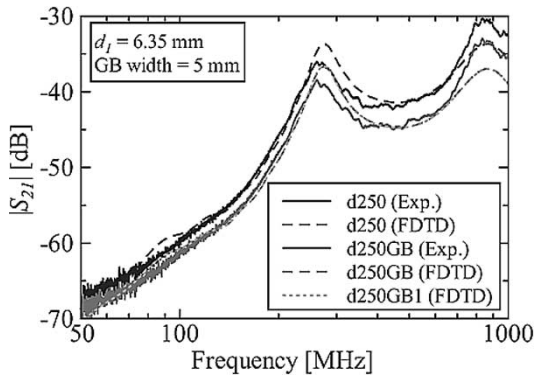

Fig. 8. Example of $|S_{21}|$ in the case with and without the guard band with 5-mm width ($d_1 = 6.35$ mm).

with the FDTD method, where the width w_{GB} of guard band was 5 mm. For the case GB, the guard band was around the entire board periphery, GB1 was parallel to and near a trace, GB2 was parallel to a trace, and GB3 was at a right angle to a trace. As an example, the measured and calculated results for the "$d_1 = 6.35$ mm (d250)" case are shown in Fig. 8. The calculated and measured results are in good agreement. The $|S_{21}|$ in the cases with the GB1 and GB2 is almost the same as the case with GB which is connected along the entire edge, and these curves overlay. On the other hand, the GB3 has no effect in suppressing $|S_{21}|$. Consequently, the results of the cases with GB2 and GB3 are omitted in Fig. 8. These results indicate that the guard band parallel to and near a trace is most effective in suppressing the CM current.

B. Magnetic Field Distribution

In order to understand the details of the guard band suppressing the CM current, the magnetic field distributions for the x-z plane at the center of the PCB in the case of "center," "d250," and "d250GB" were calculated by using the FDTD method. A 1-V 865-MHz sinusoidal signal, which is the second resonance frequency of the test configuration was applied. After the signal reached the steady state, the root-mean-square value of the magnetic field strength was calculated from the waveform over one cycle. The calculation results for the magnetic field $|\boldsymbol{H}|$ distribution for the x-z plane at the center of PCB are shown in Fig. 9. To compare the effect of the guard band quantitatively, the magnetic field H_x distribution in the x direction is calculated, as shown in Fig. 10. In the "center" and "d250" case, the tendency of the H_x distribution is almost the same as that measured by a magnetic shielded-loop antenna in [19]. If the magnetic flux which encloses a ground plane (related to H_x) increases, the impedance of the ground plane will increase, with the result that CM current increases [4].

For the "center" case, the magnetic field on the under side of the PCB is relatively small. When a trace is placed near a PCB edge (d250), the magnetic field under the PCB increases dramatically. On the other hand, the magnetic field distributed on the under side of the PCB with the guard band (d250GB) is smaller, as compared with the magnetic field in the "d250" case. This demonstrates the guard band suppresses the magnetic flux which encloses a ground plane. So, the guard band can be effective in suppressing the CM current resulting from a high-speed trace as a trace with high-frequency noise on it nears a PCB edge.

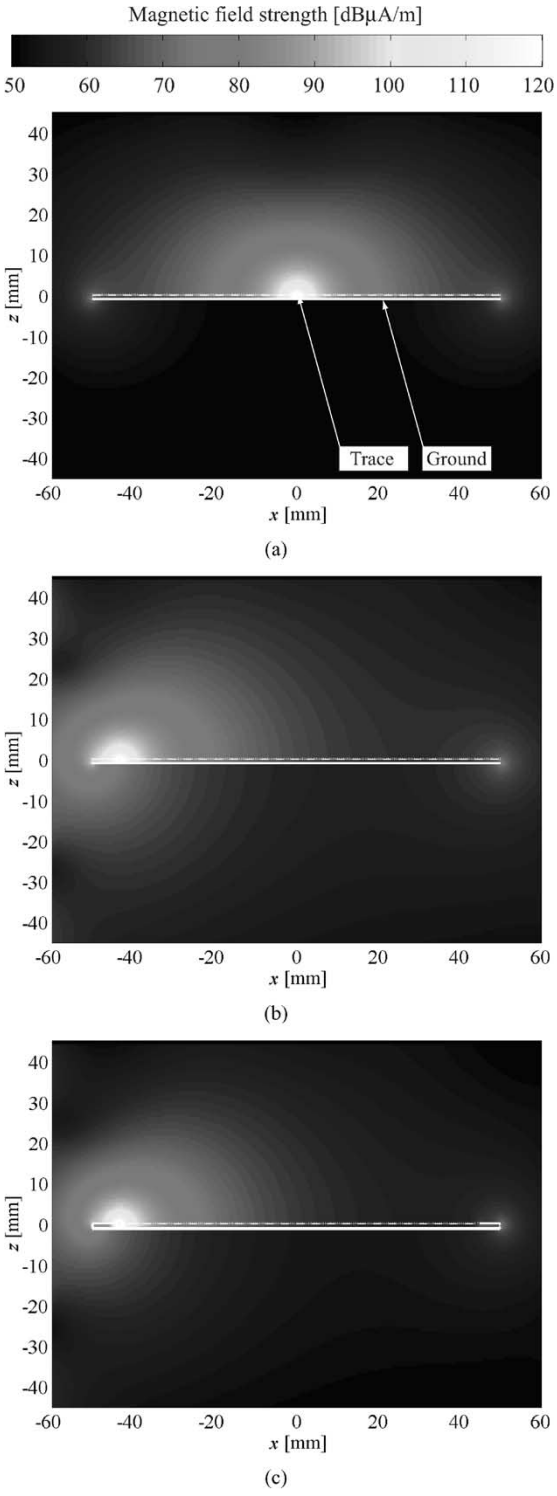

Fig. 9. Magnetic field $\boldsymbol{H}$ distribution in the x-z plane at the center of the PCB. (a) center. (b) d250. (c) d250 GB.

C. Quantifying the CM Current and Its Suppression by a Guard Band

Empirical expressions to quantify the relationship between the position of the trace and CM current for the case with a guard band can be developed from the FDTD simulation results. The

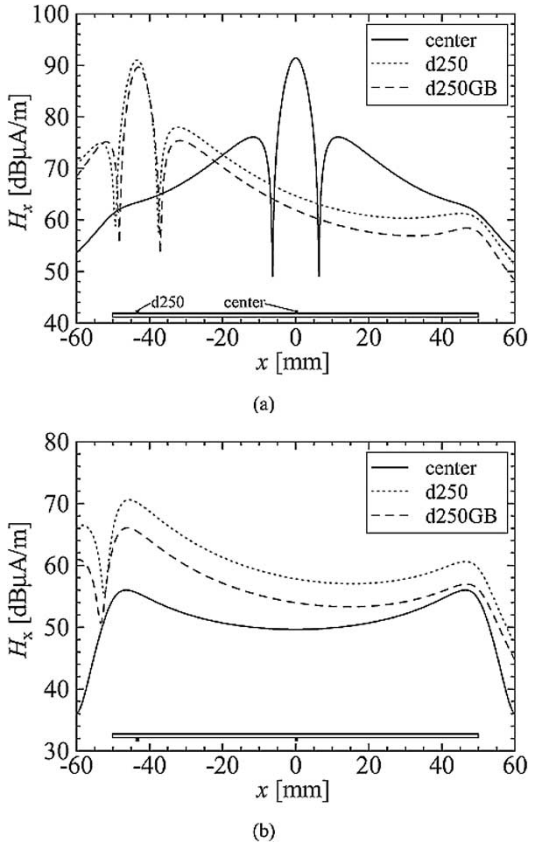

Fig. 10. H_x distribution along the x direction. (a) Magnetic field H_x distribution calculated at 6 mm above the PCB. (b) Magnetic field H_x distribution calculated at 6 mm under the ground plane.

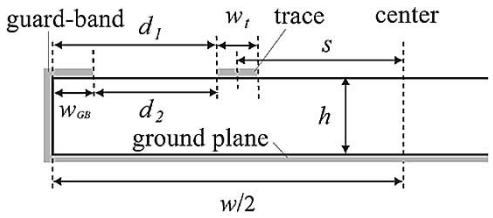

Fig. 11. Cross-section of the PCB showing the relevant dimensions.

cross-sectional dimensions of a part of the PCB with the guard band, related to the formulation, is shown in Fig. 11. To investigate the effect of the guard band with the position of the signal trace, the width of the GB1 was varied with $w_{\rm GB} = 0$, 2.5 and 5.0 mm. In Fig. 11, $w_{\rm GB} = 0$ mm means that there is a vertical metallic part of guard band on the PCB edge, but with no horizontal metallic part on the top of the PCB. In addition, the thickness of the dielectric substrate was varied with $h = 1.09$, 1.64 and 2.18 mm, as shown in Table II. The $|S_{21}|$ was calculated from the FDTD modeling. The signal trace was terminated in a matched load Z_0.

The guard band effect GBE in decibels, which is the difference between the $|S_{21}|$ with GB1 ($|S_{21}|_{\rm GB}$) and the $|S_{21}|$ without the guard band ($|S_{21}|$), is defined herein as

$$\mathrm{GBE} \equiv |S_{21}| - |S_{21}|_{\rm GB}. \tag{7}$$

TABLE II
PARAMETERS OF PCB IN FDTD MODELING

h [mm]	1.09	1.64	2.18
Z_0 [Ω]	91, 100	112	123
d_1 [mm]	$0 \sim 49.75$		
guard band	without GB		
	w_{GB} =0, 2.5, 5.0 mm		

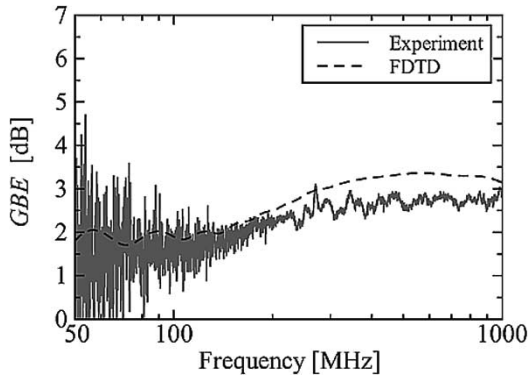

Fig. 12. GBE versus frequency (ex. $d_1 = 6.35$ mm, $w_{\rm GB} = 5$ mm).

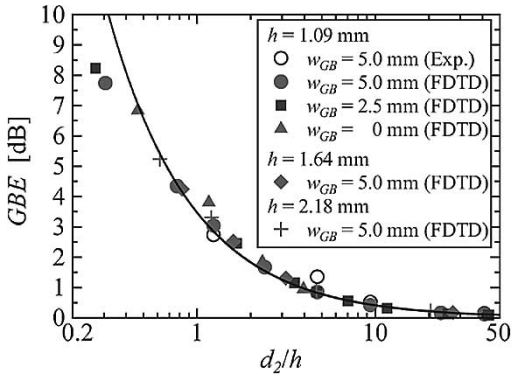

Fig. 13. Guard band effect GBE versus d_2/h.

As an example, GBE in the case of "$d_1 = 6.35$ mm, $w_{\rm GB} = 5.0$ mm," i.e., "d250GB," is shown in Fig. 12. Since the GBE is approximately constant over the considered frequency range, as GBE, the average value in the considered frequency range is used. The deviation between calculated and measured results is approximately 1 dB, and the average and the standard deviation of GBE is approximately 2.73 and 0.55 dB, respectively. Using the distance d_2 between the trace and GB1, and h, the relationship between GBE and d_2/h is shown in Fig. 13. The GBE can be expressed as an empirical equation with parameters determined with a correlation coefficient of 0.99 by the least squares method,

$$\mathrm{GBE} \approx 3.46 \left(\frac{d_2}{h}\right)^{-0.92} \tag{8}$$

where d_2 is the distance between the trace and the edge of GB1 ($d_2 = d_1 - w_{\rm GB}$), and $w_{\rm GB}$ is the width of the guard band. The solid line in Fig. 13 is the least squares curve fit given by (8). The points on this curve would have error of approximately 0.5 dB, because each GBE in Fig. 13 has the deviation as shown in

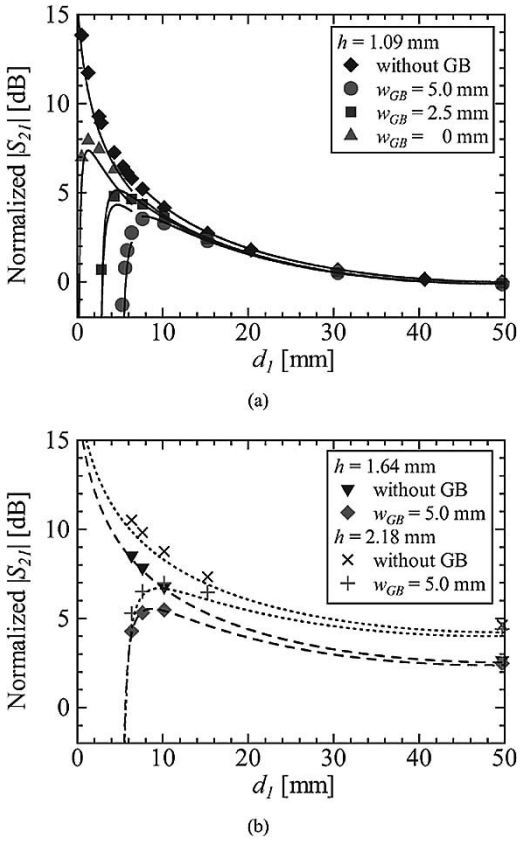

Fig. 14. Normalized $|S_{21}|$ versus d_1. Lines are calculated results from (6) and (9), and symbols are FDTD calculated results. (a) $h = 1.09$ mm. (b) $h = 1.64$ and 2.18 mm.

Fig. 12. However, as d_2 decreases and/or h increases, the GBE increases significantly.

Now, the guard band effect GBE is considered through $|S_{21}|_{\text{GB norm}}$. Using (6)–(8), the $|S_{21}|_{\text{GB norm}}$ is given as an empirical equation

$$|S_{21}|_{\text{GB norm}} = |S_{21}|_{\text{norm}} - \text{GBE} = 20\log_{10}\left(\frac{\frac{h}{h_{\text{ref}}}\frac{R_{\text{ref}}}{R}}{\sqrt{1-4(1-2\frac{h}{w})(\frac{s}{w})^2}}\right) - 3.46\left(\frac{d_2}{h}\right)^{-0.92}. \quad (9)$$

The relationship between the normalized $|S_{21}|$ and d_1 is shown in Fig. 14. In the case of "$h = 1.09$ mm," the normalized $|S_{21}|$ is not calculated for $6.35 \leq d_1 \leq 7.62$ mm, because the terminating resistor R in the case with $d_1 \geq 7.62$ mm is different from that with $d_1 \leq 6.35$ mm, as shown in Table I. As d_1 decreases and/or h increases, the normalized $|S_{21}|$ in the case without the guard band increases. On the other hand, the normalized $|S_{21}|$ in the case with a guard band has a peak and then decreases as d_1 is smaller. The calculated results (lines in Fig. 14) using (6) and (9) agree well with the FDTD calculated results (symbols). This indicates the effect of the guard band to suppress the CM current can be estimated using (9).

Using the ratio of d_1 to $w/2$ in (9), a design guideline can be formulated. The ratio $d_1/(w/2)$ between the cases with and without a guard band can be compared for a significant reduction in the normalized $|S_{21}|$. As an example, the cases where the normalized $|S_{21}| < 3$ dB is required in PCB designs are compared. Fig. 15 shows the normalized $|S_{21}|$ for the case of a PCB with $h = 1.09$ m, where $R_{\text{ref}}/R = 1$ in (6) and (9). The $d_1/(w/2)$ of the case without the guard band should be larger than 0.28, as mentioned in Section III. On the other hand, the case with a guard band can be set to approximately 0.12. This indicates that the guard band allows for a trace to be routed near a PCB edge, and the necessary "keep-out" area (i.e., distance d_1) can be set smaller. Though the effect of a guard band was discussed in the case without a thin wire attached, these results can be applied to the case with a thin wire. Therefore, a guard band will be effective for high-density PCB packaging with high-speed traces.

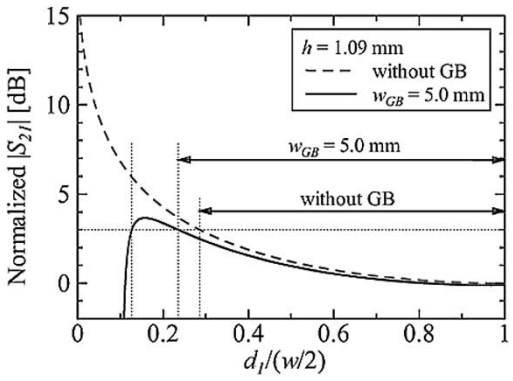

Fig. 15. Normalized $|S_{21}|$ versus $d_1/(w/2)$. Lines are calculated results from (6) and (9).

V. Conclusion

The CM current due to a trace near a PCB edge and its suppression by a guard band was studied experimentally and with FDTD modeling. First, a PCB noise source that results from the nonzero impedance of the PCB ground plane was discussed to determine the necessary "keep-out" area on the PCB edge for high-speed trace routing. The results suggest that $d_1/(w/2) > 0.28$ may be most suitable in the design of traces on a PCB without a guard band. Second, the effect of the guard band on CM current was discussed. The guard band parallel to and near a trace was most effective in suppressing the CM current. And, the cross-sectional magnetic field distribution at the center of the PCB with and without the guard band was calculated using the FDTD method. The guard band decreases the magnetic field distributed on the under side of a PCB. These results indicate the guard band is effective in suppressing CM current. Finally, an empirical formula to quantify the relationship between the position of a trace and CM current of the case with a guard band was proposed. Calculated results using an empirical formula and FDTD modeling were in good agreement. As d_2/h decreases, the effect of the guard band to suppress the CM current increases. The guard band allows for a trace to be routed near a PCB edge, and the necessary "keep-out" area can be set smaller.

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