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Analysis of a Novel Four-Level DC/DC Boost Converter

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Abstract **- In this paper, novel two-quadrant buck/boost and one-quadrant boost four-level DC/DC converters are introduced. The primary application for these converters is that of interfacing a low voltage DC source, such as a fuel cell or battery, to a high-voltage four-level inverter. One important feature of the four-level DC/DC converters proposed herein is the ability to perform the power conversion and balance the inverter capacitor voltages simultaneously. With the capacitor voltage balancing, it is possible to obtain the full voltage from the inverter. For the boost converter, the steady-state and Non-Linear Average-Value (NLAM) models are developed. The NLAM is verified against a detailed simulation of a four-level converter/inverter drive system.**

Keywords: Multi-level converters, four-level converters, DC/DC converters, average-value modeling, triangle modulation, current-regulated control.

I. Introduction

The general trend in power electronics devices has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. However, the increase in switching frequency increases the switching losses which become especially significant at high power levels. Several methods for decreasing switching losses have been proposed including constructing resonant inverters and multi-level inverters [1].

Resonant inverters avoid switching losses by adding an LC resonant circuit to the hard switched inverter topology. The inverter transistors can be switched when their voltage or current is zero, thus mitigating switching losses. Examples of this type of inverter include the resonant DC link [2], and the Auxiliary Resonant Commutated Pole inverter (ARCP) [3,4]. One disadvantage of resonant inverters is that the added resonant circuitry will increase the complexity and cost of the inverter control. Furthermore, high IGBT switching edge rates can create switch level control problems.

Multi-level inverters offer another approach to reducing switching losses. In particular, these converters offer a high number of switching states so that the inverter output voltage can be "stepped" in smaller increments [5-11]. This allows mitigation of harmonics at a low switching frequencies thereby reducing switching losses. In addition, EMC concerns are reduced through the lower common mode current facilitated by lower dv/dt's produced by the smaller voltage steps. One disadvantages of these techniques are that they require a high number of switching devices. The primary disadvantage of multi-level inverters is that they must be supplied from isolated DC voltage sources or a bank of series capacitors with balanced voltages. In systems where isolated DC sources are not practical, capacitor voltage balancing becomes the principal limitation for multi-level inverters.

One of the most popular industrial multi-level inverters is the diode clamped three-level inverter [5,7,8,10]. It has been well established that the DC capacitor voltages can be readily balanced through the use of straightforward selection of redundant inverter switching states [10]. However, for inverters with a higher number of levels, the voltage balancing through redundant state selection limits the output voltage to 50% of the maximum [12,13]. For this reason, some systems incorporate auxiliary DC/DC converters for capacitor voltage balancing [14-17]. Some interesting three-level boost DC/DC converters have been proposed for systems that are powered from a low-voltage source such as a battery, fuel cell, or Superconducting Magnetic Energy Storage (SMES) [18-20]. In this paper, a novel four-level DC/DC converter is presented. The standard steady-state and average-value modeling techniques are applied to this new converter. Detailed and average-value model simulation demonstrates the converter performance.

II. Proposed Four-Level Dc/Dc Converter

A. Converter Description

Figure 1 shows the novel four-level two-quadrant converter proposed herein. This converter can operate as a boost or buck converter depending on weather the DC source v_{dc} is supplying or absorbing power respectively. For many applications, bi-directional power flow is not necessary and the semiconductor parts count can be reduced to the topology shown in Figure 2. In a standard boost converter, one transistor and one diode are used for the boost process [21,22]. In this new topology, two additional transistors are added in order to provide additional switching states that can be used to balance the capacitor voltages. It should be pointed out that although there are three times as many transistors as with a standard boost converter, the switches are rated at 1/3 of the DC voltage and thus the overall semiconductor cost is roughly the same. Figure 3 shows the possible switching states of the four-level DC/DC converter. States 0 and 4 are the two states typically used for DC/DC boost conversion. Due to the nature of the motor impedance load and the switching of the four-level inverter transistors, the voltage of the center capacitor v_{c2} tends to discharge to zero in this system.

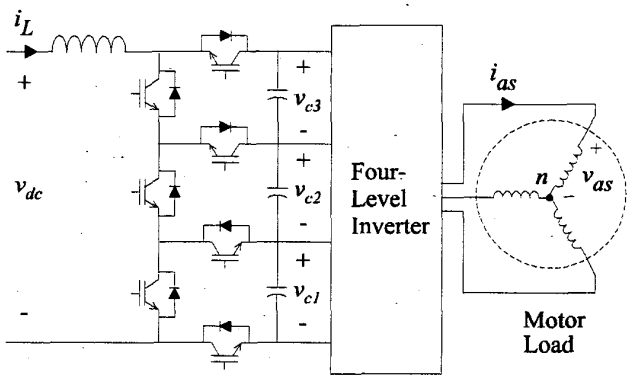

Figure 1. Proposed 4-level two-quadrant DC/DC converter.

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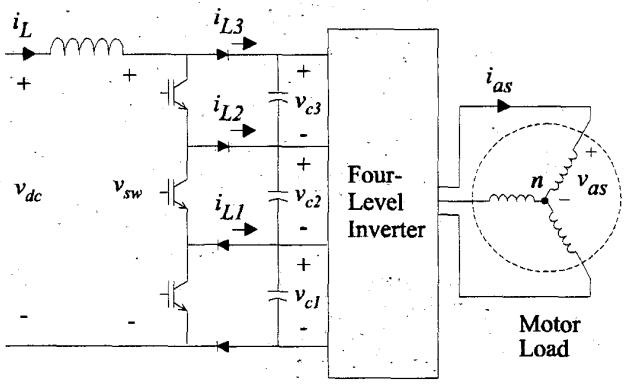

Figure 2. Proposed 4-level one-quadrant boost converter.

For this reason, state 1 is inserted in the switching sequence in order to increase the charge on the center capacitor. A secondary goal of this converter is to balance the voltages on the upper and lower capacitors. Although this is typically not difficult in four-level inverters, states 2 and 3 can be added to ensure this balance.

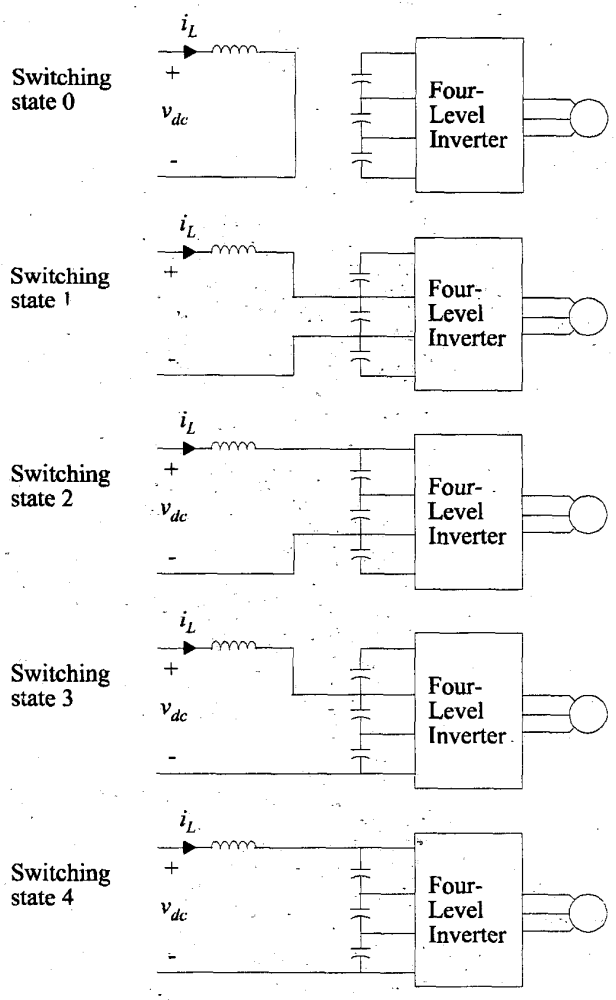

Figure 3. Four-level one-quadrant converter switching states.

B. Switching Sequence

One advantage of multi-level DC/DC power conversion is a reduction in the inductor current ripple when compared to a standard DC/DC converter. For the three-level DC/DC converter, a reduction in current ripple can be accomplished by defining the switching sequence as a function of the input and output voltages [18-20]. In the case of the four-level converter, it is not possible to reduce the current ripple for all operating conditions and simultaneously balance the capacitor voltages. Therefore, one sequence has been chosen with the objective of balancing the capacitor voltages. The overall switching state sequence suggested for this converter is 0 - 1 - (2 or 3) - 4 - (2 or 3) - 1 - 0. The state diagram for this sequence is shown in Figure 4. Note that this sequence is similar to that of a standard DC/DC converter with two additional switching states. Two additional duty cycles are defined in the sequence timing for control of the additional states. The timing sequence is defined by

$$\text{state} = \begin{cases} 0, & 0 \le t < d_1 T \\ 1, & d_1 T \le t < (d_1 + d_2) T \\ 2/3, & (d_1 + d_2) T \le t < (d_1 + d_2 + d_3) T \\ 4, & (d_1 + d_2 + d_3) T \le t < T \end{cases} \quad (1)$$

where d_1, d_2, and d_3 are the controller duty cycles and T is the total time spent in the switching states. The remainder of the sequence is to reverse the order spending the same amount of time in each state as before. Therefore, the total time of the switching controller is $T_{sw} = 2T$.

The amount of time spent at the particular switching state can be controlled depending on the desired output voltage and the capacitor voltage imbalance. For example, the time spent at switching state 1 can be increased in order to increase the voltage across the center capacitor. The time spent at states 2 and 3 can be controlled to maintain the voltage balance between the upper and lower capacitors. The choice as to which state to switch to during the sequence (2 or 3) is made depending on which of the two capacitor voltages v_{c1} or v_{c3} is underbalanced with respect to the other.

C. Steady-State Modeling

As with other types of DC/DC converters, it is instructive to perform a steady-state analysis of the converter driving a resistive load [18-21]. In the case of the four-level boost converter, the circuit topology is that of Figure 5. Since the goal of this converter is to equalize the capacitor voltages, it will be assumed that the controller duty cycles have been set so that the capacitor voltages are equal, or

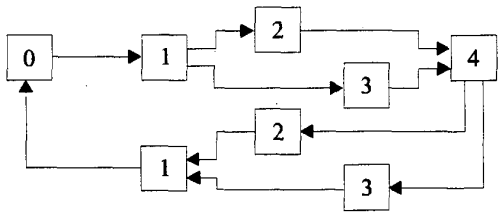

Figure 4. Four-level converter switching sequence.

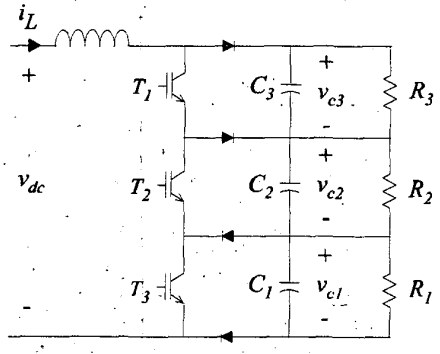

Figure 5. Four-level converter with resistive load.

$$v_{c1} = v_{c2} = v_{c3} = \frac{v_c}{3}. \tag{2}$$

It will also be assumed that $R_3 > R_1$ so that switching state 3 is used during the time when there is a choice between states 2 and 3. The resulting inductor current waveform is shown in Figure 6. For steady-state periodic operation, it is necessary that the average inductor voltage be zero. From this requirement, the output to input voltage ratio can be determined as

$$\frac{v_c}{v_{dc}} = \frac{1}{1 - d_1 - \frac{2}{3}d_2 - \frac{1}{3}d_3}. \tag{3}$$

Assuming that the converter losses are negligible, the average inductor current can be found from the output power and input voltage as

$$I_{Lavg} = \frac{v_c^2}{9v_{dc}}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right). \tag{4}$$

From the load equations and the fact that the average capacitor currents must be zero, it can be shown that the steady-state currents, defined in Figure 6, are

$$I_1 = I_{Lavg} + \frac{d_3 T_{sw}}{6L}(2v_c - 3v_{dc}) + \cdots$$
$$\frac{T_{sw}}{2L}(1 - d_1 - d_2 - d_3)(v_c - v_{dc}) + \cdots \tag{5}$$
$$\frac{d_2 T_{sw}(v_c - 3v_{dc})}{6L}$$

$$I_2 = I_{Lavg} + \frac{d_3 T_{sw}}{6L}(2v_c - 3v_{dc}) + \cdots$$
$$\frac{T_{sw}}{2L}(1 - d_1 - d_2 - d_3)(v_c - v_{dc}) \tag{6}$$

$$I_3 = I_{Lavg} + \frac{d_3 T_{sw}}{L}(2v_c - 3v_{dc}) + \cdots$$
$$\frac{T_{sw}}{2L}(1 - d_1 - d_2 - d_3)(v_c - v_{dc}) \tag{7}$$

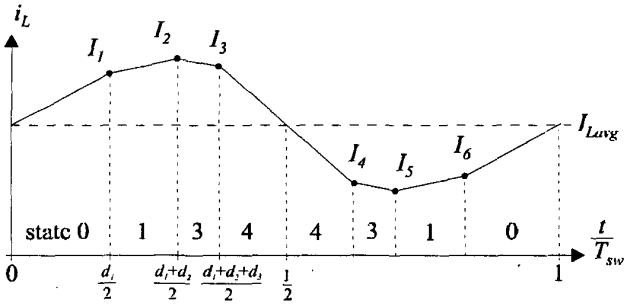

Figure 6. Steady-state inductor current waveform.

By waveform symmetry,

$$I_4 = 2I_{Lavg} - I_3 \tag{8}$$

$$I_5 = 2I_{Lavg} - I_2 \tag{9}$$

$$I_6 = 2I_{Lavg} - I_1. \tag{10}$$

For design purposes, it is often desirable to calculate the inductor current ripple ΔI_L. From (5-10), it can be seen that

$$\Delta I_L = 2\left|\max(I_1, I_2, I_3) - I_{Lavg}\right|. \tag{11}$$

Note that the maximum current (I_1, I_2, or I_3) depends on the shape of the inductor current and thus depends on the DC input and capacitor voltages. Regardless of which current is the maximum, it can be seen that the inductor current ripple decreases with increasing switching frequency, inductance, and load resistance as is typical of DC/DC converters.

It may be desirable to calculate the required duty cycles for a given set of load resistances. In this case, setting the average capacitor currents to zero yields three equations which can be solved for duty cycles resulting in

$$d_1 = 1 - \frac{3v_{dc}}{R_2 v_c\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)} \tag{12}$$

$$d_2 = \frac{3v_{dc}\left(\frac{1}{R_2} - \frac{1}{R_1}\right)}{v_c\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)} \tag{13}$$

$$d_3 = \frac{v_{dc}\left(\frac{1}{R_1} - \frac{1}{R_3}\right)}{v_c\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)}. \tag{14}$$

The steady-state model equations presented herein have been verified through the use of detailed computer simulation. Although the steady-state model is useful for design calculations, a dynamic model is needed for evaluating system transient performance.

D. Non-Linear Average-Value Modeling

The general concept of Non-Linear Average-Value Models (NLAM's) is that the high-frequency switching of the power

converter is represented on an average-value basis. These models provide insight into the operation of switching converters as well as suggest control strategies. Another advantage of NLAM's is that some simulation packages can linearize these models about an operating point and determine the state space matrices. From this information, classical control theory can be applied and the system stability can be evaluated [22].

Figure 7 shows the general structure of the NLAM where the converter switches have been replaced by dependant voltage and current sources. Therein, the ^ symbol denotes the fast-average which is the average-value of the quantity over one switching cycle of the converter T_{sw}. The converter waveforms used for determining the dependant source equations are shown in Figure 8 with the assumption that $v_{c3}>v_{c1}$ and state 3 is not used. If the inductor current ripple is neglected, the average-value equations are

$$\hat{v}_{sw} = \hat{v}_{c2}(1-d_1) + \hat{v}_{c1}(1-d_1-d_2) + \cdots \hat{v}_{c3}(1-d_1-d_2-d_3) \quad (15)$$

$$\hat{i}_{L1} = -\hat{i}_{dc}\, d_2 \quad (16)$$

$$\hat{i}_{L2} = \hat{i}_{dc}(d_2+d_3) \quad (17)$$

$$\hat{i}_{L3} = \hat{i}_L(1-d_1-d_2-d_3). \quad (18)$$

If $v_{c2}>v_{c3}$, then the average-value equations become

$$\hat{v}_{sw} = \hat{v}_{c2}(1-d_1) + \hat{v}_{c3}(1-d_1-d_2) + \cdots \hat{v}_{c1}(1-d_1-d_2-d_3) \quad (19)$$

$$\hat{i}_{L1} = -\hat{i}_{dc}(d_2+d_3) \quad (20)$$

$$\hat{i}_{L2} = \hat{i}_{dc}\, d_2 \quad (21)$$

$$\hat{i}_{L3} = \hat{i}_L(1-d_1-d_2). \quad (22)$$

For four-level inverter loads, the unbalance of capacitor voltages v_{c1} and v_{c3} is not severe and the controller will select state 2 over state 3 about one-half of the time. In this case, the two sets of equations can be averaged to yield one model. For example, an equation for v_{sw} can be obtained by averaging (15) and (19).

The NLAM can be used to evaluate the dynamic and steady-state performance of the converter without including the high-frequency switching of the controller. If a resistive load is connected to the NLAM, equations (3) and (12-14) can readily be derived. Alternatively, an NLAM of a four-level inverter can be

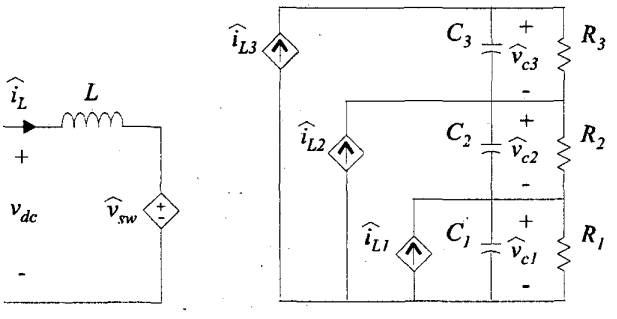

Figure 7. Converter average-value model structure.

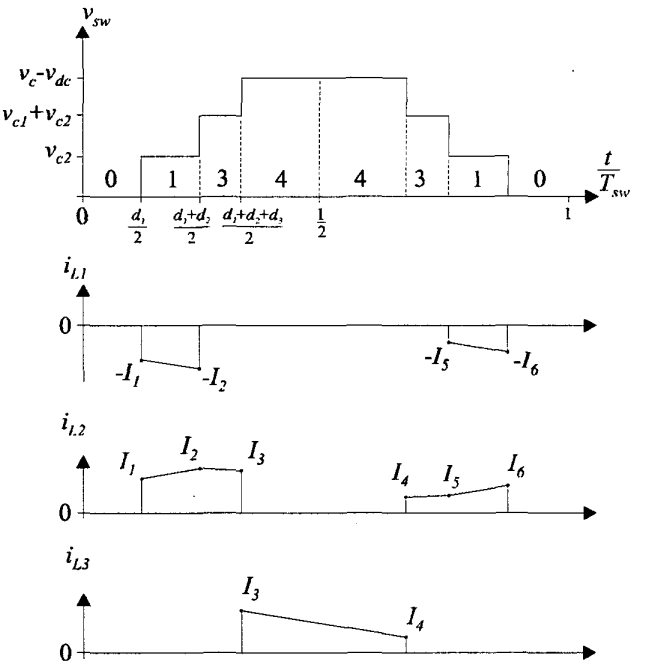

Figure 8. Converter switching waveforms.

connected to the converter NLAM for dynamic modeling of the system depicted in Figure 2.

III. Four-Level Inverter

Figure 9 illustrates a four-level diode clamped inverter [6-8,12,13]. The general theory of this inverter is that each phase (*a*, *b*, or *c*) can be electrically connected to the junctions d_0, d_1, d_2, and d_3 by appropriate switching of the inverter transistors. Assuming that the IGBT's operate as ideal switched, the *a*-phase switching can be modeled by an ideal positional switch as shown in Figure 10. The *b*- and *c*-phase circuits can be modeled by similar switches connecting to the same capacitor junctions. By pulse-width modulation of the positional switch, the inverter line-to-ground voltages v_{ag}, v_{bg}, and v_{cg} can be directly controlled. The motor line-to-neutral voltages can be calculated from the line-to-ground voltages by [23].

$$v_{as} = \frac{2}{3}v_{ag} - \frac{1}{3}v_{bg} - \frac{1}{3}v_{cg} \quad (23)$$

$$v_{bs} = \frac{2}{3}v_{bg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{cg} \quad (24)$$

$$v_{cs} = \frac{2}{3}v_{cg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{bg}. \quad (25)$$

In most motor control systems, the commanded phase currents are determined from the desired torque. A regulating control then generates commanded motor phase voltages based on the commanded currents. In general, these commanded voltages can be expresses as

$$v_{as}^* = \sqrt{2}v_s^*\cos(\theta_c) \quad (26)$$

$$v_{bs}^* = \sqrt{2}v_s^*\cos\left(\theta_c - \frac{2\pi}{3}\right) \quad (27)$$

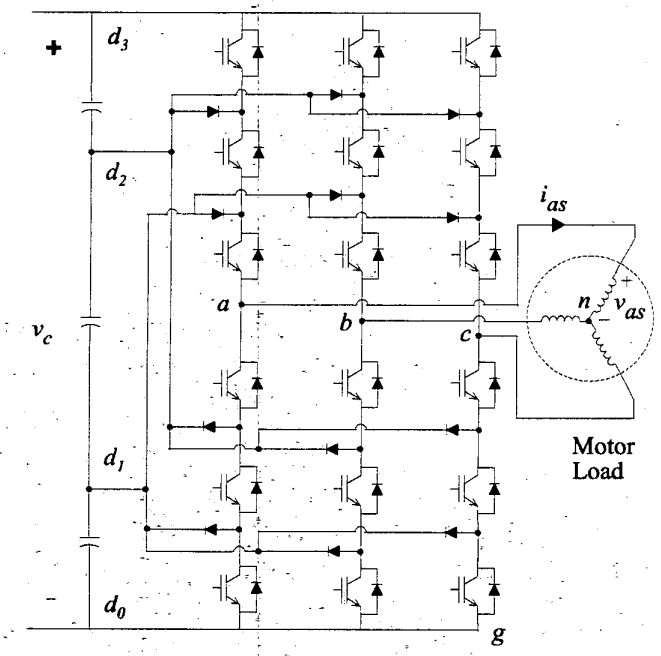

Figure 9. Four-level inverter topology.

$$v_{cs}^{*} = \sqrt{2} v_s^{*} \cos\left(\theta_c + \frac{2\pi}{3}\right) \tag{28}$$

where v_s* is the commanded RMS phase voltage and θ_c is the controller electrical angle. It can be noted from (23-25) that there is no unique set of line-to-ground voltages for a given set of commanded motor phase voltages. This is due to the fact that common-mode terms in the line-to-ground voltages will cancel when evaluating (23-25). One method of obtaining the desired motor phase voltages is to command line-to-ground voltages with a third harmonic term. It has been shown that this method allows the maximum voltage to be obtained from the inverter [24]. Using this method, the line-to-ground voltages can be commanded as

$$v_{ag}^{*} = \frac{v_c}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \tag{29}$$

$$v_{bg}^{*} = \frac{v_c}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{30}$$

$$v_{cg}^{*} = \frac{v_c}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{31}$$

where m is the modulation index that has a range of

$$0 \le m \le \frac{2}{\sqrt{3}} \tag{32}$$

in order to avoid over-modulation. Assuming that the commanded voltages are obtained by the PWM control, the fast-averages of the resulting motor phase voltages are

$$\hat{v}_{as} = \frac{m v_c}{2}\cos(\theta_c) \tag{33}$$

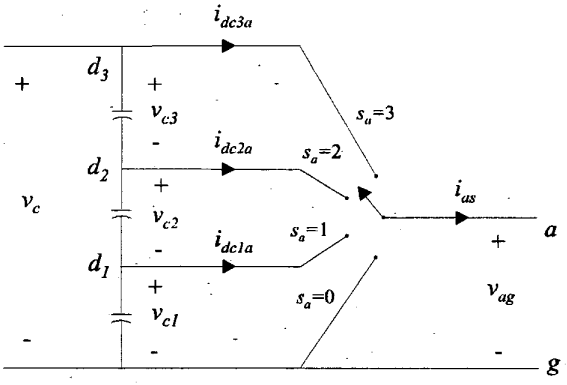

Figure 10. Equivalent switching of the four-level inverter.

$$\hat{v}_{bs} = \frac{m v_c}{2}\cos\left(\theta_c - \frac{2\pi}{3}\right) \tag{34}$$

$$\hat{v}_{cs} = \frac{m v_c}{2}\cos\left(\theta_c + \frac{2\pi}{3}\right). \tag{35}$$

By comparing (33-35) to (26-28), it can be seen that the desired voltage magnitude and phase angle can be set by selecting m and θ_c in (29-31). Typically, (29-31) are normalized to the DC voltage v_c. This yields duty cycles defined by

$$d_a = \frac{1}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \tag{36}$$

$$d_b = \frac{1}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{37}$$

$$d_c = \frac{1}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right]. \tag{38}$$

The duty cycles can then be integerized to determine the switching states for the PWM control. For example, if the a-phase duty cycle is integerized by

$$l_a = \mathrm{INT}(3 d_a) \tag{39}$$

then the PWM switching will be between levels s_a=l_a and s_a=l_a+1. If the clock frequency of the PWM controller is T_s, then the a-phase switching states for one cycle are

$$s_a = \begin{cases} l_a + 1, & 0 \le t < (3 d_a - l_a) T_s \\ l_a, & (3 d_a - l_a) T_s \le t \le T_s \end{cases}. \tag{40}$$

For the purposes of system model comparison, an average-value model of the four-level inverter has been developed. The structure of the a-phase of the average-value model is shown in Figure 11. Figure 12 shows the first step in the derivation of the average-value model dependant source equations. Therein, the modulation duty-cycle is plotted versus the controller electrical angle. The functions s_1, s_2, and s_3 represent the percent of time that the a-phase is switched to junctions d_1, d_2, and d_3 respectively. These switching functions are related to the a-phase duty cycle as shown in Figure 12. Using these switching functions, the currents drawn from the diode junctions are defined by

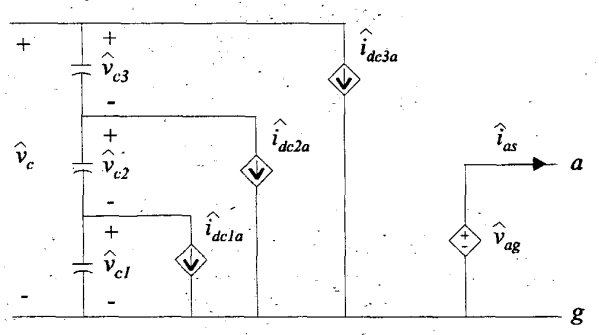

Figure 11. Average-value model of the four-level inverter.

$$i_{dc1a} = s_1 i_{as} \tag{41}$$

$$i_{dc1a} = s_1 i_{as} \tag{42}$$

$$i_{dc1a} = s_1 i_{as}. \tag{43}$$

For the average-value model to have variables which are constant in the steady-state, it is necessary to relate the a-phase current to the induction motor q- and d-axis currents in the controller reference frame. This relationship is given by [23]

$$i_{as} = i_{qs}^{c}\cos(\theta_c) + i_{ds}^{c}\sin(\theta_c). \tag{44}$$

The next step in the average-value model is to average the DC currents over one cycle of θ_c. The resulting expression is extensive and is not included herein. Due to the symmetry of the drive and modulation, the b- and c-phase average-value DC currents are identical to that of the a-phase. A similar averaging procedure is used to find the q- and d-axis induction motor voltages from the switching functions and the capacitor voltages.

IV. Four-Level System Simulations

Detailed and NLAM based simulations were performed on the converter / inverter system shown in Figure 2. The induction motor used in these studies is a 3.7kW machine with the parameters listed in Table I [23].

Table I. Induction motor parameters		
$r_s = 0.4\,\Omega$	$P = 4$	$r_r' = 0.227\,\Omega$
$L_{ls} = 5.7$ mH	$L_m = 64.4$ mH	$L_{lr}' = 4.6$ mH

The induction motor is operating at a constant speed of 183.3 rad/sec and a constant electrical frequency of 60 Hz ensured by setting

$$\theta_c = 2\pi f t \tag{45}$$

in the inverter control. The modulation index m is stepped from 0.6 to 1.13 resulting in a step change in applied voltage on the motor. For the detailed simulation, the PWM switching period is set to T_s=0.185 ms.

The DC/DC converter regulates the DC voltage supplied to the inverter and maintains capacitor voltage balance through controlling the duty cycles d_1, d_2, and d_3. This control can be challenging since the system is Multi-Input Multi-Output (MIMO). A MIMO control design may be the work of future research in this area. For the studies presented herein, a straightforward Proportional plus Integral (PI) control was used.

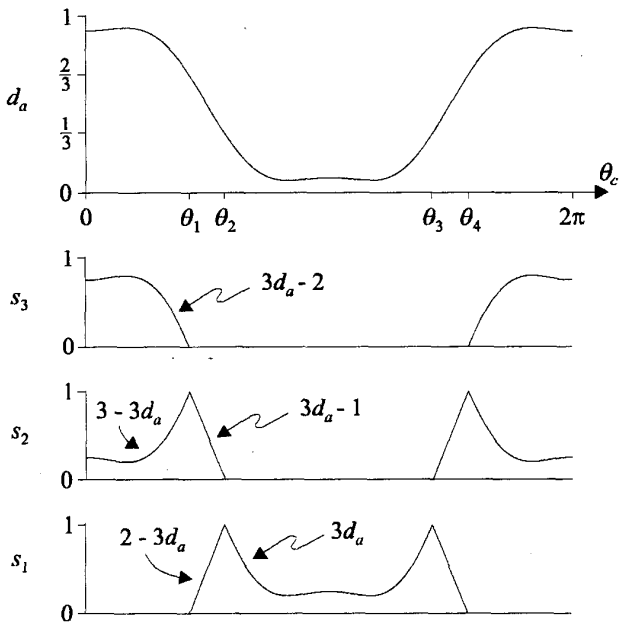

Figure 12. A-phase duty cycle and switching functions of the four-level inverter.

Use of this control was justified by examining the sensitivity of the system outputs (capacitor voltages) to the changing inputs (duty cycles). Using the NLAM, it was observed that the capacitor voltage v_{c2} was more sensitive to changes in d_2 than v_{c1} or v_{c3}. Furthermore, v_{c1} and v_{c3} were more sensitive to changes in d_1 than v_{c2}. This sensitivity somewhat decouples the control and allows for the following approximate control to be used.

$$d_1 = K_{p1}e_1 + K_{i1}\int e_1 dt \tag{46}$$

$$d_2 = K_{p2}e_2 + K_{i2}\int e_2 dt \tag{47}$$

where the errors e_1 and e_2 are defined by

$$e_1 = v_c^* - v_c \tag{48}$$

$$e_2 = v_{c2}^* - v_{c2}. \tag{49}$$

The commanded converter output voltage v_c^* was set to a constant value of 318 V. The commanded voltage on the center capacitor was set to

$$v_{c2}^* = \frac{1}{3}v_c. \tag{50}$$

The third duty cycle was set to a constant value of d_3=0.05. For this study, the PI controller gains were set to the values listed in Table II.

Table II. Converter PI controller gains.	
$K_{p1} = 0.001$	$K_{p2} = 0.2$
$K_{i1} = 0.01$	$K_{i2} = 0.5$

The DC input voltage was v_{dc}=150 V and the controller switching period was T_{sw}=0.1 ms. The converter inductance value was L=10 mH. The capacitor values were unevenly distributed so that the voltage ripple of all capacitors would be roughly the same in the detailed model. The values used were C_1=C_2=9900 μF and C_3=3300 μF.

Figures 13 and 14 show the simulation results for the detailed and NLAM models respectively. As can be seen, the capacitor voltages drop when the inverter modulation index is increased. The regulating control on the DC/DC converter then controls the duty cycles so that the capacitor voltages return to their desired values. The inductor current increases as the power to the motor

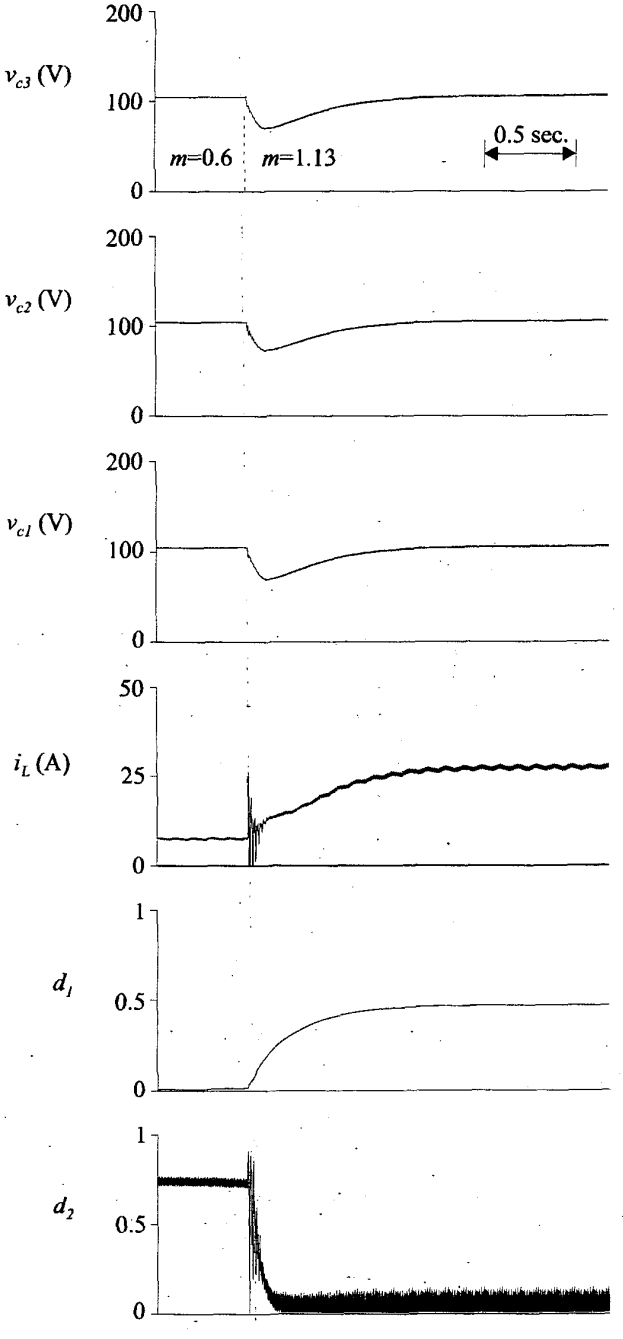

Figure 13. Detailed model prediction of system performance during a step change in modulation index.

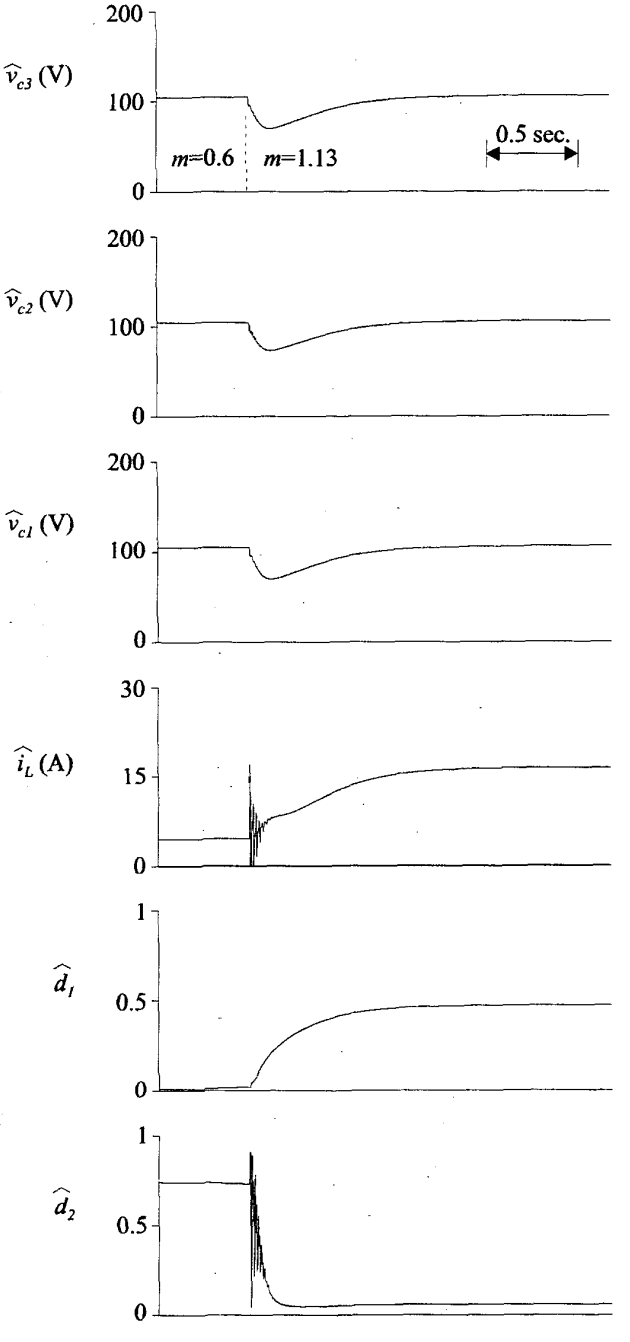

Figure 14. NLAM model prediction of system performance during a step change in modulation index.

increases. Notice from the detailed model that there are two components to the inductor current ripple. One component is due to the converter switching and the other is due to the capacitor voltage ripple. Figures 13 and 14 also display the controller duty cycles. Note that for m=0.6, the duty cycle d_1 is very low. This suggests an alternate switching sequence for m=0.6 where the switching state 0 is eliminated and the inductor current ripple is reduced as compared to a standard boost converter.

V. Conclusion

A novel four-level DC/DC converter has been introduced. The main objective of this converter is to supply a four-level diode-clamped inverter and provide capacitor voltage balancing as well as perform a boost operation. With the capacitor balancing controlled by the converter, the inverter can be operated up to its full output voltage (as compared to 50% of full output voltage when balancing the capacitors with the inverter switching). Steady-state and average-value modeling of the proposed converter is presented. A simulation study on the converter / inverter system demonstrates that the average-value model prediction compares favorably to a detailed simulation.

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