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An Improved Cascaded H-Bridge Multilevel Inverter Controlled by an Unbalanced Voltage Level Sigma-Delta Modulator

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***Abstract*—Multilevel inverters have been proven to be viable solutions for high-power automotive motor drive applications due to their high volt-ampere ratings. Cascaded H-bridge inverters are a promising breed of multilevel inverters which generally require several independent dc sources. Replacement of all but one of the dc sources with capacitors in cascaded H-bridge multilevel inverters, which leads to single-dc-source per-phase cascaded inverters, has recently gained popularity. However, very few efforts have been made to address the challenging problem of voltage regulation in the replacing capacitors. In this paper, applicability of a real-time voltage control technique named unbalanced voltage level sigma-delta modulation technique to provide voltage regulation across the replacing capacitors is examined. In addition, a new voltage ratio for the H-bridge cells is introduced, which simplifies the control tasks. Analytical and simulation results prove the effectiveness of the proposed scheme.**

***Keywords*— Delta-Sigma modulator; H-bridge multi-level inverter; voltage regulation; spectrum analysis**

I. INTRODUCTION

Multilevel inverters are mainly utilized to synthesize a desired single- or three-phase voltage waveform. They have found wide applications in automotive motor drives, static VAR compensators [1], and uninterruptible power supplies especially in high-power rating large vehicular motor drives (> 250kW), since high volt-ampere ratings are possible with these inverters. Their main advantages are low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency, capability to operate at high voltages, and modularity. In general, multilevel inverters are categorized into diode-clamped, flying capacitor, and cascaded H-bridge [2]. Fig. 1 shows the block diagram of a three-phase cascaded H-bridge inverter. As it can be observed, the inverter consists of main and auxiliary H-bridge cells in each phase. The structures of main and auxiliary cells are very similar. In Fig. 2, n is either 1 or 2 depicting the main or auxiliary inverters, respectively. As it can be seen, depending on the conduction status of four switches S_1, S_2, S_3, and S_4, each converter cell can generate three different voltage levels of $+V_n$, 0, and $-V_n$. H-bridge cells in each phase are connected in series; hence, the synthesized per-phase voltage waveform is the sum of all individual cell outputs. The output voltage of phase a can be described by the following equation (see Fig. 1).

$$V_{ag} = V_{a1} + V_{a2} \tag{1}$$

In early implementations [3-5], each H-bridge cell was fed by an independent dc source. Later, it was shown that only one cell needs to be supplied by a real dc power source and the remaining cells could be supplied with capacitors [6, 7]. However, studies show that voltage regulation of capacitors is not an easy task [8]. In previously reported works [6, 7], the ratio between the voltage of the main and auxiliary sources has been selected to be either 2:1 or 3:1, which leads to several limitations for the capacitor voltage regulation. In this paper, voltage ratio of 4:1, which simplifies the control task, is proposed and successfully implemented.

Furthermore, sigma-delta modulation (SDM) is proposed for voltage regulation across the replacing capacitors in the auxiliary cells. SDM has successfully been applied to synthesize desired voltage waveforms in discrete pulse modulated system such as resonant dc link inverters [9, 10]. The block diagram of a conventional two-level SDM is shown in Fig. 3. In Fig. 3, V_{ref} represents the desired output voltage, V_o is the synthesized output voltage, and f_s represents the sampling frequency of the system. The modulator encodes the reference signal

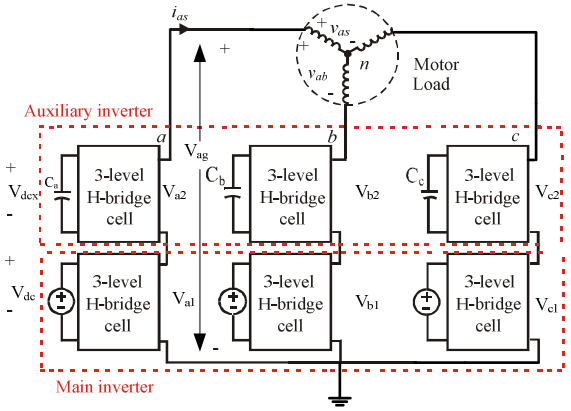

Figure 1. Block diagram of a three-phase cascaded H-bridge inverter

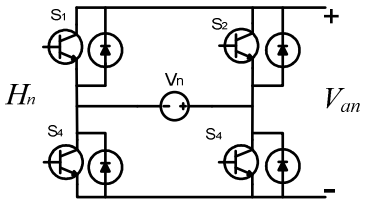

Figure 2. Circuit diagram of the main and auxiliary H-bridge cells

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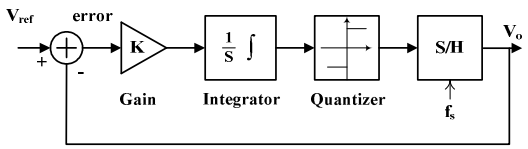

Figure 3. Block diagram of a two-level sigma-delta modulator

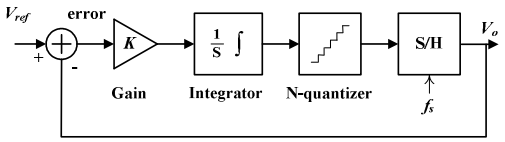

Figure 4. Block diagram representation of a multilevel sigma - delta modulator

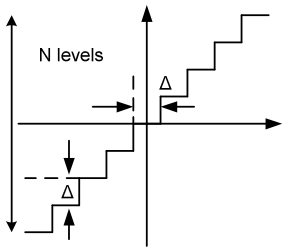

Figure 5. Static transfer characteristics of a uniform quantizer

V_{ref} into a two-level output V_o. The output is fed back and compared with the reference signal through an integrator. Under normal operating conditions, the output signal has to track the input signal with zero average error.

Sigma-delta modulation technique and appropriate selection of voltage ratio in H-bridge cells are the main focus of this paper. In Section II, SDM and its principles of operation are briefly introduced. The use of SDM for driving multi-level converter with two DC sources and selection of parameters are discussed in Section III. Voltage ratio selection is discussed in Section IV. Application of SDM to single-dc-source cascaded H-bridge multilevel inverters is discussed in Section V. Simulation results are also presented in this section. Concluding remarks and overall evaluation of the proposed method are included in Section VI and Section VII.

II. SIGMA DELTA MODULATION (SDM)

SDM can be extended to synthesize a multilevel waveform by replacing the binary quantizer with an N-level quantizer corresponding to the number of the levels of the multilevel inverter. The block diagram of the new SDM is depicted in Fig. 4.

Modulator design task requires selection of amplifier gain K, the saturation limits of the integrator block, and the sampling frequency f_s. A brief analysis of the system performance is done using the static transfer characteristics of a uniform quantizer as illustrated in Fig. 5.

Normally, the static transfer characteristics of the uniform N-level quantizer features step widths and step heights that are equal in magnitude this represents equal dc bus levels.As may be seen, each step width and the corresponding step height are of magnitude Δ. For a normalized uniform quantizer with N number of levels the relation between N and A will be

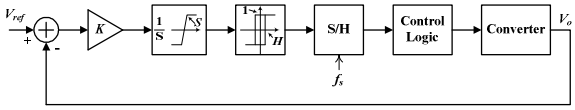

Figure 6. Control block diagram of SDM driving multilevel converter

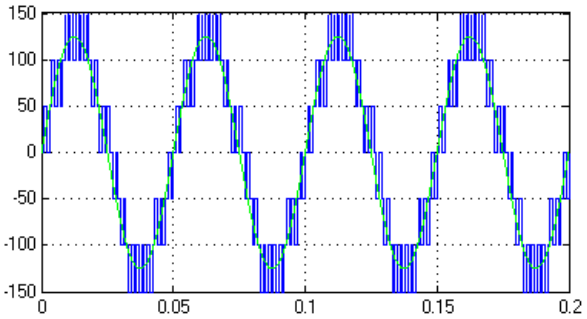

Figure 7. The output voltage which is good case

$$\Delta(N-1) = 2 \tag{2}$$

And the optimum choice of K and f_s will be determined by

$$K / f_s \le 1 \tag{3}$$

However, in this case, each voltage level is the same and the voltage of the capacitor cannot be balanced since the voltage drop during the discharging period is much larger than the voltage increase in capacitor voltage during the charging period. So an unequal voltage level Sigma-delta modulator will be used here.

III. USING SDM TO DRIVE A MULTI-LEVEL CONVERTER WITH TWO DC SOURCES

Previously, each H-bridge cell was fed by an independent dc source like a battery. The control diagram for this case can be shown as Fig.6. The priciples of operation is as follows: the reference voltage is a sinusoidal waveform, and the output voltage is tracking the reference voltage. The output of the modulator changes between the states +1 or -1 like a logic signal in time defined by the sampled frequency f_s and is used to drive the converter. The adjustable parameters are gain of the controller K, saturation limits of the integrator S, sampling frequency f_s, and threshold of the hysteresis loop H. Tracking characteristics of the synthesized output voltage depends on the appropriate selection of the above mentioned parameters. For instance, for H = 0.01, f_s = 5 kHz, S =±0.05, and K = 10 one would be able to get the output voltage that is depicted in Fig. 7. On the other hand, for H = 0.0005, f_s = 5 kHz, S =±0.5, and K = 10. The results are not satisfactory (see Fig. 8).

High sampling frequency is preferred to guarantee that the loop is fast enough to track the reference signal. Studies show that the samplimg frequency needs to be at least 30 times of the frequency of the reference signal. For gain K and the saturation limits of the integrator block, simulations show that small values for gain K (e.g. 0.1) do not result in a good tracking response. However, values of 1 and larger are satisfactory. Saturation limits of the integrator block have a similar affect like gain K.

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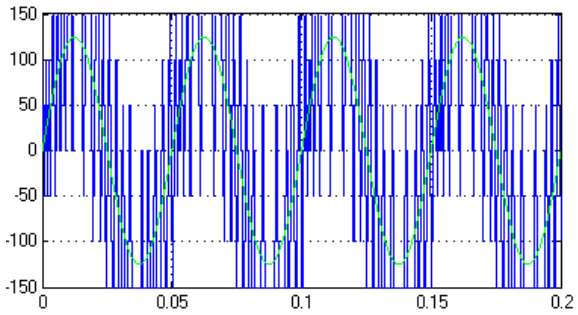

Figure 8. The output voltage which is bad case

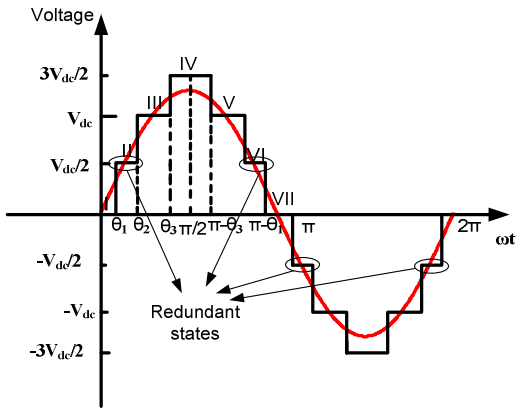

Figure 9. Output voltage redundancy for 2:1 ratio

IV. VOLTAGE RATIO SELECTION

As mentioned earlier, it has been proven that only one dc source per phase is needed in a multilevel inverter and others can be replaced with capacitors. In that case, the challenge is to regulate the voltage of the replacing capacitors [8]. Two approaches have been introduced in the literature which are redundancy [7], [11], [12], [13] and level reduction [6] methods. These two approaches both impose new limitations to the system. Redundancy method only works for a very limited load range [8] and level reduction method gives up on two of the output voltage levels, which leads to higher harmonic distortion.

Usually, the voltage ratio of the main and auxiliary inverters is selected to be 2:1 [7]; therefore, output voltage has only seven levels, as depicted in Fig. 9. In this case, V_{dc} is the voltage level of the main cell and $V_{dc}/2$ is that of the auxiliary cell.

Based on Fig. 9, one fourth of a period could be divided into the following subintervals

I. $0 < \omega t < \theta_1$ no capacitor charge or discharge
II. $\theta_1 < \omega t < \theta_2$ capacitor charge or discharge depending on the capacitor voltage
III. $\theta_2 < \omega t < \theta_3$ no capacitor charge or discharge
IV. $\theta_3 < \omega t < \pi-\theta_3$ capacitor discharge
V. $\pi-\theta_3 < \omega t < \pi- \theta_2$ no capacitor discharge
VI. $\pi - \theta_2 < \omega t < \pi-\theta_1$ capacitor charge or discharge depending on the capacitor voltage
VII. $\pi - \theta_1 < \omega t < \pi$ no capacitor charge or discharge

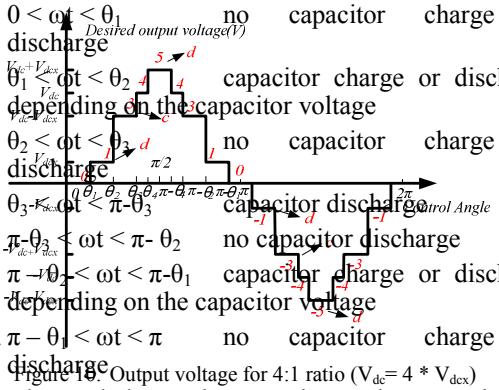

Figure 10. Output voltage for 4:1 ratio (V_{dc}= 4 * V_{dcx})

In order to balance the capacitor voltage, period IV should be very short otherwise the capacitor voltage will decrease continuously since discharging times will be longer than charging times [8]. To overcome this disadvantage, voltage ratio of 4:1 is proposed, as depicted in Fig. 10. In this case, there is no redundancy and therefore output voltage has nine levels. Capacitor is discharged when output voltage is at level 1 while it is charged when output voltage is at level 3. Therefore one fourth of a period could be divided into the following subintervals

I. $0 < \omega t < \theta 1$ no capacitor charge or discharge (level 0)
II. $\theta 1 < \omega t < \theta 2$ capacitor discharge (level 1)
III. $\theta 2 < \omega t < \theta 3$ capacitor charge (level 3)
IV. $\theta 3 < \omega t < \theta 4$ no capacitor charge or discharge (level 4)
V. $\theta 4 < \omega t < \pi- \theta 4$ capacitor discharge (level 5)
VI. $\pi - \theta 4 < \omega t < \pi-\theta 3$ no capacitor charge or discharge (level 4)
VII. $\pi - \theta 3 < \omega t < \pi - \theta 2$ capacitor charge (level 3)
VIII. $\pi - \theta 2 < \omega t < \pi - \theta 1$ capacitor discharge (level 1)
IX. $\pi - \theta 1 < \omega t < 2\pi$ no capacitor charge or discharge (level 0)

By comparing modes II and III, it can be observed that capacitor is discharged when the output voltage (and hence output current) is smaller and charged with a larger current. In this way, there is a higher chance of balancing the capacitor voltage successfully as opposed to the 2:1 case.

V. SDM APPLIED TO THE MULITLEVEL H-BRIDGE INVERTER

Instead of conventional stair-case modulation, SDM is proposed to push the undesired harmonic components of the output voltage to higher frequencies, as depicted in Fig. 11. V_{ref} is the reference signal, which is sinusoidal.

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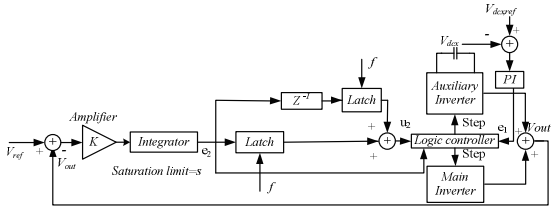

Figure 11. Proposed sigma-delta modulation applied to the multilevel inverter

TABLE I.
CONTROL LOGIC OF LOGIC CONTROLLER

u2	e2	e1	Discrete step
Level 0	1	x	Level 1
Level 0	-1	x	Level -1
Level 1	1	1	Level 3
Level 1	1	-1	Level 1
Level 1	-1	x	Level 0
Level 3	1	1	Level 3
Level 3	1	-1	Level 4
Level 3	-1	1	Level 3
Level 3	-1	-1	Level 1
Level 4	1	x	Level 5
Level 4	-1	x	Level 3
Level 5	-1	x	Level 4
Level -1	1	x	Level 0
Level -1	-1	1	Level -3
Level -1	-1	-1	Level -1
Level -3	1	1	Level -3
Level -3	1	-1	Level -1
Level -3	-1	1	Level -3
Level -3	-1	-1	Level -4
Level -4	1	x	Level -3
Level -4	-1	x	Level -5
Level -5	1	x	Level -4

The output voltage of the inverter V_{out} is compared with the reference signal V_{ref} and the resulting error is fed in to an integrator. The output of this block is named e_2 which is one of the control signals of the logic controller. The other is the integration of the error signal between the desired sinusoidal output and the staircase output e_2. These two error signals are then quantized into one of the two possible levels 1 or -1 depending on its polarity. Then a simple logic circuit decides on which switch has to be turned ON, which can be seen in Table I where u_2 is the previous status of the output voltage stage and discrete step is the next stage of the output voltage.

The output of the logic controller block step has 9 levels which are 0, ±1, ±3, ±4, ±5. Accordingly, the output of the inverter is 0, $\pm V_{dcx}$, $\pm (V_{dc}-V_{dcx})$, V_{dcx}, $\pm V_{dc}$, $\pm(V_{dc}+V_{dcx})$.

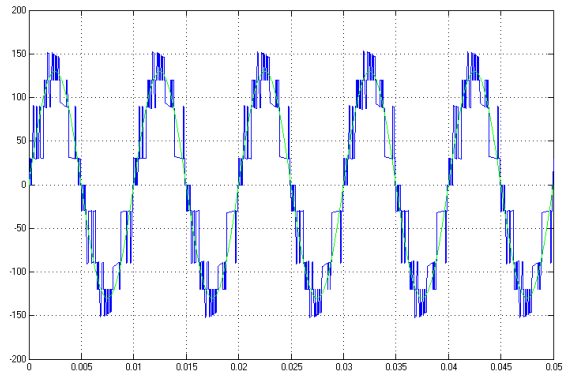

Figure 12. Output voltage waveform of the H-bridge multilevel inverter and its reference

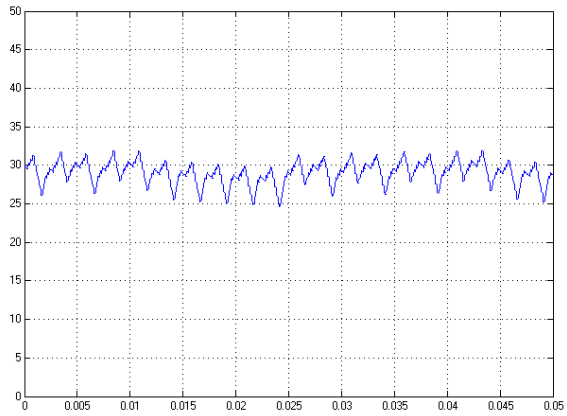

Figure 13. Regulation voltage across the capacitor in the auxiliary cell

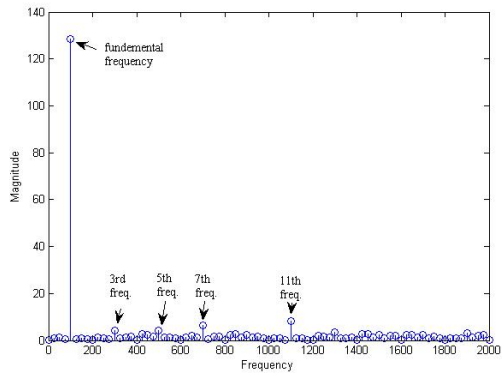

Figure 14. The spectrum of the output voltage

Fig. 12 depicts the output voltage waveform of the inverter. As it can be observed, SDM modulation is successful in tracking the sinusoidal reference signal. Fig. 13 shows the capacitor voltage in the auxiliary H-bridge cell where the amplitude of V_{ref} is 131V; the fundamental frequency is 100 Hz, the gain of the controller (K) is 10, the saturation limits of the integrator are ±0.005, the sampler frequency is 10 kHz, and the threshold of the hysteresis loop is 0.0001, the value of the capacitor is 0.001F and the load is a resistive load which is 10Ω. It is obvious that capacitor voltage is well regulated. Selection of a larger capacitor would result in lower voltage ripple.

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VI. SPECTRUM ANALYSIS

Normally, the sigma-delta modulation has a problem in which output signal frequency spectrum is worse than the PWM frequency spectrum. So one need to improve this spectral behavior by using different types of high order modulators such as interpolative modulators [14], cascaded modulators [15-17] and adaptive modulators [18-20]. However, in unbalanced voltage level Sigma-Delta modulator, the spectral behavior is good with the THD equal to 0.87% which can be shown in Fig.14.

VII. CONCLUSION

A cascaded H-bridge multilevel inverter, which requires only one dc source, driving a three phase motor has been analyzed in this paper. The inverter is proposed to have voltage ratio of 4:1, which leads to nine output voltage levels. In order to provide sinusoidal tracking characteristics, sigma-delta modulation technique is employed. Simulation results show that capacitor voltage regulation for the replacing capacitors is possible.

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