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Shuai Lu

Keith Corzine

Missouri University of Science and Technology

T. H. Fikse

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Advanced Control of Cascaded Multilevel Drives Based on P-Q Theory

Shuai Lu and Keith A. Corzine

Department of Electrical Engineering
University of Missouri - Rolla
1870 Miner Circle
Rolla, MO 65401

Tom H. Fikse

Senior Engineer
Naval Surface Warfare Center
5001 S. Broad Street
Philadelphia, PA 19112

Abstract - In recent years, there has been significant development on the cascaded multilevel inverter wherein the series connection is accomplished by splitting the neutral point of the load and driving both ends with power converters. This splits the power between a "bulk" inverter supplying higher-voltage low-frequency power and a "conditioning" inverter supplying low-voltage high-frequency power and leads to exceptional power quality which is necessary in applications such as Naval propulsion that require extremely low THD. This paper reports the development of a new control method for the cascaded multi-level inverter. The primary advantage of this new control is that the bulk inverter is controlled to switch at the fundamental frequency and therefore high-power switching devices such as IGBTs can be utilized. The conditioning inverter control is formulated in terms of its real and reactive power flow. This *P-Q* theory results in a simplified method of switching the conditioning inverter where the average real power flow into it can be commanded to zero so that it can be supplied solely from a capacitor source. Detailed simulations on an effective eight-level cascaded inverter are shown to validate the proposed control.

I. INTRODUCTION

This paper presents new research relating to the control of the cascaded multilevel inverter where two multilevel inverters are series connected by splitting the neutral point of the load [1-4]. This topology has several advantages over a traditional inverter for medium-voltage systems including higher voltage capability, higher power quality, lower dv/dt , and lower switching losses. Previous research has shown that if the two multilevel inverters are operating at different voltages, then the number of overall voltage levels is increased leading to exceptional power quality [2], and this also results in a natural split of the fundamental and PWM frequency between the higher-voltage "bulk" inverter and a lower-voltage "conditioning" inverter by natural sampled modulation [1]. In medium-voltage applications this allows IGBT's to be used in the bulk inverter and IGBTs to be used in the conditioning inverter. However, the split is not completely straightforward when the inverter dc voltage ratio is set to 3:1 and there will still be some high frequency switching in the bulk inverter output; a condition which may be difficult to achieve with IGBTs. Additionally, for some applications, such as Naval ship propulsion, the use of a single dc voltage source is preferred, so one inverter will be supplied by a purely capacitive source. This was achieved in previous research by properly selecting the redundant switching states (RSS) [1]. This, however, demands extra high frequency switching from the bulk inverter.

In this paper, a new control method is presented where the switching states command of the bulk inverter follows a space vector pattern of a typical three-level block switching voltage waveform at the fundamental frequency. The conditioning inverter control commands PWM switching to compensate the harmonics from the bulk inverter. To accomplish this, the control is formulated in terms of real and reactive power compensation (*P-Q* theory). This also proves to be a robust way of regulating the conditioning inverter capacitor voltage by simply adding a control term to the real power. Discussion of the operating regions and limitation of the control is also included. Detailed simulations verify the proposed control.

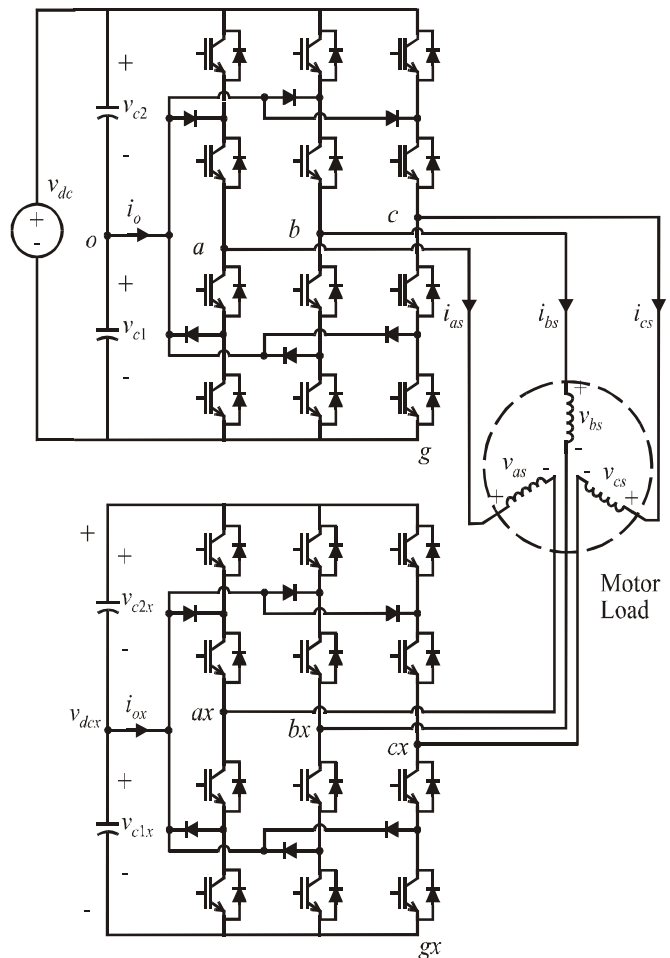


Figure 1. The cascade-3/3 multi-level inverter..

II. THE CASCADE-3/3 INVERTER TOPOLOGY

Figure 1 shows the topology of the cascade-3/3 motor drive. Therein, a three-level "bulk" inverter supplies the motor from the dc source v_{dc} . The neutral point of the machine is opened up and the other end of each phase is connected to another three-level inverter. Previous research has shown that this inverter is capable of operating with nine-level performance if the voltage ratio is set to $v_{dc} = 3v_{dcx}$ [3]. For applications where only one source is available, a capacitor supplies the "conditioning" inverter dc source v_{dcx} and its voltage is regulated using the control [1]. For this system, the line-to-ground voltages of the bulk and conditioning inverter can be computed as a function of the switching states by

$$\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} = \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} \frac{v_{dc}}{2} \quad (1)$$

$$\begin{bmatrix} v_{agx} \\ v_{bgx} \\ v_{cgx} \end{bmatrix} = \begin{bmatrix} s_{ax} \\ s_{bx} \\ s_{cx} \end{bmatrix} \frac{v_{dcx}}{2} \quad (2)$$

respectively. In (1-2) s_a , s_b , and s_c are the switching states of the bulk inverter and they may take on values of 0,1, or 2 as described in [1]. Likewise s_{ax} , s_{bx} , and s_{cx} are the switching states of the conditioning inverter. It is also assumed in (1-2) that the capacitors of each inverter are charged to half of the total dc voltage for that inverter. This condition is easily realized in the three-level inverter system. The motor load voltages can be calculated from the line-to-ground voltages using

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} - v_{agx} \\ v_{bg} - v_{bgx} \\ v_{cg} - v_{cgx} \end{bmatrix} \quad (3)$$

Equations (1-3) allow calculation of the load voltages given the dc voltages and switching states of the controller.

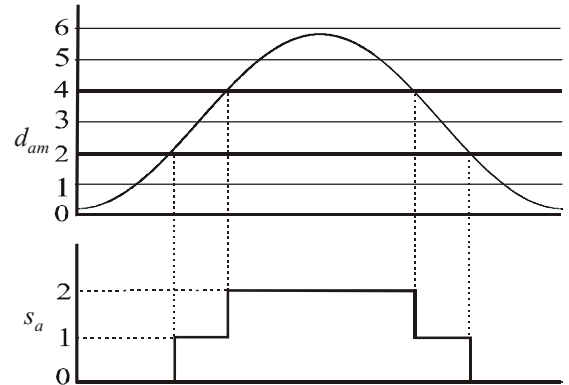
III. INVERTER CONTROL USING RSS

When the inverter dc voltage ratio is set to 3:1, natural sampled modulation (sine-triangle or duty cycle modulation [1]) can not produce bulk inverter switching purely at the fundamental frequency. This is the case because the natural sampling modulator will create switching states per-phase first and the result will be mapped to the bulk and conditioning inverter switching states. The exact mapping is shown in Tables I and II for the case where the dc voltage ratio is 2:1 and 3:1 respectively.

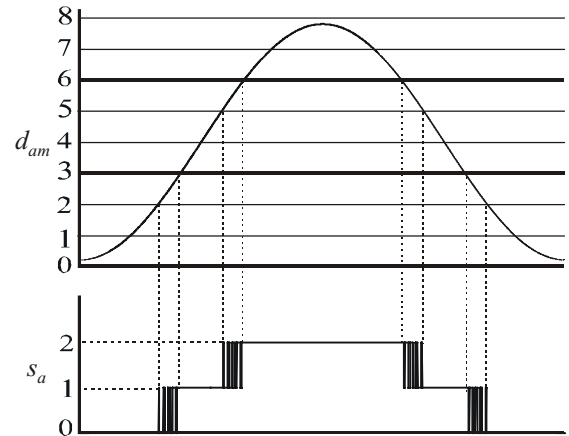
Table I. Inverter switching states ($v_{dc} = 2v_{dcx}$).									
s	0	1	2	3	4	5	6	7	8
s_a	0	0	0	1	1	1	2	2	2
s_{ax}	2	1	0	2	1	0	2	1	0

Table II. Inverter switching states ($v_{dc} = 3v_{dcx}$).									
s	0	1	2	3	4	5	6	7	8
s_a	0			1			2		
s_{ax}	2	1	0	2	1	0	2	1	0

where s is the combined switching state from the modulator. Figure 2 shows the bulk inverter states that result from natural sampling modulation for dc voltage ratios of 2:1 and 3:1. Seven- and nine-level evenly spaced thresholds are used for comparing with the sinusoidal reference based on the total number of voltage levels shown in Table I and II [1]. The darker horizontal lines symbolizes the thresholds at which the bulk inverter changes states when the sinusoidal reference crosses it. When the 2:1 ratio is used, the switching states 2 and 4 are the thresholds for the bulk switching. Both states



a) bulk switching states when $v_{dc} = 2v_{dcx}$.



b) bulk switching states when $v_{dc} = 3v_{dcx}$.

Figure 2. Natural sampling bulk inverter switching states.

has per-phase redundancy as in Table I. Then, for example, to produce the reference value between the 1 and 2, bulk state can stay at 0, while the conditioning state switch at PWM frequency between 1 and 0. There's no PWM frequency switching in the bulk inverter output [5]. For 3:1 voltage ratio, however, there's no per-phase redundancy. So when the reference is between level 2 and level 3, or between level 5 and 6, the bulk state has to switch at PWM frequency between state 0 and 1, or between state 1 and 2, respectively. This is demonstrated in the Figure 2.

Consequently, the natural sampling process on each phase can't strictly split the commanded output into fundamental and PWM frequency switching, when 3:1 dc ratio is used.

Moreover, the RSS process was used in [1] to maintain the conditioning inverter capacitor voltage, and it introduced extra notches at PWM frequency into the bulk inverter phase to ground voltage as shown in Figure 3. Herein, in the vector plot, each switching states of the bulk inverter is labeled. And the areas where the high frequency notches occur are where the sub-hexagons overlap and the vectors in the overlapped region belongs to two or more bulk switching states. The physical implication here is that for any switching states from the modulator output, the way to affect the power

flow into the conditioning inverter is being able to select its equivalent states with the different bulk inverter switching states; otherwise, the conditioning inverter's switching states will be equivalent. As a result, the contribution of the conditioning inverter load voltage v_{as} (3) will stay the same and so will the power flow into the conditioning inverter.

For example, in Figure 3, the sector 1, 2 and 3 in the circular locus of the reference vector correspond to the 1, 2 and 3 sections in the bulk phase to ground voltage output. While in sector 1 and 3, the reference vector locus traverses the areas belonging to two single sub-hexagons with bulk states 201 and 210 separately, so no RSS occurs here and the voltage v_{ag1} remains at state 2. Sector 2 belongs to both sub-hexagons which originate from the bulk switching states 200 and 100 respectively and the RSS process switches v_{ag1} between the state 1 and 2, so high frequency notches are observed.

There's an alternative way of understanding the previous method with RSS process [1]: the bulk inverter phase to ground voltage can be viewed as using 180° VSI with high frequency notches which effectively lowers its fundamental component. Then as the modulation index decreases, more PWM notches are expected. This PWM frequency switching poses detrimental effects in cases where IGCT is used in the construction of the bulk inverter.

IV. PROPOSED CONTROL DESCRIPTION

To solve the problem, the magnitude of its fundamental component can be adjusted by a firing angle α to the bulk inverter 180° VSI, instead of by adding high frequency notches as the results of the previous RSS method. This ensures that the bulk inverter switches only at the fundamental frequency and it basically become the three-level block switching modulation. Since the conditioning inverter has no dc supply, it merely compensates the harmonics in the bulk inverter voltage output and provides no average active power. To output the equivalent load voltage as in [1] with this new joint control method, two questions need to be answered:

1. By directly switching to a new bulk inverter state without PWM switching, is it possible to accurately produce the phase load voltage?
2. Without the RSS process, how to maintain the conditioning inverter capacitor bank voltage?

To answer the first question, it is helpful to go back to Figure 2 and compare the new method with the per-phase natural sampling process. Its failure to provide the distinctive bulk output is due to the fact that the bulk inverter state change results in a bulk voltage change $3E$ (assuming $v_{dc} = 6E$ and $v_{dcx} = 2E$), while the conditioning inverter has the per-phase adjustability of $v_{dcx} = 2E$ at a maximum. There's a gap of $1E$ as shown in Figure 2 that can't be synthesized by the conditioning inverter PWM switching. Here, bulk inverter has to switch back to the previous level to make up the gap.

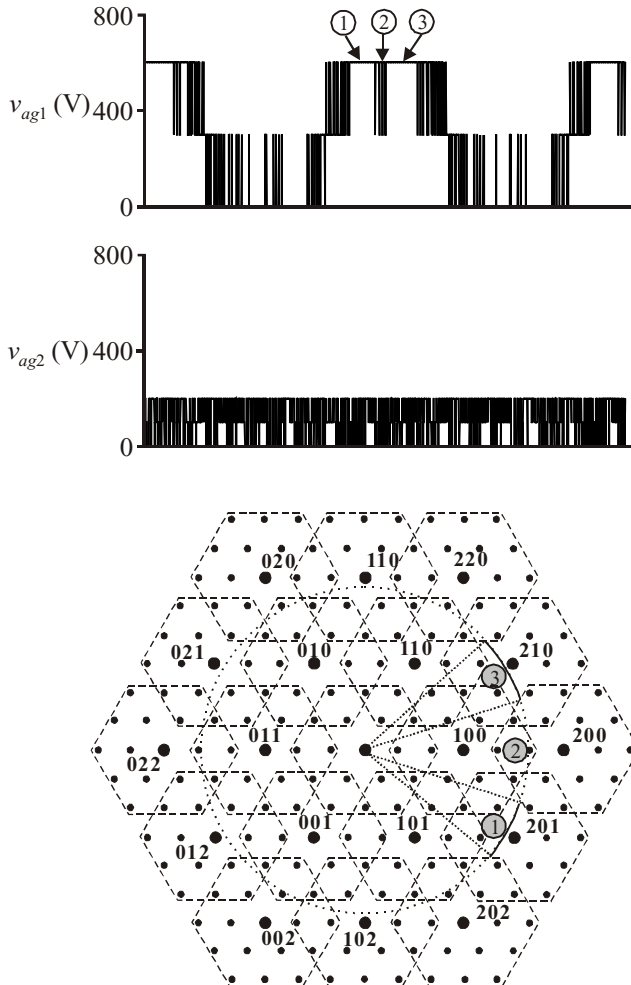


Figure 3. The line-to-ground voltages and vector plot using the RSS method.

Now that with the new joint control method, this type of high frequency switching is not permitted in bulk inverter; however, the state change of the bulk inverter can, in most cases, be compensated by conditioning inverter joint phase switching. This will be explained in the sub-section *A* below. With certain modulation indexes, the joint-phase switching of the conditioning inverter can't compensate the bulk state change at certain regions in one fundamental cycle. In that case the phase voltage can't be accurately produced and these special cases will be discussed in section V.

The conditioning inverter capacitor voltage is maintained by a straightforward PI control with direct control of the active power flow. This will be explained in sub-section *B* below where the algorithm based on the *P-Q* compensation is introduced to compute the conditioning inverter PWM switching state.

A. Bulk Inverter Control

Figure 4 shows the bulk inverter line-to-neutral-point voltages in the time domain when block switching modulation is used. The fundamental voltage amplitude of these voltages is a function of the firing angle α as

$$v_f = \frac{2v_{dc}}{\pi} \cos(\alpha). \quad (4)$$

The nine-level vector plot in Figure 5 provides more insight into the space vector implementation of block switching modulation. The three-level hexagon denoted by heavy dots represents the available switching states of the bulk inverter. For a block switching with α angle between 0° and 30° , the voltage vector traverses the 12 bulk switching states indicated as the perimeter of the outer hexagon by solid line. Different vector traversal routes exist for bulk inverter when its firing angle ranges is from 30° to 60° and from 60° to 90° . They are shown in the same figure as the lighter and the lightest solid

lines respectively. Note that the path for α between 60° and 90° , the bulk inverter follows the bulk switching states on the first level hexagon and it goes back to the origin before switching to the next state.

In Figure 5, along the vector path of the bulk inverter when α is between 0° and 30° , the area formed by all the sub-hexagons (which originate from these bulk switching states) are continuous and overlap. Therefore when the bulk states change to the next state in the path, representing its switching state change at one phase, the conditioning inverter joint-phase PWM switching will be able to synthesize the reference vector.

The bulk voltage stays at each switching state in the path for certain time interval. For a given α angle, there are only two alternate intervals as illustrated in Figure 6, which applies to the case when α is between 0° and 30° . Therein, each switching state is shown along with the time spent at that state. Depending on the α angle, the two time intervals can be calculated as the following equations

For α between 0° and 30° :

$$\begin{aligned} T_1 &= (2 \cdot \alpha) \cdot \frac{T}{360^\circ} \\ T_2 &= (60^\circ - 2 \cdot \alpha) \cdot \frac{T}{360^\circ} \end{aligned} \quad (5)$$

For α between 30° and 60° :

$$\begin{aligned} T_1 &= (120^\circ - 2 \cdot \alpha) \cdot \frac{T}{360^\circ} \\ T_2 &= (2 \cdot \alpha - 60^\circ) \cdot \frac{T}{360^\circ} \end{aligned} \quad (6)$$

For α between 60° and 90° :

$$\begin{aligned} T_1 &= (2 \cdot \alpha - 120^\circ) \cdot \frac{T}{360^\circ} \\ T_2 &= (180^\circ - 2 \cdot \alpha) \cdot \frac{T}{360^\circ} \end{aligned} \quad (7)$$

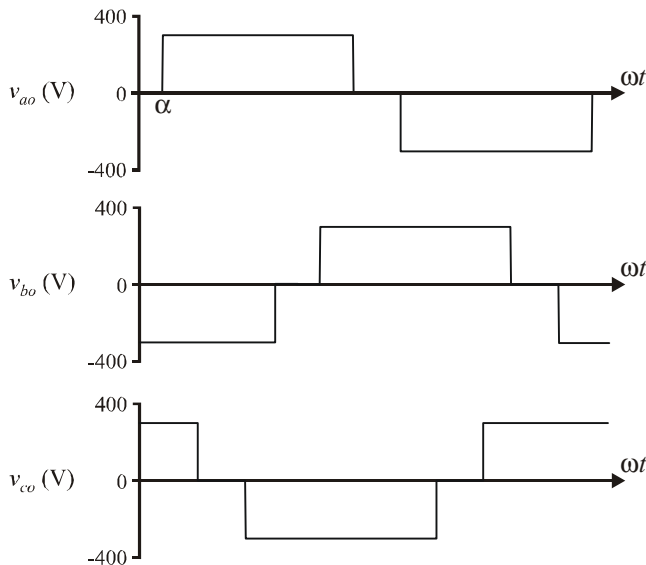


Figure 4. Bulk line-to-neutral-point voltages.

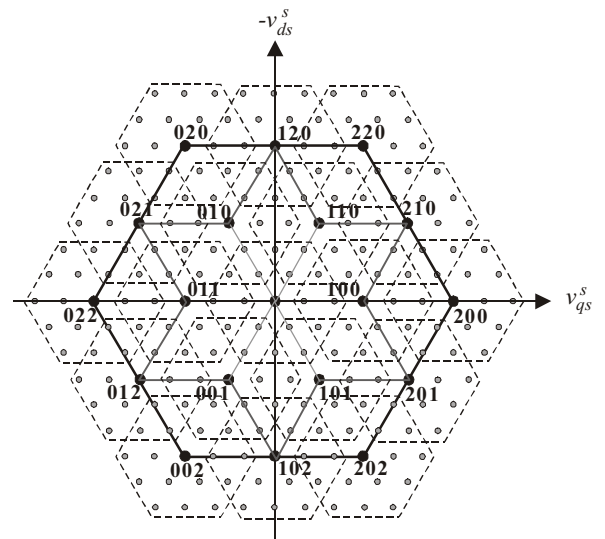


Figure 5. Vector plot of the 3/3 cascaded inverter with bulk inverter vector path.

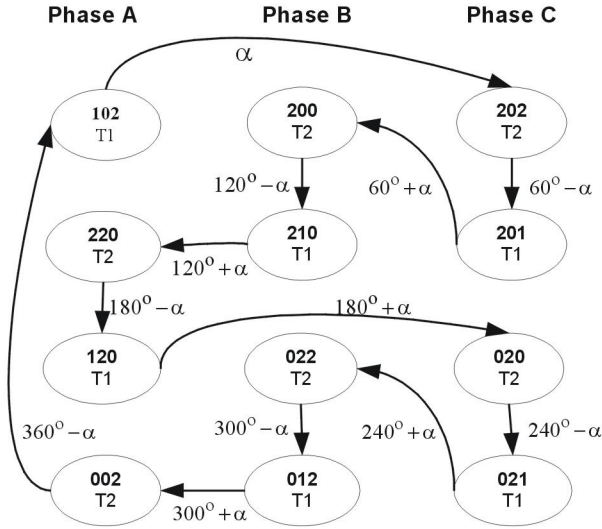


Figure 6. Bulk inverter block switching control state diagram ($0 < \alpha < 30$ degree).

where T represents the one fundamental period. Given any modulation index (i.e. α angle), the DSP controller can easily determine the interval time for each switching state traversed by the bulk inverter voltage. Because of the discrete timing of a DSP implementation, the period of the fundamental output voltage is actually a rounded-off to the nearest multiple of the DSP period. However, the DSP period can be computed and changed on the fly to fit an integer number of periods into each time interval computed ahead of time by (5-7). The timing equations here will also provide important information for analyzing the operating region of the proposed joint control discussed further in the section V.

B. Conditioning Inverter Voltage Control

The same DSP controller which outputs the transistor signals resulting in the bulk voltages of Figure 4 will also output the transistor states of the conditioning inverter. The primary goal of this control is to compensate the voltage harmonics from the bulk inverter. From Figure 4, it can be seen that these harmonics will be large and at low frequencies. A secondary goal of the conditioning inverter

control is to regulate the capacitor voltage v_{dcx} so that it can be supplied by a capacitor source. Both of these objectives are effectively met by using P - Q theory as shown by the control diagram in Figure 7. Therein, the bulk inverter three phase switching state commands is decremented by one and multiplied by half of the bulk dc voltage. The resulting bulk inverter line-to-midpoint voltages and the load currents from two current sensors are then transformed to the stationary reference frame. Using this information, the instantaneous real and reactive powers supplied by the bulk inverter are then calculated according to

$$P = \frac{3}{2} (v_{qs}^s i_{qs}^s + v_{ds}^s i_{ds}^s) \quad (8)$$

$$Q = \frac{3}{2} (v_{qs}^s i_{ds}^s - v_{ds}^s i_{qs}^s) \quad (9)$$

For a system devoid of harmonics, the real and reactive power would be dc quantities (for steady-state operation). To obtain near-ideal values of real and reactive power P - Q , the instantaneous quantities are passed through a low-pass filter (LPF). Note that the dc values will not be attenuated by the LPF and the P - Q value of the bulk inverter fundamental component can be accurately obtained. The difference between the filtered and instantaneous values then produces the commanded real and reactive power for the conditioning inverter P_x^* and Q_x^* . Since the conditioning inverter currents are the same as the bulk inverter, expressions for its commanded stationary reference frame voltages can be obtained by an inverse solution of the real and reactive power equations, leading to

$$v_{qsx}^{s*} = -\frac{2}{3} \left(\frac{P_x^* i_{qs}^s + Q_x^* i_{ds}^s}{i_{qs}^{s2} + i_{ds}^{s2}} \right) \quad (10)$$

$$v_{dsx}^{s*} = -\frac{2}{3} \left(\frac{P_x^* i_{ds}^s - Q_x^* i_{qs}^s}{i_{qs}^{s2} + i_{ds}^{s2}} \right) \quad (11)$$

These voltages are transformed back to a - b - c quantities leading to the voltages v_{asx}^* , v_{bsx}^* , and v_{csx}^* as shown in Figure

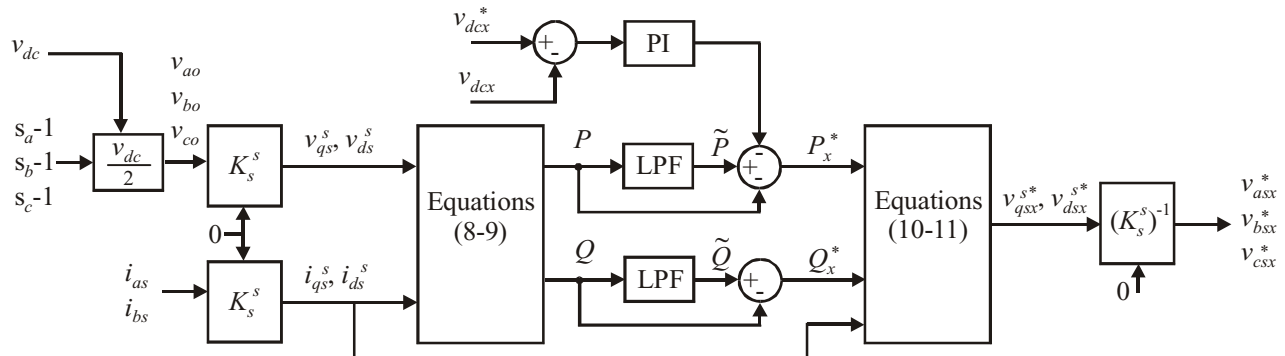


Figure 7. Conditioning inverter P-Q controller block diagram.

7. These voltages can then be normalized to the dc voltage and used as PWM duty cycles [6]. An additional PI control term is included in the commanded power (as shown in the same figure) for the regulation of the conditioning inverter capacitor voltage.

The algorithm based on P - Q theory makes the system P - Q output commands available. So the PI control can directly adjust the active power flow into the conditioning inverter and force zero net real power flow. This is a direct and robust way to regulate the conditioning inverter capacitor bank.

V. OPERATING REGION ISSUES

According to the previous discussion, the time intervals for each bulk switching state in the proposed control can be expressed by (5-7) in terms of α angle. Special cases occur at the $\alpha=0^\circ$, 30° and 60° , at which the bulk inverter time

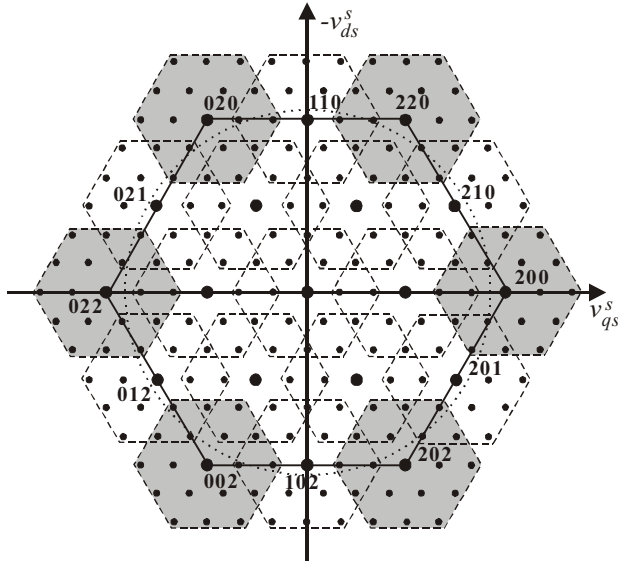


Figure 8. The vector path when $\alpha=0$ degree.

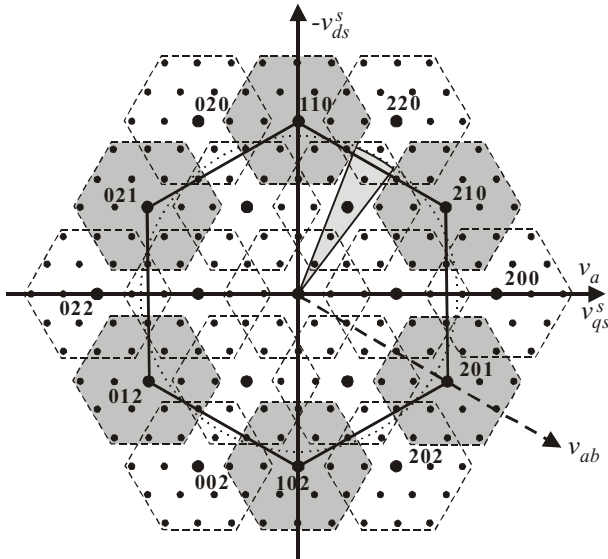


Figure 9. The vector path when $\alpha=30$ degree.

duration on one of every two switching states in the regular path are zero, so the vector path of $\alpha=0^\circ$, 30° and 60° take different patterns and are represented by the solid lines as shown in Figure 8 and 9.

The shaded sub-hexagons in Figures 8 and 9 are the ones originating from the switching states traversed by the bulk inverter when $\alpha=0^\circ$ and 30° , respectively. These shaded areas are where the reference vector can be precisely synthesized by the conditioning inverter PWM switching. And the circular locus of the dotted line is the reference vector path at that α angle. Obviously, there are gaps between the shaded areas, and the combined load voltage vector has to jump over the gap right into the next closest sub-hexagon in the CCW direction. This leads to a failure to produce continuous phase voltage at certain regions as will be demonstrated in the simulations. When $\alpha=60^\circ$, there's no gap between the sub-hexagons in its vector path, hence, no performance deterioration is expected here.

When α angle is close to but not exactly at 0° and 30° , the bulk inverter vector path appears to be regular and have a continuous "synthesizable path" for the reference vector, i.e. no gap between the sub-hexagons in the bulk vector path; however, the duration at one of every two bulk inverter switching states is too short for the reference vector to go at the fundamental velocity through the hexagonal region solely owned by that bulk states. For example, in Figure 9, the shaded sector is the path through the region owned by bulk states 220. If α angle is close to 30° , the residing time on 220 states (as calculated by (5,6)) could be less than what it takes to go through the sector. In this case, the discrete leap in phase voltage still exists.

For valid output in the whole fundamental cycle, the firing angle should avoid the proximity of the 0° and 30° by a few degrees. By geometric computation and with (5-6), the firing angle ranges to avoid are ideally $[0^\circ, 10^\circ]$ and $[22^\circ, 38^\circ]$. Beyond these ranges, there's no degradation of performance. In practice, avoiding the narrower ranges $[0^\circ, 6^\circ]$ and $[24^\circ, 36^\circ]$ will still give satisfactory performance while it's not ideal.

VI. SIMULATION RESULTS

The proposed control was verified by simulation of the cascade-3/3 inverter. The bulk inverter dc supply is 600V and the firing angle was set to $\alpha=18^\circ$, 30° , and 45° . The conditioning inverter capacitor bank voltage is maintained at 200V by the PI control. The motor was emulated by a three-phase R-L load with $R=2\Omega$ and $L=2.9\text{mH}$. Figure 10 shows the simulation results when $\alpha=18^\circ$. Therein, the bulk and conditioning inverter voltages line-to-ground are shown on the left side as well as the conditioning inverter capacitor voltage. It can be seen that the bulk inverter operates with block switching output without narrow pulses. The capacitor voltage is regulated around 200V with some ripple which comes about since a heavy load was used to test the robustness of the control. However, the ripple will not affect the output voltage because this term is compensated in the PWM [6]. The load voltage, line-to-line voltage and load

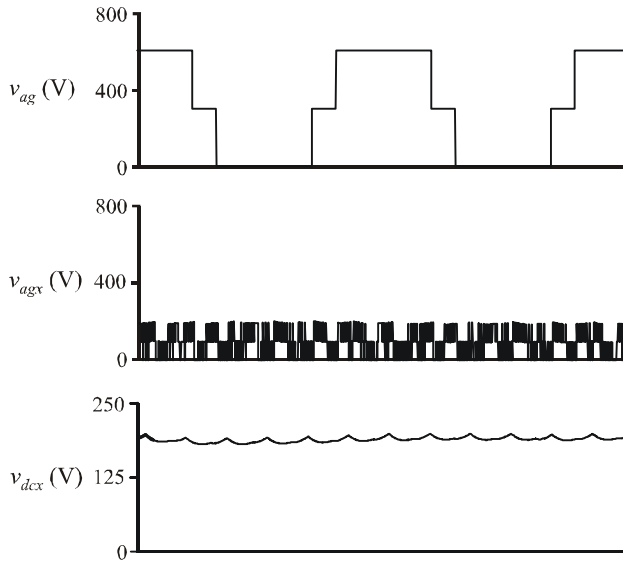


Figure 10. Cascade-3/3 inverter simulation results when $\alpha=18$ degree.

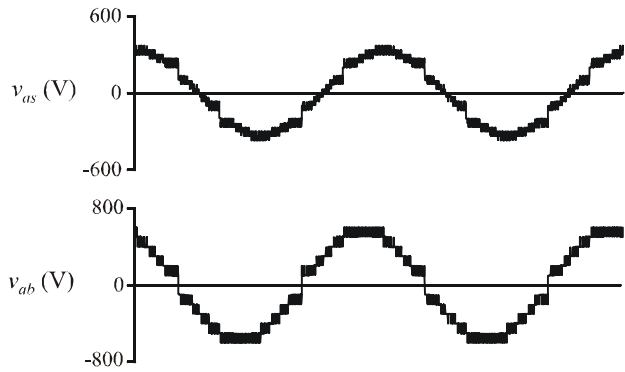
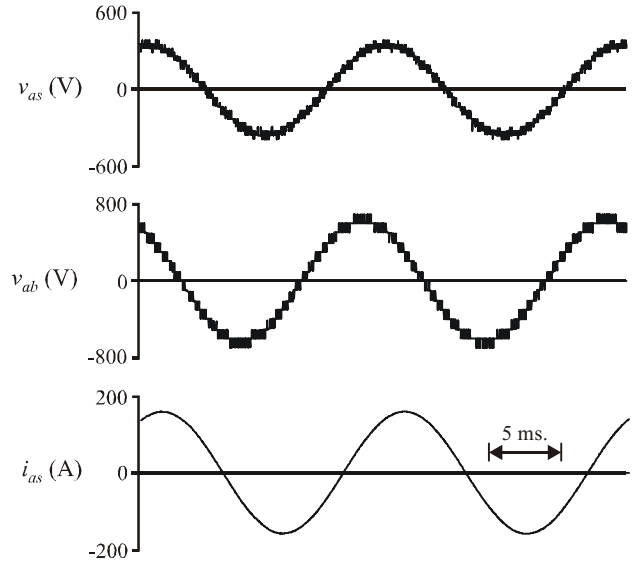


Figure 11. Simulation results when $\alpha=30$ degree.

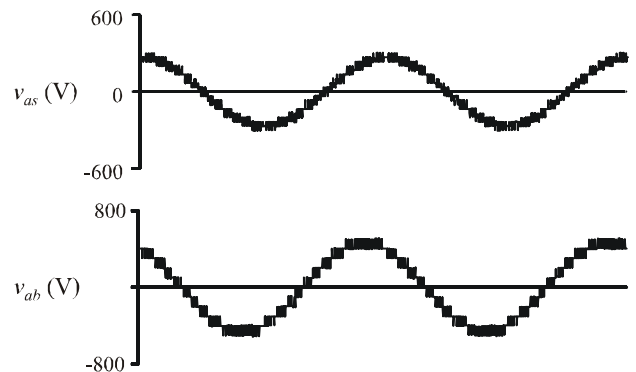


Figure 12. Simulation results when $\alpha=45$ degree.

currents are shown on the right side of Figure 10. The effective line-to-line voltage in this case is $v_{ab} = v_{as} - v_{bs}$ and can be seen to have fifteen distinct levels which is characteristic of eight-level inverter performance.

For $\alpha=30^\circ$, 45° , the load voltage, and line-to-line voltages are plotted in Figures 11 and 12. In Figure 12, when $\alpha=45^\circ$, the modulation index is lower than $\alpha=18^\circ$, and as can be verified by eleven line-to-line voltage levels (six-level performance). Interesting observations can be made at firing angle $\alpha=30^\circ$. The performance degradation happens around the phase angle 30° (not the firing angle) as validated from the vector plot in Figure 9. This sudden leap in the phase voltage can be explained with the gap between the two neighboring sub-hexagons at exactly 30° in the vector plot (where the q -axis/ a -axis represents 90° in phase angle). However, no obvious performance deterioration observed around phase angle 90° . That's because the proximity of 90° of a sinusoidal waveform is quite smooth, so the leap in value is not as noticeable as when it is 30° . Moreover, for v_{ab} , the voltage discontinuity occurs around zero degrees which

matches the existence of the gap around 0° degree phase angle in v_{ab} .

VI. CONCLUSION

This paper presents a new type of control method for the cascaded multilevel inverter (wherein two three-phase three-level inverters are connected in series through the load). The control avoids the high frequency switching (narrow pulses) in the bulk-power inverter, and outputs the precise fundamental frequency. An advanced modulation method based on P - Q compensation is developed for the control of the conditioning inverter, which successfully maintains the capacitor voltage so that only one dc source is needed for the cascaded multilevel drive. Simulation results demonstrate the effectiveness of the proposed control. Laboratory validation is on-going.

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Shuai Lu received BSEE degree from the Chongqing University, China in 1997; and the MSEE degree from the University of Wisconsin - Milwaukee in 2003 and is now pursuing a Ph.D. degree at the University of Missouri - Rolla. His research specialty is power electronics and machine drives. Contact: sl4xf@umr.edu.

Keith A. Corzine received the BSEE, MSEE, and Ph.D. degrees from the University of Missouri - Rolla in 1992, 1994, and 1997 respectively. He taught at the University of Wisconsin - Milwaukee from 1997 to 2004 and is now an Associate Professor at the University of Missouri - Rolla. His research interests include power electronics, motor drives, Naval ship propulsion systems, and electric machinery analysis. Contact: Keith@Corzine.net.

Tom H. Fikse received BSME degree from the Pennsylvania State University and has completed over 50 credits of advanced education from the same institution. Mr. Fikse has over twenty years of experience working on diverse NSWCCD projects ranging from air masking systems, novel electromagnetic devices, applied superconductivity to advanced power electronics. For the last six years, Mr. Fikse has concentrated on motor drives and power converters associated with Integrated Power Systems research & development.