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Shuai Lu

Keith Corzine
Missouri University of Science and Technology

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Advanced Control and Analysis of Cascaded Multilevel Converters Based on P-Q Compensation

Shuai Lu, *Student Member, IEEE*, and Keith A. Corzine, *Senior Member, IEEE*

***Abstract*—This paper introduces new controls for the cascaded multilevel power converter. This converter is also sometimes referred to as a "hybrid converter" since it splits high-voltage/low-frequency and low-voltage/pulsewidth-modulation (PWM)-frequency power production between "bulk" and "conditioning" converters respectively. Cascaded multilevel converters achieve higher power quality with a given switch count when compared to traditional multilevel converters. This is a particularly favorable option for high power and high performance applications such as Naval ship propulsion. This paper first presents a new control method for the topology using three-level bulk and conditioning inverters connected in series through a three-phase load. This control avoids PWM frequency switching in the bulk inverter. The conditioning inverter uses a capacitor source and its control is based on compensating the real and reactive (P-Q) power difference between the bulk inverter and the load. The new control explicitly commands power into the conditioning inverter so that its capacitor voltage remains constant. A unique space vector analysis of hybrid converter modulation is introduced to quantitatively determine operating limitations. The conclusion is then generalized for all types of controls of the hybrid multilevel converters (involving three-level converter cells). The proposed control methods and analytical conclusions are verified by simulation and laboratory measurements.**

***Index Terms*—AC motor drives, DC–AC power conversion, pulsewidth-modulated inverters.**

I. Introduction

THERE ARE several major topologies of cascaded multilevel converters (hybrid converters), such as the cascaded H-bridge [1]–[5], cascaded multilevel converters through split neutral load [6]–[10], and the three-level diode-clamped inverter in series with H-bridge inverters (DCH) [11]–[13]. The controls for various topologies can be used interchangeably with minor modification. So far, the most practical cascading scheme is to use two three-level inverters. When a 3:1 dc voltage ratio (maximal distension) is used, its output is equivalent to a nine-level inverter [6]. The different inverter dc voltages also result in a natural split of fundamental and pulsewidth-modulation (PWM) frequencies between the higher-voltage "bulk" inverter and a lower-voltage "conditioning" inverter using natural sampling modulation [6], [11]–[15] or its variants. Therefore, in medium-voltage applications, it is desirable to use integrated gate-commutated thyristors (IGCTs) and insulated-gate bipolar transistors (IGBTs) as the switches for the bulk and conditioning inverters, respectively. However, when the inverter dc voltage ratio is set at 3:1, the natural sample modulator per-phase needs certain PWM frequency switching in the bulk inverter. This causes unacceptable stress on its IGCT switches [16], [17]. Therefore, even the PWM frequency in the IGBT-based conditioning inverter has to be lowered. Additionally, for applications requiring a simple dc front end, such as Naval ship propulsion, the use of a single dc voltage source is preferred, so one inverter is supplied by a purely capacitive source. This was demonstrated in previous research by properly selecting the converters redundant switching states (RSS) [6], or explicitly adjusting the common mode [11]. In essence, both methods swap the bulk inverter switching states in every PWM cycle, which then introduces extra PWM frequency switching into the bulk inverter.

This paper presents new research in the control of the cascaded multilevel inverter where two multilevel inverters are connected in series by splitting the neutral point of the three-phase load. This topology is an attractive option for Naval ship propulsion drives because of its inherent redundancy [6]. The new control eliminates PWM switching in the bulk inverter while the conditioning inverter capacitors are regulated at the commanded voltage without the need for a real-power dc source. The converter ideal operation limitations are systematically explored and quantitatively defined according their dc voltage ratio and the availability of the conditioning inverter dc sources. Multiple solutions are then given to solve the performance degradation problem. The proposed control and analytical methodology can be easily adapted to all other types of cascaded (hybrid) multilevel converter topologies.

Section II of this paper briefly reviews the topology of the cascade-3/3 multilevel converter. Section III explains the causes of bulk inverter PWM switching. Section IV presents the new control method, where the switching states of the bulk inverter follow certain space vector patterns at the fundamental frequency; while the conditioning inverter control is based on real and reactive power compensation (P-Q theory), which is a robust way of regulating the conditioning inverter capacitor voltage by simply adding a control term to the real power. A detailed analysis of the cascaded/hybrid converter operating regions is presented in Section V. Next, Section VI provides comprehensive solutions to fully utilize the performance potentials of the proposed control set. Finally, experimental results are shown in Section VII.

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The authors are with the Department of Electrical and Computer Engineering, University of Missouri–Rolla, Rolla, MO 65409-0040 USA (e-mail: SL4xf@umr.edu; Keith@Corzine.net).

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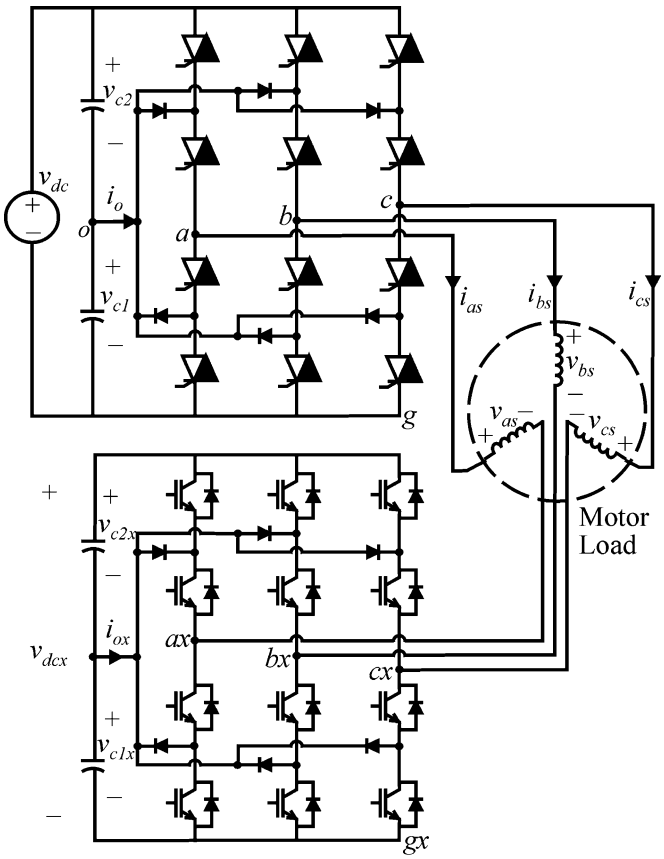

Fig. 1. Cascade-3/3 multilevel inverter.

II. Cascade-3/3 Inverter Topology

Fig. 1 shows the topology of the cascade-3/3 converter. Therein, a three-level "bulk" inverter supplies a motor load from the dc source $v_{\rm dc}$. The neutral point of the machine is opened up and the other ends of the three phases are connected to another three-level "conditioning" inverter. Previous research has shown that this inverter is able to operate with nine-level performance if the voltage ratio is set to $v_{\rm dc} = 3v_{{\rm dc}x}$ [6]. For applications where a singe dc source is preferred, a capacitor supplies the conditioning inverter dc-link voltage $v_{{\rm dc}x}$ and its value is regulated using the control [6]. For this system, the line-to-ground voltages of the bulk and conditioning inverters are computed as a function of the switching states by

$$\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} = \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} \frac{v_{\rm dc}}{2} \tag{1}$$

$$\begin{bmatrix} v_{agx} \\ v_{bgx} \\ v_{cgx} \end{bmatrix} = \begin{bmatrix} s_{ax} \\ s_{bx} \\ s_{cx} \end{bmatrix} \frac{v_{{\rm dc}x}}{2} \tag{2}$$

respectively. In (1) and (2), s_a, s_b, and s_c are the switching states of the bulk inverter and may take on values of 0, 1, or 2 as described in [6]. Likewise, these are the switching states of the conditioning inverter. It is also assumed in (1) and (2) that the capacitors of each inverter are charged to one-half of the total dc voltage for that inverter. This condition is easily realized in the three-level inverter system. The motor load phase voltages can be calculated from the line-to-ground voltages using

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} - v_{agx} \\ v_{bg} - v_{bgx} \\ v_{cg} - v_{cgx} \end{bmatrix}. \tag{3}$$

Equations (1)–(3) allow the calculation of the load voltages given the dc voltages and switching states of the controller.

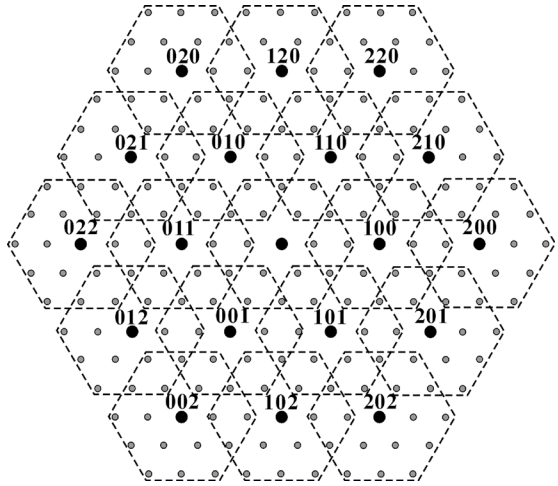

Fig. 2. Cascaded 3/3 inverter voltage vector plot.

TABLE I
Inverters Switching States ($v_{\rm dc} = 2\,v_{{\rm dc}x}$)

s	0	1	2		3	4		5	6
s_a	0	0	0	1	1	1	2	2	2
s_{ax}	2	1	0	2	1	0	2	1	0

The cascade-3/3 inverter voltage vector plot is given in Fig. 2. Each vector dot represents one or more inverter switching states plotted in the stationary $q-d$ reference frame [6], [7], [13]. This vector plot is valuable for visualization and analysis of cascaded inverters and will be used intensively in this paper. The three-layer hexagon pattern denoted by the heavier dots represents the switching states of the bulk inverter, and are named "bulk vectors" hereafter. Each bulk vector is the origin of the smaller three-layer vector patterns enclosed by the dotted subhexagons. These vectors represent the full enumeration of the conditioning inverter switching states. At the 3:1 dc voltage ratio, the size of the subhexagon is exactly 1/3 of the bulk vectors hexagonal pattern.

III. Previous Controls Using Natural Sampling

When the inverter dc voltage ratio is at 3:1, natural sampling modulation using multiple carriers (sine-triangle or duty cycle modulation [14], [15]) cannot produce the bulk inverter switching purely at the fundamental frequency [6], [11], [12]. For the a-phase, this modulation scheme first generates a switching state s according to the reference. The results are then mapped into the a-phase switching states s_a, and s_{ax} of the bulk and conditioning inverters. The mapping Tables I and II are used when the dc ratios are 2:1 and 3:1, respectively.

TABLE II
INVERTERS SWITCHING STATES ($v_{\rm dc} = 3v_{{\rm dc}x}$)

s	0	1	2	3	4	5	6	7	8
s_a	0			1			2		
s_{ax}	2	1	0	2	1	0	2	1	0

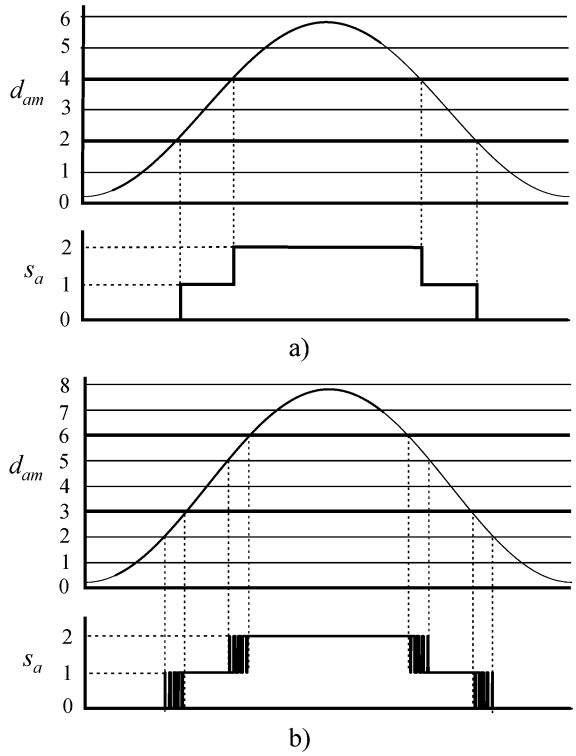

Fig. 3. Bulk inverter switching states from the natural sampling modulator.

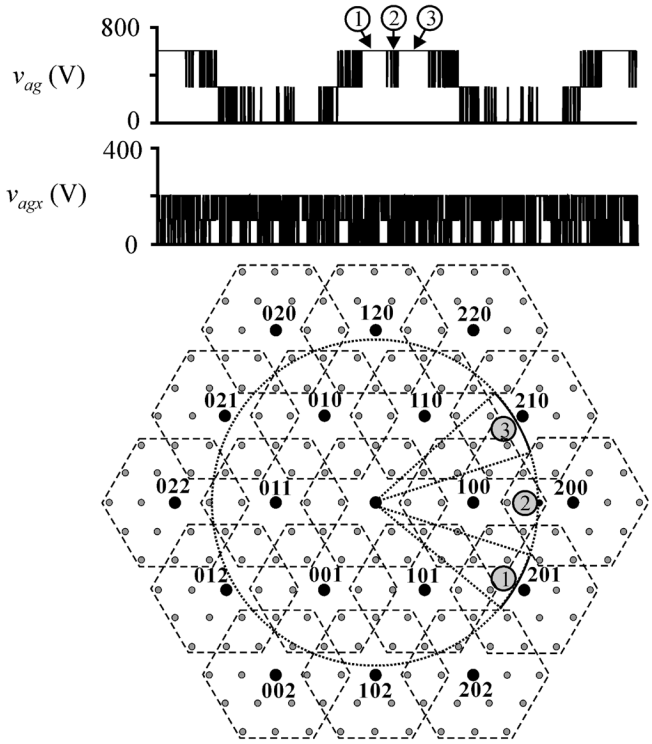

Fig. 4. Line-to-ground voltages and the vector plot using the redundant states selection.

Fig. 3 shows the bulk inverter a-phase switching states resulting from the natural sampling process. The reference is compared with seven and nine evenly spaced thresholds representing the total number of voltage levels at dc ratios of 2:1 and 3:1, respectively. The thicker horizontal lines represent the boundaries where the bulk inverter changes states. At the 2:1 ratio, levels 2 and 4 are such boundaries. Since both states have per-phase redundancy (as seen in Table I) then, for example, to produce the reference between levels 1 and 2, the bulk inverter can stay at state 0, while the conditioning inverter switches between 1 and 0 at the PWM frequency. Hence, there is no PWM frequency switching in the bulk inverter. For the 3:1 voltage ratio, however, no per-phase redundancy exists. So as in Fig. 3, when the reference is between levels 2 and 3, or levels 5 and 6, the bulk inverter has to switch between state 0 and 1, or state 1 and 2 at the PWM frequency.

Moreover, the RSS process was used in [6] to regulate the conditioning inverter capacitor voltage $v_{{\rm dc}x}$. It introduces additional notches at the PWM frequency into the bulk inverter line-to-ground voltage v_{ag} as shown in Fig. 4. The regions where the high-frequency notches occur in v_{ag} corresponds to where the subhexagons overlap in the space vector illustration. The vector dots in the overlapped region belong to two or more bulk vectors and each vector dot has several redundant switching states. So by properly swapping between these states, the three-phase load voltages (v_{as}, v_{bs} and v_{cs}) remain the same, while the bulk inverter switching states are changed. This process affects the net power flow into the conditioning inverter and regulates $v_{{\rm dc}x}$. For example, in Fig. 4, sectors 1, 2, and 3 along the circular locus of the reference correspond to the sections labeled 1, 2, and 3 in v_{ag}. While in sectors 1 and 3, the reference locus traversed the two single subhexagons belonging to the bulk vector 201 and 210 separately. Therefore, no RSS occurs here and v_{ag} remains at state 2. However, Section 2 belongs to both subhexagons of the bulk vector 200 and 100. The RSS process results in switching between these two bulk vectors and accordingly v_{ag} switches between state 1 and 2 in the time domain.

When the common-mode reference adjustment [11] is used to regulate the conditioning inverter capacitor voltages, it implicitly results in fast swapping of the bulk vectors and extra PWM frequency switching in the bulk inverter. The PWM frequency switching poses detrimental effects to the IGCTs used in the bulk inverter. For the previous methods [6], [11], [12] based on natural sampling [14], [15], this problem is particularly acute at low modulation indices. Consider that the conditioning inverter has no real power dc supply; the magnitude of the output voltage has to be equal to the fundamental component of the bulk inverter output. Therefore, the PWM frequency notches in the bulk inverter line-to-ground voltages are a mechanism to effectively lower its fundamental value or the output modulation index (m-index). As the m-index decreases, more PWM frequency notches are experienced.

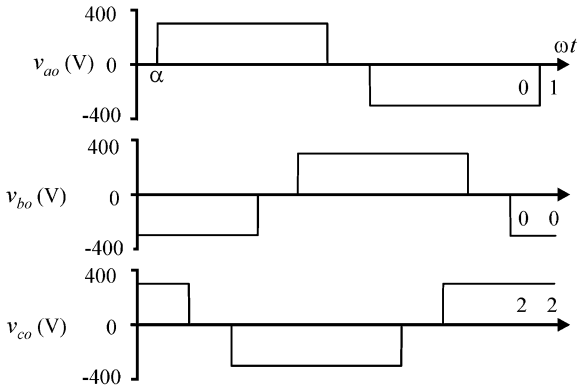

Fig. 5. Bulk inverter line-to-neutral-point voltages.

IV. Proposed Control Method

When the bulk inverter is commanded to switch only at the fundamental frequency, it outputs three-level staircase waveforms as shown in Fig. 5. The bulk inverter fundamental value is adjusted by a firing angle α, instead of by adding PWM frequency notches as previously done. The following two questions arise with this new control scheme.

1) Without PWM switching in the bulk inverter, is it still possible to accurately synthesize the output voltage reference?
2) Without dynamic bulk vector swapping, how can a stable $v_{\mathrm{dc}x}$ be maintained?

To answer the first question, it is helpful to revisit the example at a 3:1 ratio in Fig. 3. When the a-phase reference is between levels 2 and 3, or between levels 5 and 6, if the bulk inverter is not allowed to switch between the state 0 and 1, or state 1 and 2 in every PWM cycle, the resulting a-phase line-to-ground voltage will not correctly synthesize the reference. However, according to (3), the effective phase voltage on the load is not just determined by the output of one phase. Using the proper outputs from the other two phases of the conditioning inverter, the phase voltages on the load can still correctly trace the three-phase references, even though the line-to-ground voltage will no longer conform to the references.

When examined in the $q-d$ vector space, this bulk inverter PWM elimination scheme becomes straightforward as in Fig. 6. For clarity, only three subhexagons are shown. After conversion to $q-d$ space, the three-phase references become a reference vector v_{ref} rotating along a circular locus. As v_{ref} goes through the overlap region between 002 and 102 subhexagons, the bulk vector changes from 002 to 102, and the bulk inverter a-phase changes from state 0 to 1. Since v_{ref} resides in both subhexagons, it can be synthesized by the conditioning inverter PWM while the bulk vector is fixed at 002 and 102, before and after the state change on phase a. Therefore, the bulk inverter PWM switching is not necessary for accurately synthesizing the modulator references.

The relative location of v_{ref} within the subhexagon serves as the output reference for the conditioning inverter, which then produces the PWM output with regular three-level modulation methods [14], [15]. As it is also necessary to achieve zero net power into the conditioning inverter, the reference for the conditioning inverter is not obtained by vector subtraction, but indirectly by P-Q compensation. The voltage $v_{\mathrm{dc}x}$ is maintained by a straightforward PI controller with direct adjustment of the active power. This control provides the answer to the second question and is detailed in subsection B.

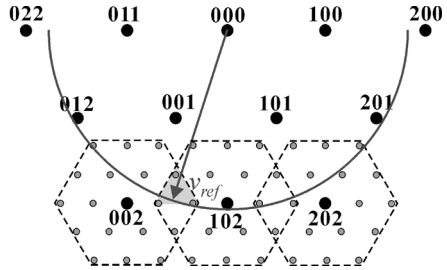

Fig. 6. Visualization of the new modulation method at $\alpha = 10°$.

A. Bulk Inverter Control

Fig. 5 shows the staircase waveforms of the bulk inverter line-to-midpoint voltages. Their fundamental voltage amplitude is a function of the firing angle α given by

$$v_f = \frac{2v_{\mathrm{dc}}}{\pi}\cos(\alpha). \tag{4}$$

When the conditioning inverter does not have a real-power dc source, it only supplies reactive power, and the bulk inverter fundamental has to be equal to the output voltage magnitude. For better understanding and analysis of the cascaded (hybrid) multilevel inverter control, this paper introduces a unique space vector perspective into the bulk inverter fundamental frequency switching scheme as described.

When the α angle is in the range of [0°, 30°], [30°, 60°], and [60°, 90°], the bulk inverter output in $q-d$ space will traverse 12 bulk vectors in one fundamental cycle with three different sequences or patterns as in Fig. 7 and Tables III–V.

Each bulk vector (switching state) in the sequence has a certain amount of time duration. For any given α angle or m-index, there are only two alternate time durations as formulated by (5)–(7). Tables III– V show the timing assignment on each bulk vector in the sequence. When α is exactly 0°, 30°, and 60°, one time duration becomes zero; hence, only six bulk vectors are used in the sequence with each vector having a time duration of 1/6 of one period.

For α between 0° and 30°

$$\mathrm{T}_1 = (2\cdot\alpha)\cdot\frac{\mathrm{T}}{360°}$$
$$\mathrm{T}_2 = (60° - 2\cdot\alpha)\cdot\frac{\mathrm{T}}{360°}. \tag{5}$$

For α between 30° and 60°

$$\mathrm{T}_1 = (120° - 2\cdot\alpha)\cdot\frac{\mathrm{T}}{360°}$$
$$\mathrm{T}_2 = (2\cdot\alpha - 60°)\cdot\frac{\mathrm{T}}{360°}. \tag{6}$$

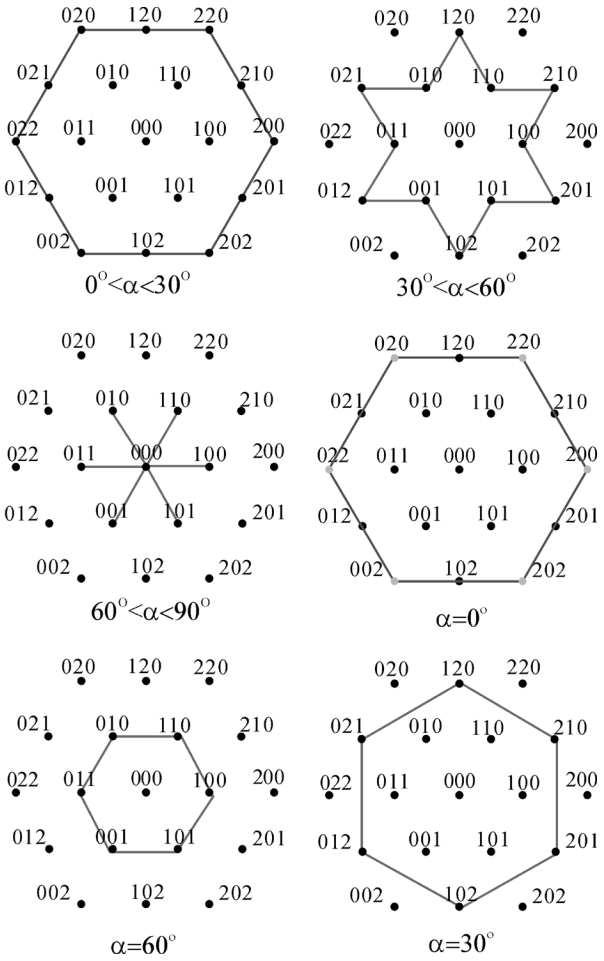

Fig. 7. Bulk vector traversal patterns at various α angles.

TABLE III
BULK VECTOR SEQUENCE/TIMING WHEN $\alpha = [0°, 30°]$

200	210	220	120	020	021	022	012	002	102	202	201
T2	T1	T2	T1	T2	T1	T2	T1	T2	T1	T2	T1

TABLE IV
BULK VECTOR SEQUENCE/TIMING AT $\alpha = [30°, 60°]$

100	210	110	120	010	021	011	012	001	102	101	201
T2	T1	T2	T1	T2	T1	T2	T1	T2	T1	T2	T1

TABLE V
BULK VECTOR SEQUENCE/TIMING AT $\alpha = [60°, 90°]$

000	100	000	110	000	010	000	011	000	001	000	101
T1	T2	T1	T2	T1	T2	T1	T2	T1	T2	T1	T2

For α between 60° and 90°

$$\mathrm{T}_1 = (2 \cdot \alpha - 120°) \cdot \frac{\mathrm{T}}{360°}$$
$$\mathrm{T}_2 = (180° - 2 \cdot \alpha) \cdot \frac{\mathrm{T}}{360°} \tag{7}$$

where T represents the one fundamental cycle period.

The common physical implication of (5)–(7) is that when the m-index is higher (smaller α angle), the bulk vectors with the larger magnitudes will have longer time durations and vice versa. The bulk vector timing analysis above provides the basis to study the operating ranges of all types of cascaded multilevel converters controls, including the control being introduced in this paper.

B. Conditioning Inverter Control

The primary goal of the conditioning inverter control is to compensate the low-order harmonic active and reactive power from the bulk inverter. A secondary goal is to regulate the voltage $v_{\mathrm{dc}x}$ so that it can be supplied by a capacitor source. Both of these objectives are effectively met by using the proposed P-Q compensation as shown in Fig. 8. Therein, the bulk inverter three-phase switching state commands are used to determine the bulk line-to-midpoint voltages. The resulting voltages and the load currents from two current sensors are then transformed to the stationary reference frame. Using this information, the instantaneous real and reactive powers supplied by the bulk inverter are calculated according to

$$P = \frac{3}{2}\left(v_{qs}^{s} i_{qs}^{s} + v_{ds}^{s} i_{ds}^{s}\right) \tag{8}$$
$$Q = \frac{3}{2}\left(v_{qs}^{s} i_{ds}^{s} - v_{ds}^{s} i_{qs}^{s}\right). \tag{9}$$

For a system devoid of harmonics, the real and reactive power P-Q would be dc quantities (in steady state). By passing the instantaneous quantities through low-pass filters (LPFs), the P-Q dc values of the bulk inverter can be accurately extracted without filter attenuation. The difference between the filtered and instantaneous P-Q values represents the compensation power output P_x^* and Q_x^* from the conditioning inverter. Expressions for the conditioning inverter reference voltages are obtained by an inverse solution of the real and reactive power (8)–(9) in a stationary frame, leading to

$$v_{qsx}^{s*} = -\frac{2}{3}\left(\frac{P_x^* i_{qs}^{s} + Q_x^* i_{ds}^{s}}{i_{qs}^{s2} + i_{ds}^{s2}}\right) \tag{10}$$
$$v_{dsx}^{s*} = -\frac{2}{3}\left(\frac{P_x^* i_{ds}^{s} - Q_x^* i_{qs}^{s}}{i_{qs}^{s2} + i_{ds}^{s2}}\right). \tag{11}$$

Note that the negative signs in (10) and (11) are present because the output currents from the conditioning inverter are in the opposite direction of the load currents. The reference voltages are then transformed back to $a - b - c$ quantities as v_{asx}^*, v_{bsx}^*, and v_{csx}^*, which are further normalized into PWM duty cycles in the voltage levels [14].

An additional PI control term is included in the commanded real power (Fig. 8) for regulating $v_{\mathrm{dc}x}$. The algorithm based on P-Q compensation makes the system P-Q output directly controllable, so the PI control can force zero real power flow into the conditioning inverter. This offers a direct and robust way to regulate the conditioning inverter capacitor voltage. Finally, to equally split the voltage $v_{\mathrm{dc}x}$ between the upper and lower capacitors, an RSS method [6] for the three-level diode-clamped inverter is used.

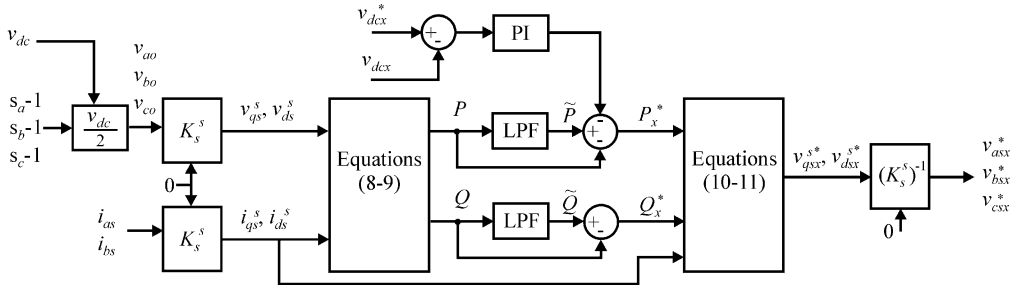

Fig. 8. Conditioning inverter P-Q controller block diagram.

V. Comprehensive Converter Operating Range Analysis

The space vector analysis in [13] defines the "modulation domain" as the area covered by the subhexagons of all the bulk vectors. In this domain, the PWM modulator works properly. Herein, cascaded-3/3 topology with a 3:1 ratio also has all of its subhexagons overlap and does not leaves any "holes" [13] in the resulting hexagonal region as in Fig. 2. However, in this work, it is discovered that when the bulk inverter fundamental switching and power/capacitor voltage regulation are to be satisfied, the PWM "modularity" is not just an issue of whether the subhexagons can cover the path of the reference vector $v_{\rm ref}$. The power/capacitor-voltage regulation requires the bulk inverter output fundamental magnitude to be equal to the combined output, which then dictates the sequence and time assignment to bulk vectors as analyzed in Section IV-A. When the time on a certain bulk vector is less than what is needed for the $v_{\rm ref}$ vector to go through its affiliated subhexagon, it causes the "out of range" (performance degradation) problem, and $v_{\rm ref}$ cannot be accurately synthesized. This undesirable situation is caused by the following two factors combined together.

The first factor is the limited flexibility in its bulk vector traversal sequences and timing due to the lack of real-power dc source in the conditioning inverter. Second, at a 3:1 dc voltage ratio $v_{{\rm dc}x}$, the size of the subhexagons is small. Therefore, in some m-index ranges, it is possible to have the rotating reference vector outside the range of the conditioning inverter. This section theoretically analyzes the causes of this "out of range" problem and quantitatively defines the m-index ranges with performance degradation, which applies to all types of controls of the cascade-3/3 (hybrid) multilevel inverter, as long as the 3:1 dc ratio and the capacitive dc-source in the conditioning inverter [6], [11]–[12] are used simultaneously. Comprehensive solutions are then proposed in the subsequent Section VI to address the problem and achieve ideal converter performance.

A. Operating Ranges for the Proposed Control

As given by (5)–(7), when $\alpha = 0°$, 30°, and 60°, the time interval on one of every two bulk vectors in the traversal path becomes zero, so that the vector path with $\alpha = 0°$, 30°, and 60° uses only six bulk vectors per cycle. Figs. 9 and 10 show the shaded subhexagons with their origins at the six bulk vectors along the path when $\alpha = 0°$ and 30°, respectively. The reference vector within the shaded areas can be precisely synthesized by the conditioning inverter PWM switching. However, the locus of the reference vector in Figs. 9 and 10 has gaps in between the shaded areas, and the resulting load voltage vector has to jump over the gap into the next closest subhexagon in the counterclockwise direction. This fails to produce a continuous phase voltage at certain regions as demonstrated by the simulation waveforms in Fig. 11.

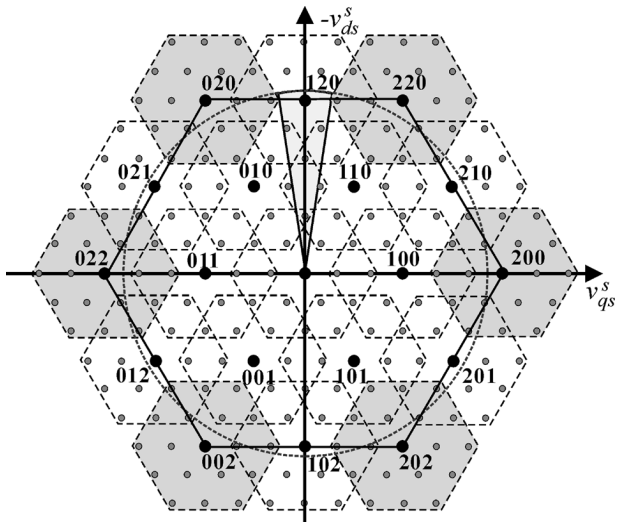

Fig. 9. Performance degradation when $\alpha = 0°$.

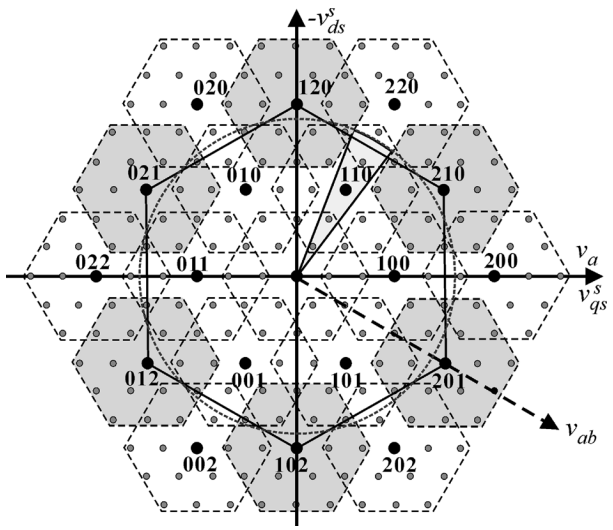

Fig. 10. Performance degradation when $\alpha = 30°$.

When α is close but not equal to 0° and 30°, 12 bulk vectors are to be used as shown in Fig. 7. There does not appear to

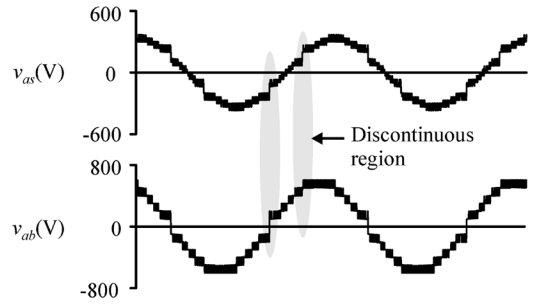

Fig. 11. Simulation results when $\alpha = 30°$.

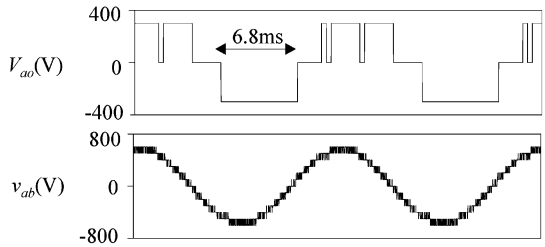

Fig. 12. Modified bulk inverter fundamental switching scheme.

be gaps between all 12 subhexagons along the reference vector locus. However, the time duration on one of every two bulk vectors is too short for $v_{\rm ref}$ (at the fundamental frequency) to go through the subhexagon region solely owned by that bulk vector. For example, the highlighted sector in Fig. 9 shows the $v_{\rm ref}$ locus through the region owned by the bulk vector 220. When α is close to 30°, the time duration on vector 220 given by (5) and (6) could be less than what it takes $v_{\rm ref}$ to go through the sector with the fundamental frequency. Therefore, the discrete leap in phase voltages still exists.

By geometric computation, together with timing (5) and (6), the problematic α ranges in the proximity of $\alpha = 0°$, and $\alpha = 30°$ is calculated to be [0°, 10°] and [22°, 38°]. The bulk inverter fundamental switching pattern can be modified to avoid the performance degradation when α is around 30°. According to (5), the time durations on vectors with the largest magnitudes (at the vertex of the hexagon path, such as 220) approach zero, when the m-index decreases and α approaches 30°. However, by assigning part of the time duration on 220 (magnitude of 2/3 $v_{\rm dc}$) to vector 110 (small magnitude of 1/3 $v_{\rm dc}$), the m-index can also be decreased. Meanwhile, the total time on 220 and 110 remains long enough for the $v_{\rm ref}$ to go through the highlighted sector in Fig. 10. Note that this sector is completely covered by the overlapped area of two subhexagons of 220 and 110. Simulation results are shown in Fig. 12. The bulk inverter output is no longer a pure staircase. However, it still avoids the PWM frequency switching in the bulk inverter and produces the continuous v_{ab} waveform when α is around 30°.

For $\alpha = 60°$, as in Fig. 13, exactly six bulk vectors are used and there are no gaps in between the six subhexagons along the $v_{\rm ref}$ locus of circle 1. However, for any circle smaller than it [i.e., the lower m-index range $(60° < \alpha < 90°)$]; the zero vector must be used alternately with these six bulk vectors as given by the sequence in Table V. For example, circle 2 represents the $v_{\rm ref}$ locus at $\alpha = 65°$. It is beyond the innermost subhexagon.

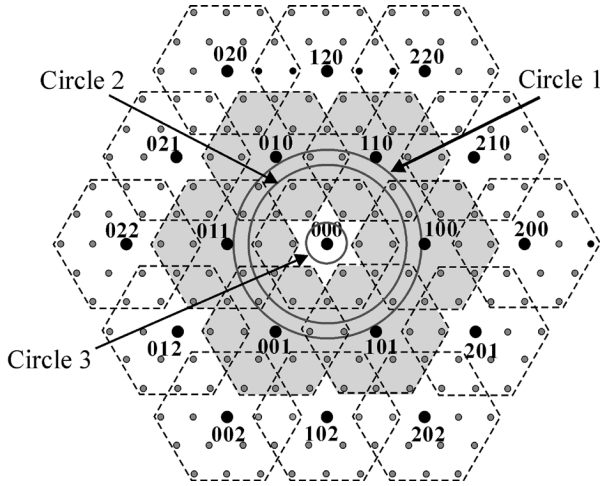

Fig. 13. Operating range analysis $(60° < \alpha < 90°)$.

Therefore, when the bulk inverter inevitably switches to 000, the conditioning inverter can no longer accurately synthesize $v_{\rm ref}$. A similar out-of-range situation exists for producing the $v_{\rm ref}$ locus along circle 3. It is then concluded that the [$60° < \alpha < 90°$] range always has performance degradation.

B. Operating Limitations for Other Types of Controls

It is easily proven that all other methods [6], [11], [12] controlling the cascade-3/3 inverters (hybrid inverters) with a 3:1 dc ratio and without a dc source in the conditioning inverter will encounter the same performance degradation m-index ranges. The same low m-index range in Fig. 13 (lower than circle 1) is used in this proof. Unlike the new control introduced in this paper, other controls [6], [11], [12] have PWM frequency switching in their bulk inverter outputs which creates bulk vector sequences other than those described in Fig. 7 and Tables III–V. But their bulk inverter fundamental value will still be equal to $|v_{\rm ref}|$. Suppose that $v_{\rm ref}$ follows circle 2. Further assume that this specific control under study can avoid the vector 000 throughout the fundamental cycle; hence, the $v_{\rm ref}$ locus along circle 2 can be continuously produced without performance degradation. However, without the zero vector, the smallest possible m-index achievable is represented by circle 1, when the sequence of the six bulk vectors is used (100-110-010-011-001-101). This contradicts the assumption and proves that the usage of the zero vector and the loss of continuous PWM coverage is inevitable.

The same problem exists for the high m-index range corresponding to $\alpha = 0° \sim 10°$. For the proximity of $\alpha = 30°$, other controls can also avoid the problem when $v_{\rm ref}$ travels across the highlighted sector in Fig. 10. However, they achieve this by implicitly switching between bulk vector pairs (for example, 220 and 110) with PWM frequency.

In summary, as long as the cascaded (hybrid) multilevel inverters operate with a 3:1 dc ratio and without a dc source in the conditioning inverter, the same performance degradation in the lower half of the m-index persists no matter what controls are being used. In Section VI, comprehensive options are provided to circumvent the performance degradation and fully utilize the proposed control set. Therefore, better converter performance and higher operational flexibility are achieved.

VI. General Control Solutions for Ideal Output Performance

As stated in the last section, the two conditions (3:1 dc ratio and capacitive dc source in the conditioning inverter) must be both satisfied to observe the performance degradations in the lower half of the m-index. Accordingly, three solutions are proposed to achieve ideal output performance in the full converter operating range. All of them use the proposed bulk inverter switching scheme and completely avoid PWM frequency switching in the bulk inverter. For capacitor voltage regulation in solutions A and B, the proposed P-Q compensation control can be used for 3:1 and 2:1 dc ratios without any change of the algorithm except for the commanded $v_{\mathrm{dc}x}$ value. The details are given in Sections VI-A and B. Solution C does not require any $v_{\mathrm{dc}x}$ regulation, so its control is very straightforward as discussed in Section VI-C.

A. Using a 3:1 Ratio Without DC Sources in the Conditioning Inverter

This solution is preferable when variable-voltage variable-frequency (VVVF) control is used; as in naval ship propulsion applications. As the bulk inverter dc-link voltage is controlled via a dc/dc converter, the m-index can be fixed at a high value or be adjustable only in the upper half of the m-index where performance degradation does not exist. A practical solution here is to first fix the m-index at the median value and ramp up the dc voltage from zero to the ship dc bus voltage. This process effectively adjusts the output voltage from zero to the half-rated value (together with output frequency). Then, the m-index can be further increased until $\alpha = 10°$, which represents the maximum practical voltage output. This solution results in better power quality for lower output voltages since more voltage levels are available. Since the dc/dc converter only operates under the half-rated output magnitude and frequency, and only about 12% of the full power is needed at half speed in ship propulsion, the rating of the dc/dc converter is small.

B. Using a 2:1 Ratio Without DC Sources in the Conditioning Inverter

In the case when the bulk inverter dc-link voltage is fixed, the lower half m-index cannot be simply avoided. Instead, it can still be correctly synthesized if the size of the "subhexagon" is increased (i.e., setting the dc ratio to 2:1). As shown in Fig. 14, the vector plot of the 2:1 ratio has no "gap" between the subhexagons of the adjacent bulk vectors. Using the previous analytical method in vector space, it can be proven that for any bulk vector traversal sequence and timing given in Fig. 7 and Tables III–V, the reference vector v_{ref} can always be enclosed by the subhexagon of the currently applied bulk vector. The problematic low m-index range is hence eliminated.

When α is close to 90°, the bulk inverter outputs narrow pulses. This does not pose a performance problem at a 2:1 dc voltage ratio since v_{ref} is enclosed by the subhexagons of the bulk vectors that are being used. An alternative explanation is that the bulk inverter power pulses keep $v_{\mathrm{dc}x}$ at its commanded value, and the conditioning inverter uses PWM to produce a low m-index output to the load. Fig. 15 shows a simulation result of this operating condition.

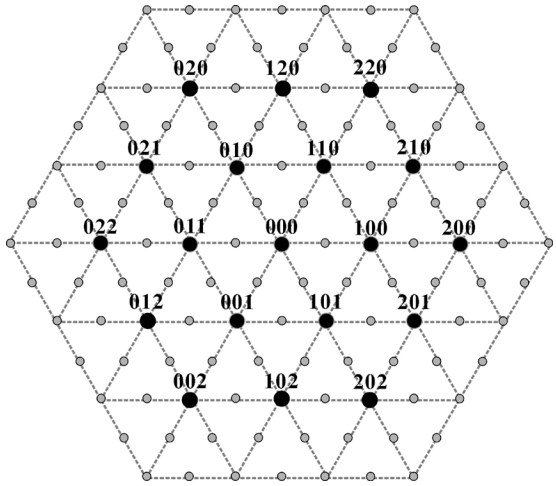

Fig. 14. Voltage vector plot when the dc ratio is 2:1.

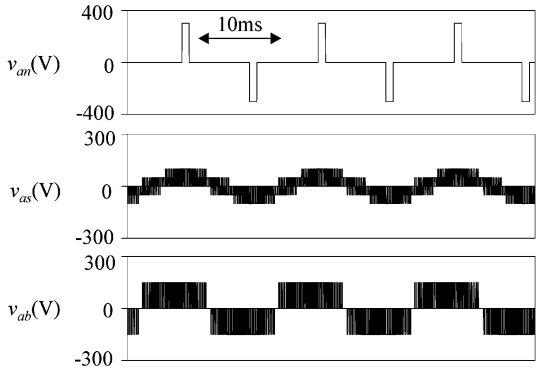

Fig. 15. Operation at a very low m-index at a 2:1 dc ratio without the dc source in the conditioning inverter.

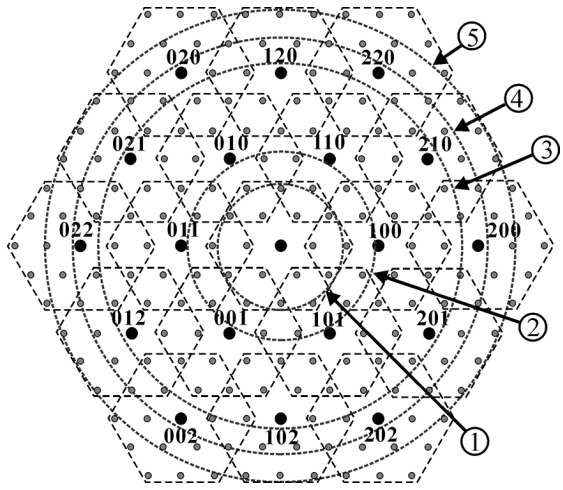

Fig. 16. Cascaded 3/3 converter control operating range (dc-source available in the conditioning inverter).

C. Using a 3:1 Ratio With DC Sources in the Conditioning Inverter

For a 3:1 ratio, allowing the bulk inverter to have a fundamental value other than the output reference $|v_{\mathrm{ref}}|$ will provide flexible bulk vector sequence and timing. This can also keep the

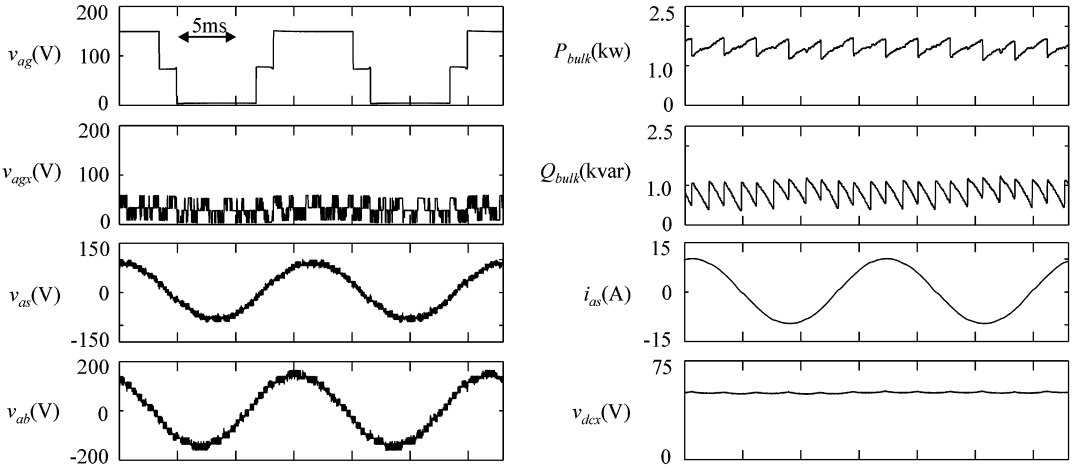

Fig. 17. Laboratory measurement.

$v_{\rm ref}$ always within the range of the conditioning inverter. However, this also entails a dc source for the conditioning inverter. In Naval ship propulsion, a dc/dc converter can be used to convert the ship dc distribution bus voltage to $v_{{\rm dc}x}$. Without the task of capacitor voltage $v_{{\rm dc}x}$ regulation, the proposed converter control can be simplified as the bulk inverter fundamental frequency switching together with the conditioning inverter control via vector subtraction between the bulk vector and output reference vector. It is usually preferred to avoid or reduce negative real power flow into the conditioning inverter [1]. Based on the same vector space analytical method, the converter operating modes and ranges are defined as in Fig. 16.

For the low m-index within the inscribing circle 1 of the innermost subhexagon (0.192*$v_{\rm dc}$), the bulk inverter can remain off and the conditioning inverter provides total output power. Between circle 1 and circle 2 ($\alpha = 60^\circ$ or 0.318*$v_{\rm dc}$), to keep the reference within the range of the conditioning inverter, the bulk inverter switches at $\alpha = 60^\circ$ with the vector sequence in Fig. 7. In this region, the bulk inverter output power exceeds the load and causes the real power flow into the conditioning inverter.

Then for the m-index to be higher than the circle 2, the positive conditioning inverter power flow can be guaranteed by keeping the bulk inverter fundamental lower than the output magnitude $|v_{\rm ref}|$ with α angle control. This operating mode continues until it reaches the circle 3 ($\alpha = 10^\circ$ or 0.627*$v_{\rm dc}$). When the output magnitude is beyond this limit, the bulk inverter has to be fixed at $\alpha = 10^\circ$ and then the conditioning inverter will provide the difference. Hence, the power direction from the conditioning inverter remains positive. Note that the α range between 0° and 10° will not be used since it requires short time durations on certain bulk vectors and causes the "out of the range" problem as previously analyzed. Finally, to keep the bulk inverter free of PWM frequency switching, the maximal system voltage output cannot exceed the magnitude represented by the circle 4 (0.689*$v_{\rm dc}$).

Then it can be easily concluded that the conditioning inverter maximal real power demand occurs when $v_{\rm ref}$ is at circle 4. However, it only constitutes 9% of the full output power. Therefore, the dc/dc converter providing $v_{{\rm dc}x}$ can have a relatively low rating.

VII. Experimental Results

The proposed converter control and analysis were verified by both simulations and experiments. As their results match well, only the laboratory data are shown. The laboratory setup uses the cascade-3/3 inverter topology as in Fig. 1 via a three-phase resistive-inductive load with $R = 7.5\ \Omega$, and $L = 7.9$ mH. The bulk inverter dc supply was set to 150 V and the conditioning inverter dc-link capacitance was 1650 μF. A floating-point digital signal processor (DSP) (TI-TMS320C32) implements the proposed control set with a sample frequency of 10 kHz and a FLEK10K field-programmable gate array (FPGA) is programmed as the multilevel PWM timer.

Fig. 17 shows the high m-index experiment results at $\alpha = 15^\circ$. Therein, the bulk and conditioning inverter line-to-ground voltages are shown on the left side as well as the load voltage, effective line-to-line voltage ($v_{ab} = v_{as} - v_{bs}$). It can be seen that the bulk inverter operates without the PWM frequency switching. The voltage v_{ab} has 15 distinct levels which is characteristic of the expected eight-level inverter performance. Two upper traces on the right side of Fig. 17 are the bulk inverter instantaneous real and reactive power outputs as computed by the DSP. The harmonic components of the P-Q power (ripples) are compensated by the conditioning inverter and the resulting load powers are in nearly dc values. The conditioning inverter capacitor voltage $v_{{\rm dc}x}$ is regulated well around 50 V by the control.

Fig. 18 shows a set of experimental results with various m-indices to further verify the effectiveness of the proposed control. As the m-index decreases, the bulk inverter staircase width decreases accordingly without introducing PWM frequency switching and $v_{{\rm dc}x}$ is always well maintained. These results also verify the analytical predictions of the performance degradations in Section V.

At $\alpha = 30^\circ$, the load voltage and line-to-line voltages are plotted in Fig. 18(a). This validates the existence of discrete leaps in the output phase voltage, which is predicted by the

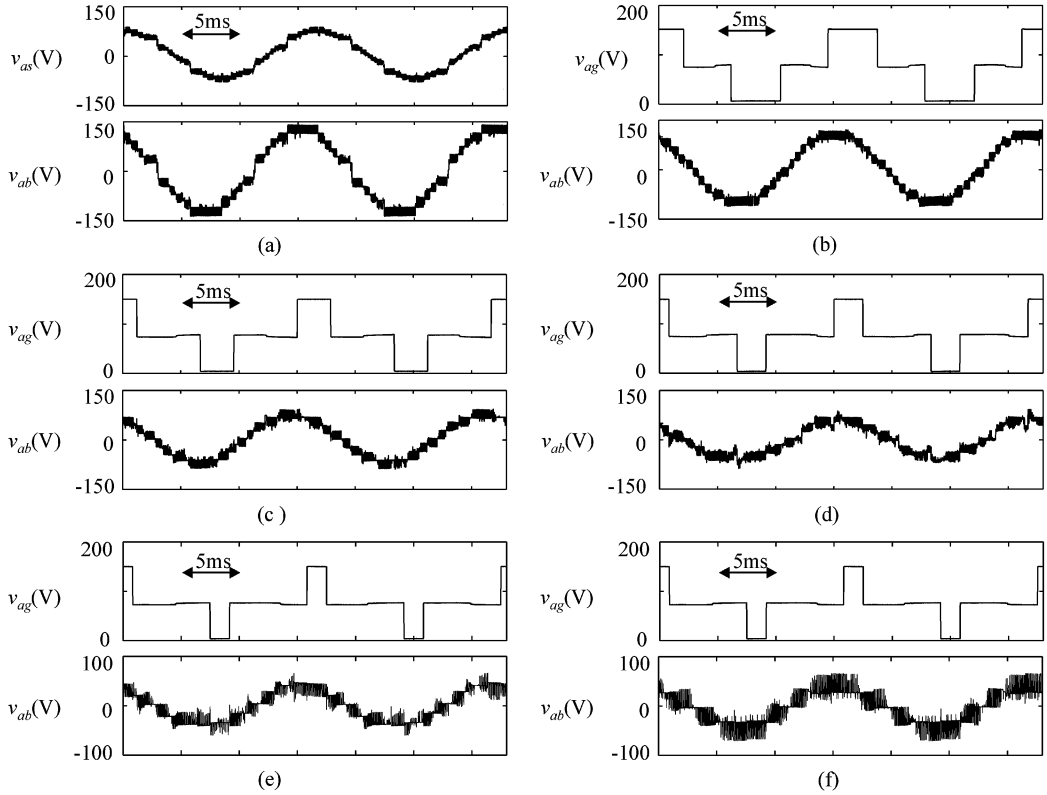

Fig. 18. Laboratory measurement of various operating points.

space vector analysis and simulation. In Fig. 18(b) and (c), when $\alpha = 42°$ and 60°, line-to-line voltages have six- and five-level inverter performance, respectively. And there is no performance degradation as is evident in the v_{ab} waveform. However, as previously predicted, any α larger than 60°, such as 65° and 70° in Fig. 18(d) and (e), will leave some portions of the reference "out-of-range" of the conditioning inverter. The problem is manifest in the deformed v_{ab} with periodic notches. In Fig. 18(f), for the same low m-index $(\alpha = 70°)$, the use of the 2:1 dc ratio solves the problem and results in a regular v_{ab} waveform.

VIII. Conclusion

This paper presents a new type of control method for the cascaded (hybrid) multilevel inverter (wherein two three-phase three-level inverters are connected in series through the load). It avoids high-frequency switching in the bulk-power inverter manufactured of IGCTs, which is caused by conventional modulation and control methods. An advanced modulation method based on P-Q compensation is developed for the control of the conditioning inverter, which implicitly creates a multilevel inverter output to the load and successfully maintains the conditioning inverter capacitor voltage so that only one dc source is needed for the cascaded multilevel inverter. An insightful and comprehensive inverter operation analysis in vector space is presented and it reveals the operating limitations for this control and also other types of controls for hybrid multilevel inverters. Various solutions are provided to avoid these limitations, which shed more insight into the general control principles of hybrid multilevel inverters. Simulation and laboratory results demonstrate the effectiveness of the proposed control set and validate the analysis.

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Shuai Lu (S'05) received the B.S.E.E. degree from Chongqing University, Chongqing, China, in 1997, the M.S.E.E. degree from the University of Wisconsin–Milwaukee, in 2003, and the Ph.D.E.E. degree from the University of Missouri–Rolla in 2007.

Currently, he is a Senior R&D Engineer with MTS System Corp., Eden Prairie, MN. His research includes several areas in power electronics and motor drives, including multilevel converters, multiphase power conversion, electric motor analysis/design/control, and their applications to hybrid (electric) vehicle and renewable energy. His current focus is the ultra-high power density and high-performance electric drive systems for hybridizing racing cars and ground vehicle testing systems. He has authored and co-authored many technical papers including seven IEEE Transactions papers, and has two patents pending.

Keith A. Corzine (S'92–M'97–SM'06) received the B.S.E.E., M.S.E.E., and Ph.D. degrees from the University of Missouri–Rolla, in 1992, 1994, and 1997, respectively.

He taught at the University of Wisconsin–Milwaukee, from 1997 to 2004. Currently, he is an Associate Professor at the University of Missouri–Rolla. His research interests include power electronics, motor drives, naval ship propulsion systems, and electric machinery analysis.