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A Stabilizing, High-Performance Controller for Input Series-Output Parallel Converters

Jonathan W. Kimball, *Senior Member, IEEE*, Joseph T. Mossoba, *Member, IEEE*, and Philip T. Krein, *Fellow, IEEE*

***Abstract*—A form of sensorless current mode (SCM) control stabilizes sharing in multiphase input-series-output-parallel (ISOP) dc–dc converter topologies. Previously, ISOP converters have been proposed to reduce the voltage and current ratings of switching devices. Since the inputs are all connected in series, each phase need only be rated for a fraction of the total input voltage. Voltage and current sharing are key—if there is any phase-to-phase imbalance, the system benefits are substantially reduced. In the present work, a simple SCM controller is shown to guarantee stable sharing. Each phase acts independently on the same output reference and desired input voltage. The algorithm and the physics of the circuit lead to balanced input voltages and output currents, even during transients. The ISOP topology is a special case of an interleaved multiphase system. A reduced-order small-signal model is presented. The model is composed of two factors, a single-phase equivalent and a multidelay comb filter. The model fits a measured transfer function well and can be used in feedback design. Experimental results for a five-phase converter demonstrate fast response to a load step, line disturbance rejection, accurate static and dynamic sharing, and high efficiency.**

***Index Terms*—Current sharing, dc–dc converter, input series output parallel (ISOP) converter, multiphase converters, sensorless current mode (SCM) control, voltage sharing.**

I. Introduction

INFORMATION technology (IT) equipment requires increasing power at decreasing voltage levels. Multistage power architectures are in common use [1]–[3]. These systems start from a relatively high voltage derived from ac mains. Next, a converter stage generates an intermediate potential, e.g., 48 V, for system-wide distribution. Sometimes, another stage generates a locally distributed potential, such as 12 V or 5 V. Finally, each load has a local point-of-load power converter to deliver precisely regulated voltage. Each stage must handle the total downstream load. System efficiency is the product of the efficiencies of each stage along this conversion sequence.

Multiphase dc–dc converters are widely used, particularly for point-of-load converters. In a multiphase system, there are several converters, each rated for a fraction of the total load power. Typically, their inputs and outputs are connected in parallel. The converter switching periods are interleaved to reduce total ripple current [4]. In a well-designed system composed of n interleaved converters, each with a switching frequency $f_{\rm sw}$, the output capacitor filters ripple current at $nf_{\rm sw}$. Many performance trade-offs become favorable, at the small expense of additional system complexity. Supervisory control methods can enable a fault-tolerant system, where a failure in one phase reduces the output power capability while the converter still delivers regulated voltage to the load.

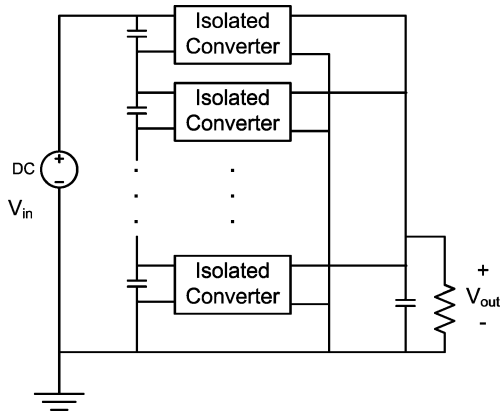

Fig. 1. Abstracted ISOP system consisting of converters 1 (bottom) through n (top).

In an input-series-output-parallel (ISOP) multiphase converter system, shown in Fig. 1, the outputs are connected in parallel, as in a standard multiphase system. The inputs are connected in series, though, rather than the typical parallel connection. An individual phase in an n-phase ISOP system sees $V_{\rm in}/n$ at its input. The reduced voltage rating provides substantial design flexibility. For example, in [5], converter ratings that would normally require the use of IGBTs were achieved with low-voltage MOSFETs. Ratings were extended further, to medium-voltage (10 kV) inputs, in [6]. As in a standard multiphase system, fault-tolerant controls are possible [7]. The ISOP approach holds excellent promise for converter systems with high input-to-output ratios. Instead of multiple sequential stages, each rated for the total load power $P_{\rm out}$, a single multiphase ISOP conversion stage with phases rated at $P_{\rm out}/n$ can provide high efficiency and high performance. Power distribution at 48 V or even 400 V dc becomes feasible, and a low intermediate voltage such as 5 or 12 V can be avoided.

In an ISOP converter connection, voltage balance is critical. The individual series inputs must share voltage evenly to make the arrangement useful. Conventional control schemes tend to give a switching power converter (or an individual phase of a multiphase system) either a constant-power characteristic or a constant-current characteristic. Either controller type will lead

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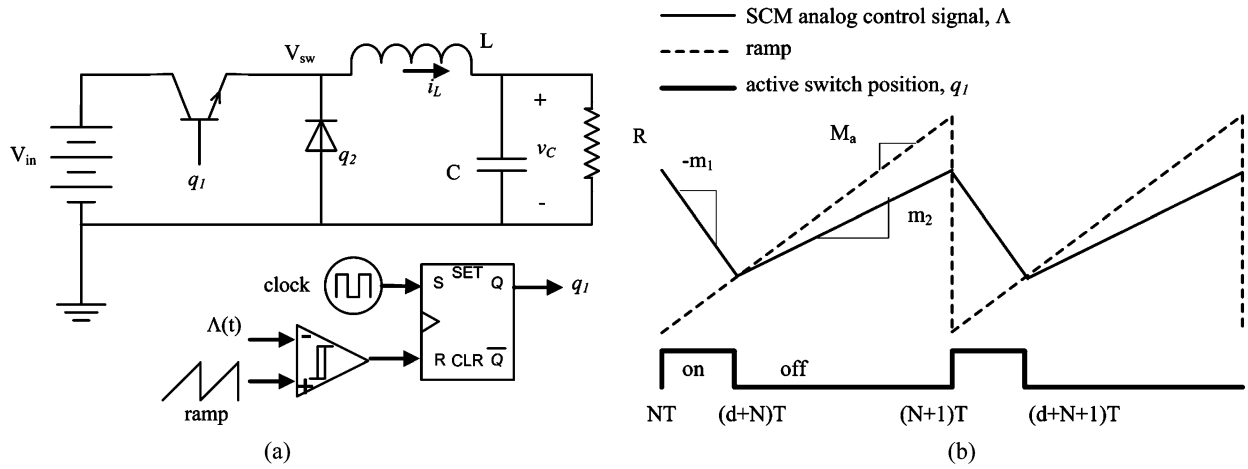

Fig. 2. Example of a buck converter (a) with SCM modulator and (b) with control waveforms.

to unstable voltage sharing in an ISOP arrangement [8]. Much of the prior work in ISOP converters has focused on multiloop control schemes to balance phase input voltages. In [5], the control system included a voltage feedforward term and a charge controller. In [9], [10], the controller used an outer output voltage loop that generated a current reference, an input voltage loop on each phase that modified the current reference, and a peak current mode controller on each phase. In [7], [11], the control loop is simpler: one phase acts as a master, and all other phases use the same duty ratio. The duty ratio could be generated either with voltage mode or current mode control. The approach in [8] resembles [9], [10], with voltage mode controllers in place of current mode controllers. Similarly, the designs in [6] are predicated on all phases switching with identical duty ratios.

Sensorless current mode (SCM) control provides an alternative control approach that can resolve the challenges in an ISOP connection. SCM control has been previously discussed and modeled in detail [12]–[16] for either single converters or conventional input-parallel output-parallel multiphase arrangements. In the present work, a variation on conventional SCM control is used to create a stable ISOP controller. This expands and formalizes preliminary work from [17]–[19]. The proposed controller uses a single outer loop to generate a reference. Each phase uses this as a global reference, along with the desired phase input voltage. These values serve as parameters in an SCM controller to generate switching waveforms. Input voltage sharing and output current sharing become stable and accurate. Transient response is similar to other multiphase techniques. The primary benefit of SCM control, as compared to the common-duty-ratio methods reported in the literature is that it provides the stable sharing of common-duty-ratio approaches while substantially improving input disturbance rejection. This results in what is effectively an open-loop ISOP sharing control that accounts for line disturbances, and requires only a modest closed-loop correction to account for load disturbances. The control algorithm is formulated in Section II. Section III contains an analysis of sharing stability. A new reduced-order small-signal model is derived in Section IV to include interleaving effects. Section V shows experimental results for a five-phase converter switching at frequencies up to 400 kHz.

II. SCM Control of an ISOP System

SCM control is a well-established alternative to voltage-mode and current-mode controls. SCM control is based on an inductor current observer [13]. Inductor node voltages are used to provide a current observer signal, which is then fed into a conventional modulator. While hysteresis or delta modulation are possible [12], [20], most implementations use pulse width modulation (PWM). For a multiphase system, fixed-frequency PWM simplifies interleaving. SCM control shares some features with other methods that use inductor voltage signals [21]–[25], as discussed in [20].

Here, SCM control is illustrated for a standard buck converter, shown in Fig. 2. As in [12], [13], the SCM control law for a buck converter is

$$\Lambda(t) = G \int (V_{\rm sw} - V^*_{\rm ref}) dt. \tag{1}$$

$V^*_{\rm ref}$ can either be a fixed reference (as in conventional open-loop SCM control) or the output of a voltage feedback system (as in conventional closed-loop SCM control). $V_{\rm sw}$ is the voltage at the switching node—the diode voltage in a buck converter. Often, $V_{\rm sw}$ is constructed from the switching function q and the input voltage $V_{\rm in}$, since we expect $V_{\rm sw} \approx qV_{\rm in}$ in this circuit. The controller output, $\Lambda(t)$, is used in a conventional PWM process or other modulation process to generate the switching function q. The integrator gain G is chosen in concert with the modulation process design [12], [16].

To derive the control law for an ISOP connection, consider the push-pull converter shown in Fig. 3. A push–pull converter provides the function of an isolated buck-derived converter suitable for the ISOP connection. The SCM control law is

$$\Lambda(t) = G \int \left(q \frac{V_{\rm in}}{a} - V^*_{\rm ref} \right) dt. \tag{2}$$

Here, a is the turns ratio of the transformer and $q = q_1 + q_2$ (a logical OR, since the signals do not overlap in a voltage-fed push-pull converter). An ISOP system is typically built from n isolated converters; a push-pull topology was used in the present work because of its overall simplicity. In an ISOP system, there are two control goals: output voltage regulation and input voltage sharing. If each phase $k \in \{1, \ldots, n\}$ simply

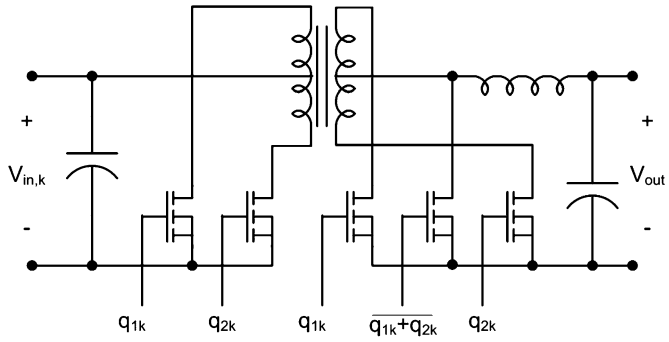

Fig. 3. One phase, k, of five-phase ISOP.

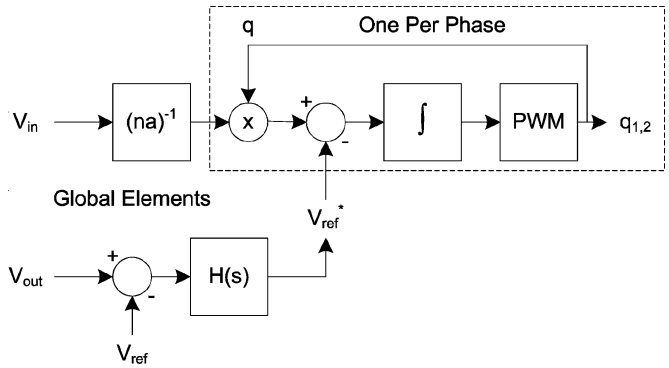

Fig. 4. Abstracted SCM controller.

uses its individual input voltage $V_{\mathrm{in},k}$, constant-power characteristics result and sharing is unstable. If instead each phase uses

$$\frac{1}{n}\sum_{i=1}^{n} V_{\mathrm{in},i} = \frac{V_{\mathrm{in}}}{n} \tag{3}$$

then phase input voltages will all be driven towards the mean. Voltage sharing is excellent and fast, as shown in Section III. Intuitively, if one phase has a high input voltage, the average voltage across its output inductor will be positive, so current will increase. The increasing current will tend to discharge the phase input capacitance and bring down the phase voltage. To satisfy Kirchhoff's voltage law, other phase voltages must increase. After a transient, voltages will all be equal. Component tolerances, particularly losses in the transformers and inductors, will distort the sharing slightly.

A typical control system is shown in Fig. 4 for an ISOP control law of

$$\Lambda_k(t) = G\int\left(q_k\frac{V_{\mathrm{in}}}{\mathrm{na}} - V_{\mathrm{ref}}^*\right)dt \tag{4}$$

for the kth phase, $k \in \{1,\ldots,n\}$. For closed-loop control, the central controller measures total input voltage and output voltage. A feedback circuit generates V_{ref}^*, while a simple gain stage or voltage divider stack generates $V_{\mathrm{in}}/(\mathrm{na})$. The central controller also supplies synchronization pulses to interleave the phases. Each phase uses V_{ref}^* and $V_{\mathrm{in}}/(\mathrm{na})$ to create a local input signal Λ_k, which is fed into a local PWM process to generate switching signals q_{1k} and q_{2k}. A logical OR generates q_k from q_{1k} and q_{2k}.

The proposed method has only one control function to regulate all phase input voltages. Naturally, component tolerances will lead to some unbalance among the phases. The present work focuses on ensuring that the effects of component variations are small, compared to the global operation. A possible addition would be supervisory loops to eliminate all phase-to-phase variation, an approach that resembles previous techniques [5], [9], [10]. The results given below show that most designs can operate without the added complexity of these extra control loops.

It might be expected that an alternative would be a system composed of n identical, independent loops. However, as there is no dc path through the series inputs, any small difference in phase currents leads to severe imbalance among the phases. In essence, the input capacitors integrate any differences in input currents, and tend to magnify even minimal differences. This effect was shown in [5] through extensive simulation studies. The solution in [5] was a complicated multiple-loop, feedforward system. The solution in the present work results in a simple control.

III. Stability Analysis

The SCM control scheme presented above accomplishes three objectives. First, with an outer voltage loop, the output voltage is tightly regulated in the presence of load disturbances. Second, the structure of the SCM controller and the physics of the circuit force automatic, stable input voltage and output current sharing. Third, as for any SCM control, the output voltage is insensitive to line disturbances since the control provides a line feedforward effect common to current-mode controls.

SCM control stability has already been studied for single-phase (standard) converters. In [12] and [13], conditions for large-signal system stability were proven with a discrete-time model. In [15] and [16], small-signal analysis established the nature of open-loop performance in the presence of input voltage and output current transients. The small-signal models can be used to design stable closed-loop controllers. To properly model the multiphase dynamics of the ISOP system, though, phase-to-phase interaction must be studied. Specifically, the objective is to prove that, given stable controllers for individual phases, all phase input voltages have stable equilibria that are nearly equal and that phase output currents have stable equilibria that are also nearly equal. That is, for all phases $k \in \{1,\ldots,n\}$ and some $\varepsilon_{\mathrm{Vin}}$ and ε_{iL}

$$\begin{aligned}
&\lim_{t\to\infty} v_{\mathrm{Ck}}(t) = V_{\mathrm{Ck}}\\
&\lim_{t\to\infty} i_{\mathrm{Lk}}(t) = I_{\mathrm{Lk},\infty}\\
&\max_k\left|V_{\mathrm{Ck}} - \frac{V_{\mathrm{in}}}{n}\right| < \varepsilon_{\mathrm{Vin}}\\
&\max_k\left|I_{\mathrm{Lk}} - \frac{I_{\mathrm{out}}}{n}\right| < \varepsilon_{\mathrm{iL}}.
\end{aligned} \tag{5}$$

Current and voltage sharing are analyzed here with a large-signal average converter model. The phases have individual SCM controllers that each receive the same inputs: reference voltage V_{ref}^* and desired phase input voltage V_{in}/n. The SCM control process generates a switching waveform with duty ratio D. Since all phase controllers receive the same inputs, the commanded duty ratios will be equal, as in [6], [7], [11]. The advantage of using SCM is that D will change instantly

as $V_{\rm in}$ varies, such that the output voltage does not change. Fig. 5 shows an equivalent model of two phases, numbered k and $k+1$, in which the push-pull converters are replaced with controlled ideal transformers—a commonly used visualization of state-space averaging. The physical transformers within the converters have turns ratio a. All of the conduction losses in the MOSFETs, transformer, and inductor are lumped into $R_{\rm Lk}$. Switching losses and magnetic losses are modeled as an equivalent resistance, $R_{\rm mk}$. For a given input voltage and reference, D is a parameter, and the system can be treated as linear about an operating point value of D. In the analysis, however, component values may differ from phase to phase.

Kirchhoff's current law at the node joining the inputs of phases k and $k+1$ requires

$$C_k\frac{dv_{\rm Ck}}{dt}+\frac{D}{a}i_{\rm Lk}+\frac{v_{\rm ink}}{R_{\rm mk}} -C_{k+1}\frac{dv_{\rm Ck+1}}{dt}-\frac{D}{a}i_{\rm Lk+1}-\frac{v_{\rm ink+1}}{R_{\rm mk+1}}=0. \quad (6)$$

Kirchhoff's voltage law applied on the secondary side gives

$$\frac{D}{a}v_{\rm ink}-R_{\rm Lk}i_{\rm Lk}-L_k\frac{di_{\rm Lk}}{dt}-V_{\rm out}=0 \quad (7)$$

where $v_{\rm ink}=v_{\rm Ck}+R_{\rm Ck}C_k(dv_{\rm Ck})/(dt)$. For an n-phase converter, there are n capacitor voltages and n inductor currents to consider. This stability analysis treats $V_{\rm out}$ as a parameter. The first $n-1$ capacitor voltage equations derive from (6), while the nth equation is

$$C_n\frac{dv_{\rm Cn}}{dt}+\frac{D}{a}i_{\rm Ln}+\frac{v_{\rm inn}}{R_{mn}}-I_{\rm in}=0. \quad (8)$$

As with output voltage, the input current from the source, $I_{\rm in}$, acts as a parameter. Equations (6) through (8) can be written in matrix form; for example, a five-phase complete model is

$$\hat{C}_k=C_k(1+R_{\rm Ck}/R_{\rm mk}) \quad (9)$$

$$\mathbf{C}=\begin{bmatrix}\hat{C}_1&-\hat{C}_2&0&0&0\\0&\hat{C}_2&-\hat{C}_3&0&0\\0&0&\hat{C}_3&-\hat{C}_4&0\\0&0&0&\hat{C}_4&-\hat{C}_5\\0&0&0&0&\hat{C}_5\end{bmatrix} \quad (10)$$

$$\mathbf{R_C}=-\frac{D}{a}\begin{bmatrix}R_{C1}&0&0&0&0\\0&R_{C2}&0&0&0\\0&0&R_{C3}&0&0\\0&0&0&R_{C4}&0\\0&0&0&0&R_{C5}\end{bmatrix} \quad (11)$$

$$\mathbf{L}=\begin{bmatrix}L_1&0&0&0&0\\0&L_2&0&0&0\\0&0&L_3&0&0\\0&0&0&L_4&0\\0&0&0&0&L_5\end{bmatrix} \quad (12)$$

$$\mathbf{G_m}=\begin{bmatrix}-1/R_{m1}&1/R_{m2}&0&0&0\\0&-1/R_{m2}&1/R_{m3}&0&0\\0&0&-1/R_{m3}&1/R_{m4}&0\\0&0&0&-1/R_{m4}&1/R_{m5}\\0&0&0&0&-1/R_{m5}\end{bmatrix} \quad (13)$$

$$\mathbf{A}_{12}=\frac{D}{a}\begin{bmatrix}-1&1&0&0&0\\0&-1&1&0&0\\0&0&-1&1&0\\0&0&0&-1&1\\0&0&0&0&-1\end{bmatrix} \quad (14)$$

$$\mathbf{A}_{21}=\frac{D}{a}\begin{bmatrix}1&0&0&0&0\\0&1&0&0&0\\0&0&1&0&0\\0&0&0&1&0\\0&0&0&0&1\end{bmatrix} \quad (15)$$

$$\mathbf{R_L}=\begin{bmatrix}-R_{L1}&0&0&0&0\\0&-R_{L2}&0&0&0\\0&0&-R_{L3}&0&0\\0&0&0&-R_{L4}&0\\0&0&0&0&-R_{L5}\end{bmatrix} \quad (16)$$

$$\begin{bmatrix}\mathbf{C}&\mathbf{0}\\\mathbf{R_C}&\mathbf{L}\end{bmatrix}\frac{d}{dt}\begin{bmatrix}\mathbf{v_C}\\\mathbf{i_L}\end{bmatrix}=\begin{bmatrix}\mathbf{G_m}&\mathbf{A}_{12}\\\mathbf{A}_{21}&\mathbf{R_L}\end{bmatrix}\begin{bmatrix}\mathbf{v_C}\\\mathbf{i_L}\end{bmatrix}+\begin{bmatrix}0\\0\\0\\0\\I_{\rm in}\\-V_{\rm out}\\-V_{\rm out}\\-V_{\rm out}\\-V_{\rm out}\\-V_{\rm out}\end{bmatrix}. \quad (17)$$

The matrix on the left side of (17) is structurally nonsingular as long as C_k and L_k are all nonzero. The system can be premultiplied by the inverse of this matrix to generate a standard state-space form $\dot{\mathbf{x}}=\mathbf{Ax}+\mathbf{Bu}$. The eigenvalues of the new $\mathbf{A}$ matrix can be found symbolically to determine stability (a tool such as Mathematica[1] is of value here). For an n-phase converter, there are n pairs of eigenvalues given by (18), shown at the bottom of the next page. In the sequel, the result of adding the square root of the discriminant will be referred to as the "fast" eigenvalue, and the other root will be referred to as the "slow" eigenvalue. All of the eigenvalues have negative real part as long as duty ratio D is nonzero. Therefore, provided only that switching is taking place, the dynamical system of (17) has a stable equilibrium at which

$$V_{\rm Ck}=\frac{R_{\rm mk}}{R_{\rm Lk}+(D/a)^2R_{\rm mk}}(I_{\rm in}R_{\rm Lk}+(D/a)V_{\rm out})$$
$$I_{\rm Lk}=\frac{aDI_{\rm in}R_{\rm mk}-a^2V_{\rm out}}{D^2R_{\rm mk}+a^2R_{\rm Lk}}. \quad (19)$$

In a well-designed converter, all equivalent resistances will be nearly equal, so currents and voltages will be nearly equal. R_m is typically large, while R_L is typically small. Inductor and capacitor value variations affect system dynamics but do not affect equilibrium values. The system will return to a sharing condition regardless of mismatches in L and C values. However, if the values of L and C match, the eigenvalues also match, and the various voltages and currents will follow each other dynamically in response to an external disturbance. For static matching from (19), often, turns ratio errors will dominate the result, but even turns ratio variations will lead only to limited mismatch in the final results.

[1]Mathematica is a registered trademark of Wolfram Research, Inc.

TABLE I
COMPONENT VARIATION AND EFFECT ON (A) STATIC SHARING WITH PROPOSED CONTROLLER ACTIVE AND (B) EIGENVALUES WITH PROPOSED CONTROLLER ACTIVE

COMPONENT	VARIATION	EFFECT ON VOLTAGE SHARING	EFFECT ON CURRENT SHARING
L	Any positive value	None	None
C	Any positive value	None	None
R_L	±30%	±0.59%	±0.11%
R_C	±30%	None	None
R_m	±30%	-0.15% / +0.08%	-7.6% / +4.1%
a	±1%	±1.0%	±0.82%

(a)

COMPONENT	VARIATION	EFFECT ON FAST EIGENVALUE	EFFECT ON SLOW EIGENVALUE
L	±30%	-43% / +23%	Negligible
C	±30%	-42% / +22%	±0.5%
R_L	±30%	±0.48%	±0.37%
R_C	±30%	±30%	-42% / +23%
R_m	±30%	Negligible	-0.15% / +0.08%
a	±1%	±2%	Negligible

(b)

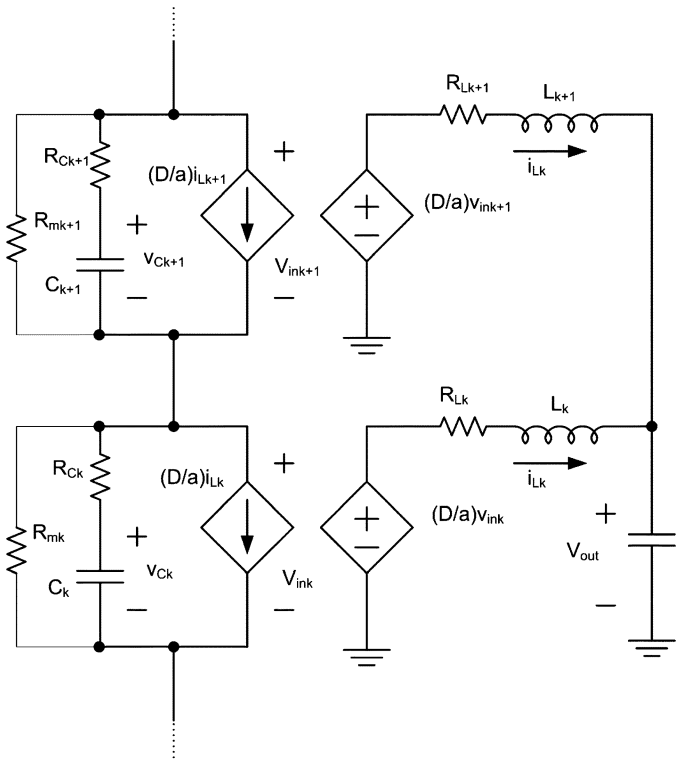

Fig. 5. Model of two adjacent phases in an ISOP converter system.

The degree of mismatch with the proposed controller in place is difficult to judge from the analytical forms in (18)–(19), so a numerical sensitivity analysis was performed. The sensitivity analysis allows a designer to evaluate both "out-of-the-box" variation due to manufacturing tolerances and variation over design life due to temperature and aging effects. The results are summarized in Table I for typical component value variation. The nominal values were derived from the experimental system shown below. The strongest impact on voltage sharing is turns ratio a, whereas the biggest influence on current sharing is R_m. Still, the static variations would have little influence on design margins since even with $\pm 30\%$ component variations the voltage variation is only about 1% and the current variation is only about 4%. L and C values affect eigenvalues, primarily the fast eigenvalue, but have no impact on steady-state sharing. Of the loss components, only R_C has a significant impact on eigenvalues. Given the small voltage and current variations despite large parameter variations, a designer can feel confident that the simple SCM controller will provide stable, accurate sharing despite manufacturing tolerances or aging effects.

Dynamic sharing is dominated by eigenvalue variation. Each phase gives rise to two system eigenvalues. The fast eigenvalues, which dominate inductor current transients, are usually at extremely high frequencies, so inductor currents respond rapidly to changes and quickly converge to a matched condition. For the slow eigenvalues, which dominate capacitor voltage transients, capacitor ESR variations of $\pm 30\%$ yield eigenvalue changes

$$-\frac{L_k + (D/a)^2 R_{\mathrm{Ck}} R_{\mathrm{mk}} + R_{\mathrm{Lk}} C_k (R_{\mathrm{Ck}} + R_{\mathrm{mk}}) \pm \sqrt{\mathrm{DISCRIMINANT}}}{2 L_k C_k (R_{\mathrm{Ck}} + R_{\mathrm{mk}})}$$

$$\mathrm{DISCRIMINANT} = ((D/a)^2 R_{\mathrm{Ck}} R_{\mathrm{mk}} + C_k R_{\mathrm{Lk}} (R_{\mathrm{Ck}} + R_{\mathrm{mk}}) + L_k)^2 \cdots - 4 L_k C_k (R_{\mathrm{Lk}} + (D/a)^2 R_{\mathrm{mk}})(R_{\mathrm{Ck}} + R_{\mathrm{mk}}) \quad (18)$$

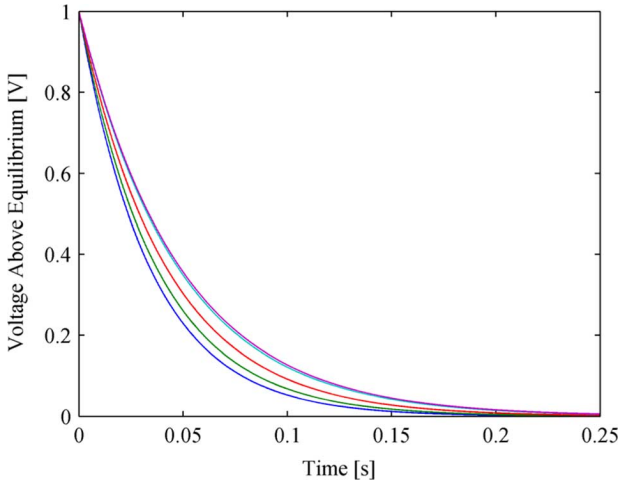

Fig. 6. Example transient for phases with varying parameters (five phase input capacitor voltages shown).

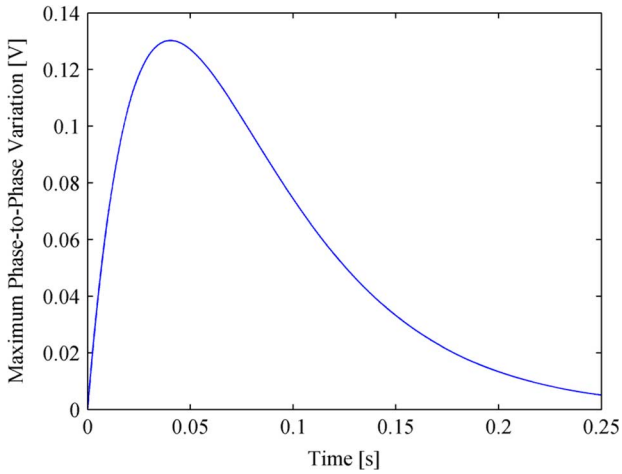

Fig. 7. Example transient for phases with varying parameters (maximum capacitor voltage difference shown).

over a range from -42% to $+23\%$, given realistic converter values. Other parameters, including capacitance, have little effect on the slow eigenvalues. To demonstrate the effect of eigenvalue variation, a Monte Carlo simulation was performed with component values that reflect the full range of parameters noted in the experiments in Section V. This includes a $\pm 10\%$ mismatch range for inductance and capacitance and $\pm 20\%$ mismatches in the parasitic resistances. Fig. 6 shows capacitor voltages just after an input voltage step of $-$ 5 V, where the baseline is the new mean phase input voltage. In the figure, the slow eigenvalues range from -29 to -21 rad/s. Even with this substantial variation, the dynamic difference never exceeds the size of the step divided by the number of phases, and is usually much smaller, as shown in Fig. 7.

The result of this analysis is that if stable SCM controllers are used for the individual converters, and the command structure described above is employed, then the result will be stable sharing of input voltage and output current among the

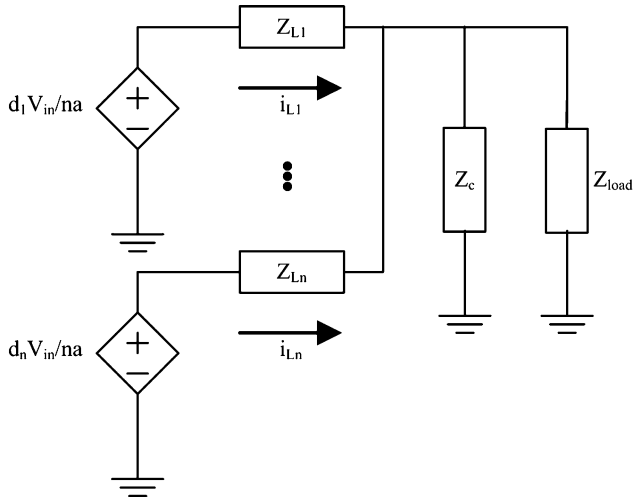

Fig. 8. Simplified multiphase model of n-phase ISOP converter, which assumes an equivalent buck converter structure for each phase.

phases, with low mismatch even during transient conditions. Large-signal stability for SCM control is similar to that for peak-current-mode control, and a stabilizing ramp is needed for duty ratios above 50%. Small-signal stability must be addressed in closed-loop design, as in [13], but both large-signal and small-signal stability requirements are routine aspects of converter design. This proves the result to be shown: Given a multiphase ISOP configuration, in which individual phases are controlled by stable SCM controllers, it is sufficient for stable sharing to have a common reference output voltage and common target input voltage $V_{\rm in}/n$.

The next section derives an equivalent model from a combination of n matched phases. Based on the result that phase voltages and currents are well matched, simplifying assumptions are possible and a combined equivalent is of value in closed-loop design.

IV. Small-Signal Dynamic Model

A full-order model of an ISOP system is difficult to analyze and provides little insight. Interleaving delays increase the order of system transfer functions if transport delays are represented by rational polynomial approximations. Order reduction [14], [26]–[28] provides a useful approach that still captures the essential behavior. The reference-to-output transfer function of an interleaved SCM converter $H_{\rm mp}(s)$ can be modeled as the product of a single-phase equivalent converter model $H^{\rm eq}_{\rm phase}(s)$ and a factor $\Psi(s)$ that aggregates the interleaving delays

$$H_{\rm mp}(s) \doteq \frac{v_{\rm out}(s)}{v^*_{\rm ref}(s)} = H^{\rm eq}_{\rm phase}(s)\Psi(s). \tag{20}$$

A Laplace domain reduced-order model (20) derives from a simplified full order small signal model of the power train, represented by Fig. 8, which assumes equal input voltages for each phase ($V_{{\rm in},k} = V_{\rm in}/n, k \in \{1, \ldots, n\}$) of the ISOP structure. Equation (21) gives the output voltage in terms of the phase- k

inductor current $(i_{L,k})$, and the combined parallel filter capacitance (Z_C) and load impedance $(Z_{\rm Load})$

$$v_{\rm out}(s) = (Z_C \| Z_{\rm Load}) \sum_{k=1}^{n} i_{L,k}(s). \tag{21}$$

The time-interleaving of the switching functions, illustrated in Fig. 9, is included in the model through the small-signal duty ratio variation of phase k, given as d_k. Under steady interleaving, the phase k duty ratio can be expressed in terms of the duty ratio in phase 1 as $d_k = d_1 e^{(-sT(k-1))/(n)}$. Assuming equal phase inductances $(Z_{L,k} = Z_L)$, the result is $i_{L,k} = ((V_{\rm in}/{\rm na})d_k - v_{\rm out})/(Z_L)$, so that

$$v_{\rm out}(s) = (Z_C \| Z_{\rm Load}) \sum_{k=1}^{n} \frac{(V_{\rm in}/{\rm na})d_k - v_{\rm out}}{Z_L}. \tag{22}$$

A solution for $v_{\rm out}$ gives the Thevenin equivalent source voltage $\bar{V}_{\rm in} d_1$ with an impedance divider formed by the Thevenin equivalent phase impedance of $Z_L^{\rm eq} = Z_L/n$

$$v_{\rm out}(s) = \frac{(Z_C \| Z_{\rm Load})}{(Z_C \| Z_{\rm Load}) + Z_L/n} \times ((V_{\rm in}/{\rm na})d_1) \left(\sum_{k=1}^{n} \frac{e^{\frac{-sT(k-1)}{n}}}{n} \right). \tag{23}$$

Since the SCM control modulator provides a feedforward effect on input voltage [15], the reference $(v_{\rm ref}^*)$ to output expression becomes

$$\underbrace{\frac{v_{\rm out}(s)}{v_{\rm ref}^*(s)}}_{H_{\rm mp}} = \underbrace{\frac{(Z_C \| Z_{\rm Load})(V_{\rm in}/{\rm na})}{(Z_C \| Z_{\rm Load}) + Z_L/n} \left(\frac{d_1}{v_{\rm ref}^*} \right)}_{H_{\rm phase}^{\rm eq}} \underbrace{\left(\frac{1}{n} \frac{1 - e^{-sT}}{1 - e^{-\frac{sT}{n}}} \right)}_{\Psi}. \tag{24}$$

This multidelay model captures both the equivalent single-phase performance $(H_{\rm phase}^{\rm eq})$ and the effects of interleaving delays (Ψ). Under assumptions of phase-to-phase symmetry and a single global control signal $v_{\rm ref}^*$, the single phase equivalent model has the parameter values in Table II.

Since the SCM modulators all use the control law $\Lambda(t) = G \int (q(V_{\rm in})/({\rm na}) - v_{\rm ref}^*) dt$, the ramp slope of the single phase equivalent model is unchanged from the per-phase value. This preserves the line-disturbance rejection properties of SCM control for buck converters [12], [15], [16] and means the large-signal stability properties of the combined equivalent match those of the individual phases. The reduced-order model (24) has a single-phase equivalent duty ratio and switching period that differ from the apparent multiphase duty ratio, $D_{\rm mp}$ [14], [27], and the corresponding effective switching period $T_{\rm mp}$ of the summed multiphase interleaved currents. $T_{\rm mp}$ is simply the ripple frequency T/n, while $D_{\rm mp}$ is the fractional part of nD. The implicit modulo operator in the definition of

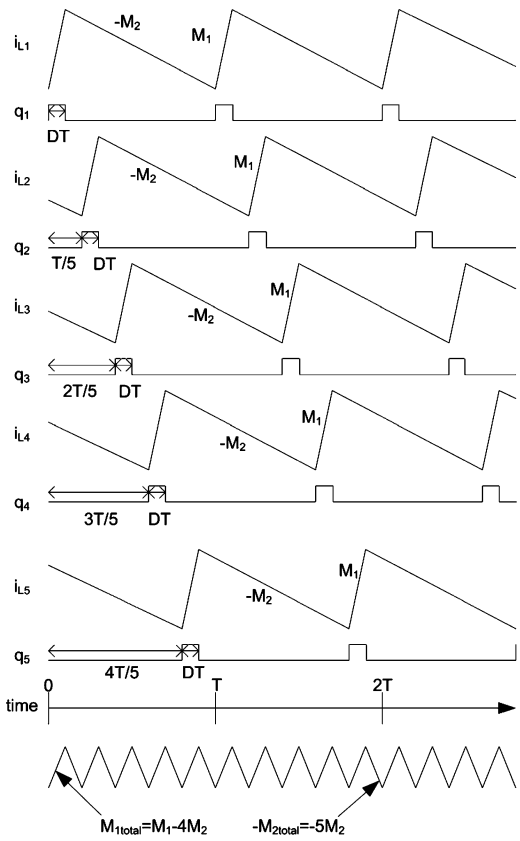

Fig. 9. Five-phase interleaved inductor current waveforms for analysis of output current ripple.

$D_{\rm mp}$ means that the apparent multiphase duty ratio is discontinuous with respect to D. The inductor current waveforms for a five-phase interleaved system (Fig. 9) illustrate these differences: in this example, each phase has 10% duty and switching period T, while the apparent duty ratio of summed inductor currents for five phases is 50% with apparent switching period T/n. In a five-phase system, an increase in D from 10% to 25% corresponds to a change in $D_{\rm mp}$ from 50% to 25% (the fractional part of 5×0.25). The discontinuous relationship between apparent duty ratio and ripple complicates efforts to capture the average ripple behavior of the summed inductor currents in the single-phase equivalent. The reduced-order model presented above (24) avoids this discontinuity and preserves the meaning of duty ratio for the individual phases.

The static benefit of having reduced output current ripple with ripple period T/n results from interleaving. The development above shows that the average linearized multiphase interleaved system can be modeled as a single-phase equivalent whose controller operates with switching period T, not T/n. The equivalent switching period given in Table II implies restrictions on the bandwidth of the reference-to-output response of the multiphase VRM. While the reduced-order model has been derived for SCM control, similar conclusions hold for voltage mode and current mode controllers.

The multiphase SCM control model assumptions are summarized as follows.

1) Voltages and currents share ideally. The previous sections justified this assumption for static and dynamic conditions.

TABLE II
SINGLE-PHASE EQUIVALENT POWER NETWORK PARAMETERS

N-PHASE SYSTEM	SINGLE-PHASE EQUIVALENT
Switching period per phase: T	Equivalent switching period: $T_{eq} = T$
Inductance per phase: L	Equivalent inductance: $L_{eq} = L/n$
Output capacitance: C	Equivalent output capacitance: $C_{eq} = C$
Load resistance: R_{load}	Equivalent load resistance: $R_{Load}^{eq} = R_{Load}$

2) The n phases are interleaved: switching takes place in synchronism, with phase k delayed by $(k-1)(360^\circ/n), k \in \{2, \ldots, n\}$, relative to phase 1.
3) The multiphase SCM control dynamics can be modeled by a single equivalent phase with switching period $T_{\rm eq} = T$, identical to a single phase of the symmetric ISOP system but with parameters

$$Z_L^{\rm eq} = Z_L/n, C_{\rm eq} = C \text{ and } R_{\rm Load}^{\rm eq} = R_{\rm Load}.$$

Under these assumptions, the model for the single-phase equivalent can be developed as in [15]. The small-signal transfer function, including output capacitor ESR effects, is

$$\begin{aligned} &H_{\rm phase}^{\rm eq}(s) \\ &\quad = \frac{(V_{\rm in}/{\rm na})(2+(2D-1)sT)R_{\rm load}(1+sC_{\rm out}R_{\rm Cout})}{2\left(\frac{V_{\rm in}}{\rm na}+M_a sT\right)(a_0+a_1 s+a_2 s^2)} \\ &a_0 = R_{\rm load}+R_L^{\rm eq} \\ &a_1 = L_{\rm out}^{\rm eq}+C_{\rm out}R_{\rm Cout}R_{\rm load}+C_{\rm out}(R_{\rm load}+R_{\rm Cout})R_L^{\rm eq} \\ &a_2 = C_{\rm out}L_{\rm out}^{\rm eq}(R_{\rm load}+R_{\rm Cout}) \end{aligned} \quad (25)$$

where $R_{\rm Cout}$ is the parasitic resistance of the output capacitor, M_a is the SCM ramp slope of a single phase controller, and D is the duty ratio of the single phase equivalent [15]. Model accuracy will be evaluated in Section V for an experimental five-phase converter.

V. EXPERIMENTAL RESULTS

The goal of the proposed control scheme is to force input voltages and output currents to share both in steady state and during transients. A five-phase converter was constructed to demonstrate stable sharing, high efficiency, and good performance. Converter parameters are summarized in Table III. Switching frequency is nominally 350 kHz for each phase converter. The reference $V_{\rm ref}$ was set to 1.0 V for all experiments. No special effort was made to minimize variation, except that the parts were all purchased simultaneously and therefore were from the same lots. Transformer leakage inductances, which directly affect R_m, could not be measured accurately. The transformers were hand-wound, so substantial variation can be assumed. The experiments below show that the significant phase-to-phase variation in losses does not translate into significant phase-to-phase variation in voltage or current.

The controller was built from discrete analog and digital components for maximum flexibility. All operational amplifiers are model TLE2082, which has a typical gain-bandwidth product of 10 MHz. The ramp shown in Fig. 2 was constructed from a resistor, a capacitor, and an analog switch (M74HC4066) driven by the synchronization pulse. The slope was set so that $M_a = m_2$ [12] to enhance line rejection. The PWM comparator was a TLV3501, which has a typical transition time of 4.5 ns. Simple

TABLE III
PARAMETERS FOR EXPERIMENTAL SYSTEM CAPACITORS MEASURED AT 10 KHZ INDUCTORS MEASURED AT 100 KHZ

MOSFET	FDS7088N3	L_k	906 ± 60 nH
n	5	R_k	46.6 ± 18 mΩ
a	5	C_{out}	347 µF
C_k	49.9 ± 0.6 µF	R_{Cout}	38 mΩ

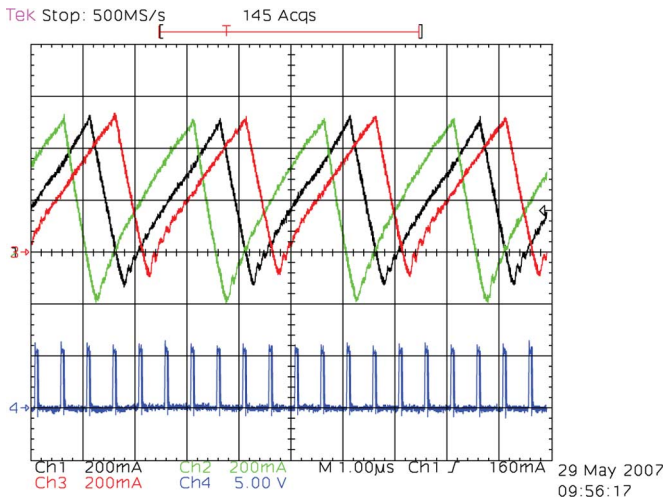

Fig. 10. Experimental interleaving at 1 μs/div with a 1 Ω load. Top set of traces, channels 1 through 3, inductor currents for phases 5, 4, and 1, respectively, 200 mA/div; bottom trace, channel 4, synchronization pulse at 2 MHz, 5 V/div.

logic chips, MIC4427 gate drivers, and SM76925 gate drive transformers completed the control section. Interleaving waveforms are shown for three of the five phases in Fig. 10 to correlate to the theoretical waveforms in Fig. 9. The offsets in the current probes were not zeroed out for this figure, so the dc offsets are not meaningful. The figure is intended to emphasize the timing information, which is accurate.

Static voltage sharing is examined in Fig. 11. Here the load current was fixed at 0.1 A and switching frequency was fixed at 300 kHz. All five phases should have input voltage that is 20% of the total; the actual ratios varied from a minimum of 0.197 to a maximum of 0.203—substantially better than the expected mismatches among the converters. The maximum input deviation from the mean input voltage was 1.6%. The phases were physically arranged so that phase 3 was connected most directly to the load, while phases 1 and 5 were both some distance away (higher inductance and resistance). As load current increases, phase 3 input voltage drops relative to the mean to reflect the added impedance from the outlying phases. A similar set of curves is shown in Fig. 12 for a load current of 2 A and switching frequency of 300 kHz. The corresponding phase-to-total voltage

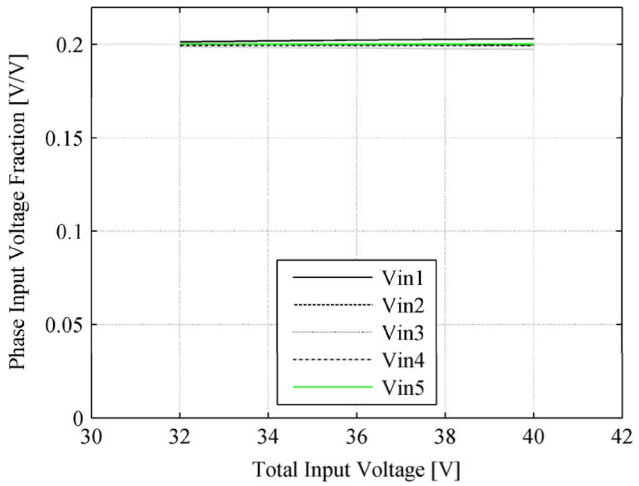

Fig. 11. Phase input voltages as a fraction of total input voltage to show static sharing, 0.1 A load, 300 kHz switching.

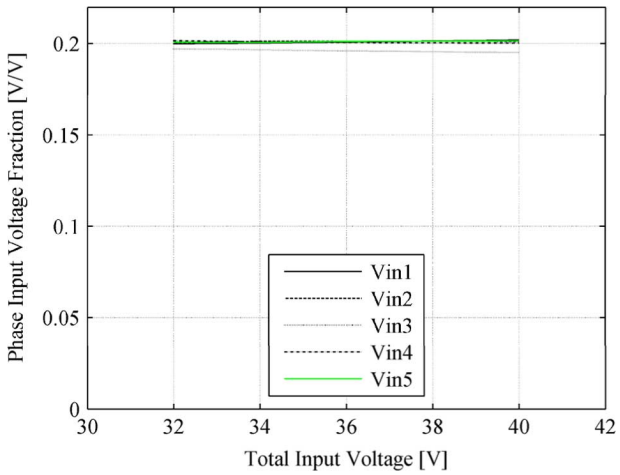

Fig. 12. As in Fig. 11, with load increased to 2 A.

ratios varied from 0.195 to 0.202. Phase 3, which is the furthest from the mean, is still within 2.4% of the mean input voltage. Since voltage sharing is excellent with the proposed controller even with substantial parameter variation, device ratings can be chosen for $V_{\rm in}/n$ with little margin.

Four of the phase currents were measured with a TCP202 Hall effect current probe. The load current was known based on measured load resistance. Offset and drift limit the dc accuracy to about $\pm$ 5 mA. The phase 3 current was taken as the net remaining value, estimated from known load resistance and other phase currents; its measurement error would be greatest. Still, as Fig. 13 shows, dc current sharing is excellent. The biggest difference from the mean is 5%, most likely governed by the 30% R_m variation as discussed in Section III.

Closed-loop performance with a feedback controller relies on a good small-signal model. The reference-to-output transfer function, shown in Fig. 14, was measured with an HP4195A network/spectrum analyzer for a 0.9 A load and 400 kHz switching frequency (per phase). Two models are superimposed: a single-phase model ($H^{\rm eq}_{\rm phase}$) and a complete model that includes delay ($H_{\rm mp}$). The fit is good for both models up to about 25% of the switching frequency, while the complete model continues to track to much higher frequency. The parameters for the model

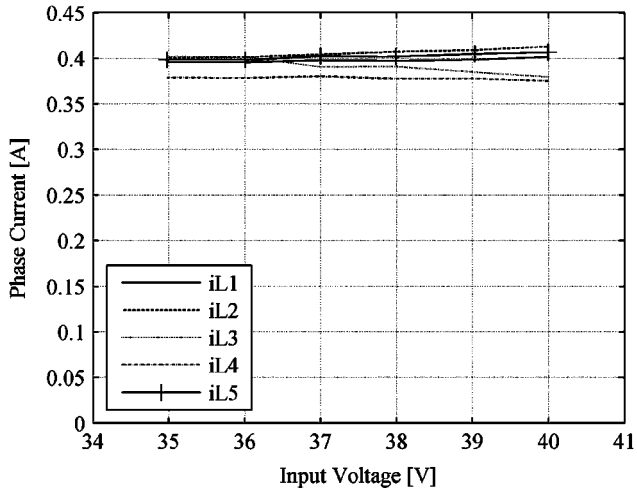

Fig. 13. Measured phase currents with a 0.5 Ω load.

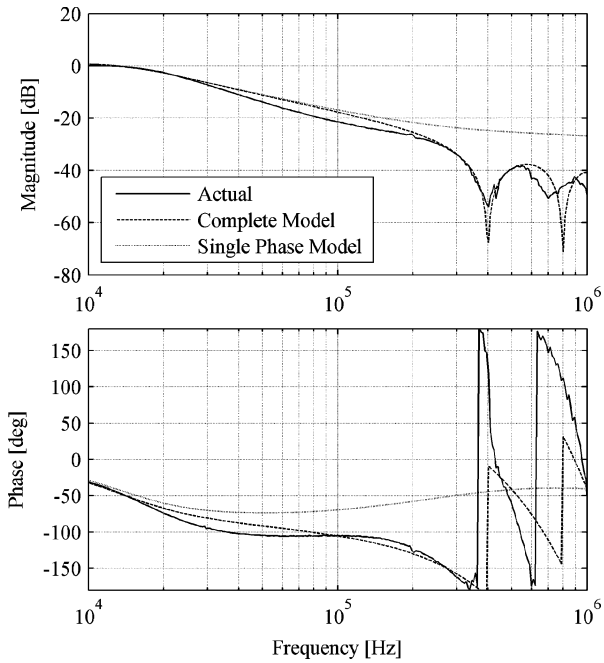

Fig. 14. Measured and modeled plant transfer functions for 0.9 A load, 400 kHz switching per phase.

came directly from the measured values, except that an inductance of 2 μH was used to account for leakage in the transformers and wiring inductance in the layout. With a simple proportional-integral (PI) controller, with a proportional gain of 5.75 and an integral gain of 2.13 $\times 10^5$, the loop gain crosses 0 dB at 56 kHz with 68° phase margin.

Transient responses are shown in Figs. 15 and 16. An input voltage step is shown in Fig. 15 with a 1 A load. The voltage divides evenly between the phases throughout the transient. The output voltage recovers quickly. The effect of a load current step on the output is shown in Fig. 16, in which the step is from 1.0 Ω to 0.1 Ω (1 to 10 A). The output voltage deviation is $-$ 80 mV to $+$72 mV.

Input voltage and load current share during line and load transients. Fig. 15 shows voltage sharing during an input voltage step—phase voltages appear to be scaled versions of the total

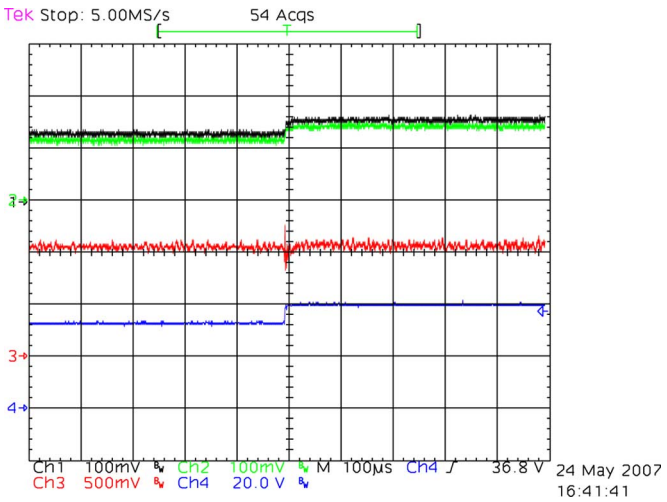

Fig. 15. Input voltage step at 100 μs/div. Top traces, channels 1 and 2, phase 5 and 4 input voltages, 5 V/div; middle trace, channel 3, output voltage, 500 mV/div; bottom trace, channel 4, input voltage, 20 V/div.

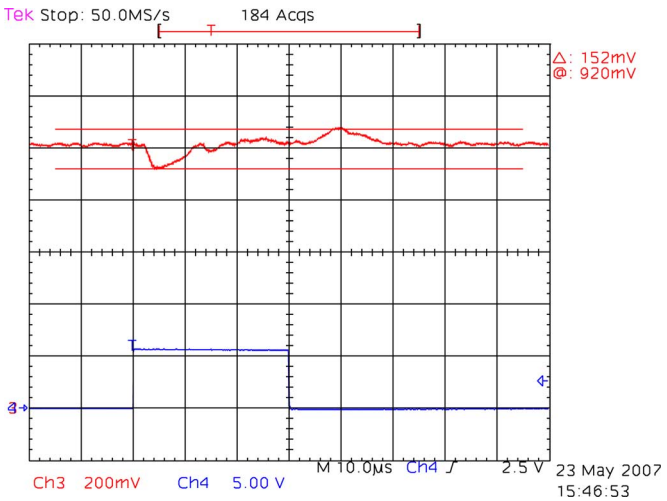

Fig. 16. Load current step (from 1 A to 10 A) at 10 μs/div. Top trace, channel 3, output voltage, 200 mV/div; bottom trace, channel 4, load command (logic signal).

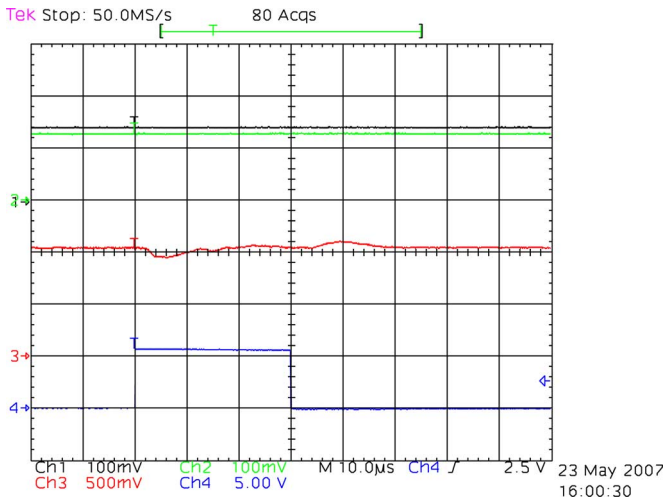

Fig. 17. Load current step (1 A to 10 A) at 100 μs/div. Top traces, channels 1 and 2, phase 5 and 4 input voltages, 5 V/div; middle trace, channel 3, output voltage, 500 mV/div; bottom trace, channel 4, load command (logic signal).

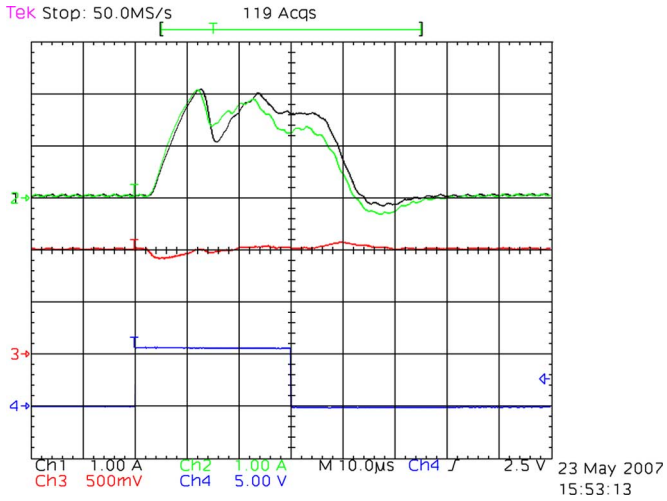

Fig. 18. Load current step (1 A to 10 A) at 100 μs/div. Top traces, channels 1 and 2, phase 5 and 4 output currents, 1 A/div; middle trace, channel 3, output voltage, 500 mV/div; bottom trace, channel 4, load command (logic signal).

input voltage, as desired. Figs. 17 and 18 each show the same load transient as in Fig. 16, a pulse from 1 A to 10 A, then back to 1 A. In Fig. 17, channels 1 and 2 are phase input voltages, which do not deviate at all. Probe offset is the basis for the apparent static difference. In Fig. 18, channels 1 and 2 are phase output currents. The dynamic differences are small despite slightly unequal phase impedance. Oscilloscope averaging was used to eliminate switching ripple effects and reveal the underlying current dynamics. Although stability was proven in Section III for constant input voltage, load resistance, and reference voltage, these experiments show that sharing is stable over a wide range of transient conditions because of the stability of the underlying SCM control process.

One advantage of the ISOP structure is high power conversion efficiency even with high input-to-output ratios. Fig. 19 shows efficiency as a function of output current with 300 kHz switching. The losses can be fit with

$$P_{\text{loss}} = 0.6451 \times 10^{-3} I_{\text{out}}^2 + 1.2 \times 10^{-9} f_{\text{sw}} V_{\text{in}}^2. \qquad (26)$$

The I_{out}^2 term reflects resistances in the system—inductors, transformers, MOSFETs, circuit board traces, and interconnection. The equivalent resistance in the loss estimate (26) is much smaller (less than 1 m Ω) than in the small-signal model (9.3 m$\Omega = \langle R_{\text{Lk}} \rangle / 5$) because of frequency effects. That is, small-signal performance includes proximity effect and core loss in the magnetic devices, but dc resistance dominates efficiency. The larger $f_{\text{sw}} V_{\text{in}}^2$ term accumulates several effects, primarily switching losses in the MOSFETs. The estimate fits the experimental measurements well for currents above 0.2 A, switching frequencies between 300 and 400 kHz, and input voltage between 32 and 40 V. For the designed operating point of $f_{\text{sw}} = 300$ kHz, $V_{\text{in}} = 36$ V, and $V_{\text{out}} = 1$ V, efficiency exceeds 80% over most of the output current range (above 2 A) and is 95.9% for an output of 10.5 A and 1 V.

VI. Conclusion

SCM control provides a stable alternative for the ISOP converter topology. This control approach produces accurate input

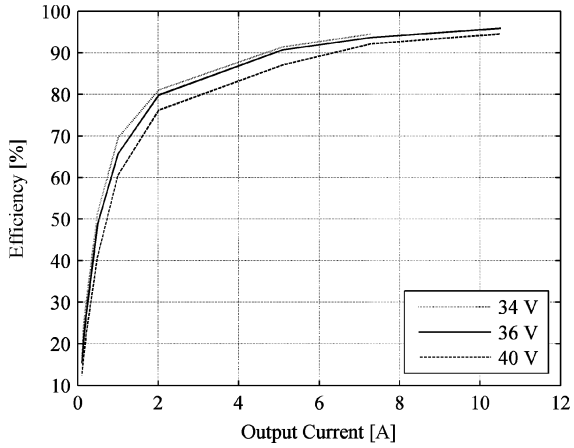

Fig. 19. Efficiency with $f_{sw} = 300$ kHz.

voltage and output current sharing even in the face of component mismatch among the multiple converters. Stability results were given. A reduced-order small-signal model was shown. The overall approach, in which the system transfer function is partitioned into an equivalent single-phase component and a multidelay component, is also valid for multiphase systems with other controllers. Experimental results on a five-phase system switching at up to 400 kHz per phase validate the theoretical predictions, both for static sharing and for dynamic performance. The ISOP controller inherits many of the benefits of SCM control, such as excellent line disturbance rejection. The same general arrangement can be applied to input-parallel output-series (IPOS) converter configurations.

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He was an Engineer with Tektronix, Beaverton, OR, then returned to the University of Illinois. At present, he holds the Grainger Endowed Director's Chair in Electric Machinery and Electromechanics as Director of the Grainger Center for Electric Machinery and Electromechanics. He published the undergraduate textbook *Elements of Power Electronics* (Oxford, UK: Oxford University Press, 1998). In 2001, he helped initiate the International Future Energy Challenge, a major student competition involving fuel cell power conversion and energy efficiency for machines. He holds eleven U.S. and four European patents. His research interests address all aspects of power electronics, machines, and drives, with emphasis on nonlinear control approaches.

Dr. Krein was a Senior Fulbright Scholar at the University of Surrey, Surrey, UK, from 1997 to 1998, was recognized as a University Scholar in 1999 (the highest research award at the University of Illinois), and received the IEEE William E. Newell Award in Power Electronics in 2003. From 1999 to 2000 he served as President of the IEEE Power Electronics Society. From 2005 to 2007, he was a Distinguished Lecturer of the IEEE Power Electronics Society. He founded and is past Editor-in-Chief of the IEEE POWER ELECTRONICS LETTERS and serves on the IEEE Board of Directors for Division II. He is a Registered Professional Engineer in Illinois and in Oregon.