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Standby Leakage Power Reduction Technique for Nanoscale CMOS VLSI Systems

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***Abstract*—In this paper, a novel low-power design technique is proposed to minimize the standby leakage power in nanoscale CMOS very large scale integration (VLSI) systems by generating the adaptive optimal reverse body-bias voltage. The adaptive optimal body-bias voltage is generated from the proposed leakage monitoring circuit, which compares the subthreshold current ($I_{\rm SUB}$) and the band-to-band tunneling (BTBT) current ($I_{\rm BTBT}$). The proposed circuit was simulated in HSPICE using 32-nm bulk CMOS technology and evaluated using ISCAS85 benchmark circuits at different operating temperatures (ranging from 25 °C to 100 °C). Analysis of the results shows a maximum of 551 and 1491 times leakage power reduction at 25 °C and 100 °C, respectively, on a circuit with 546 gates. The proposed approach demonstrates that the optimal body bias reduces a considerable amount of standby leakage power dissipation in nanoscale CMOS integrated circuits. In this approach, the temperature and supply voltage variations are compensated by the proposed feedback loop.**

***Index Terms*—Band-to-band tunneling (BTBT) leakage, gate leakage, leakage current, leakage power, optimal body bias voltage, subthreshold leakage.**

I. Introduction

OVER the past four decades, the size of transistors has continuously been reduced to increase the device speed and density on a given chip and the die yield during manufacturing. For device reliability and constant power dissipation per unit area, the supply voltage has been reduced as well. Therefore, continuous reduction in the threshold voltage of the transistor, which ensures high drive current and hence performance improvements, is inevitable [1].

Recently, however, as the supply voltage approaches 1 V, conventional scaling has deviated from ideal constant-field scaling due to the difficulty of further lowering the threshold voltage ($V_{\rm th}$). This fundamental problem stems from the nonscalable characteristic of the thermal voltage ($V_T = kT/q$), which causes relatively fixed subthreshold swing (S) at the constant temperature [2]–[4]. This, in turn, makes the subthreshold leakage current exponentially increase as the $V_{\rm th}$ reduces. Therefore, there exists a lowest possible value of $V_{\rm th}$, which is determined by the application constraints related to power consumption and circuit functionality. In addition, with the knowledge of increased $V_{\rm th}$ variation in nanoscale MOSFETs, it is necessary to keep enough margins for $V_{\rm th}$ variation to ensure that $V_{\rm th}$ stays well away from the lowest possible value of $V_{\rm th}$ [3]. In particular, for high-performance (HP) logic technology, it is required to keep a certain level of the overdrive voltage ($V_{\rm DD} - V_{\rm th}$), which determines the drive current and hence the performance in a chip. This makes it difficult to accomplish the further scaling down of the supply voltage. Fig. 1 shows the difficulty of further supply voltage scaling [3]. Under fixed $V_{\rm th}$, the reduction of $V_{\rm DD}$ trades off performance (speed) and leakage power. This trend in technology scaling has made us enter a new era in achieving HP under constrained power [4]. Fig. 2 shows the power density trends for active and standby leakage power for different channel lengths [5].

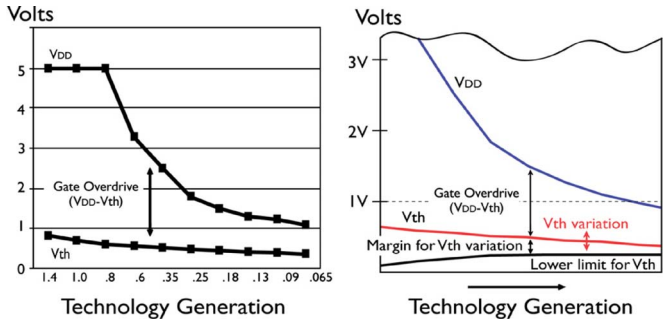

Fig. 1. Trend of supply voltage and threshold voltage scaling.

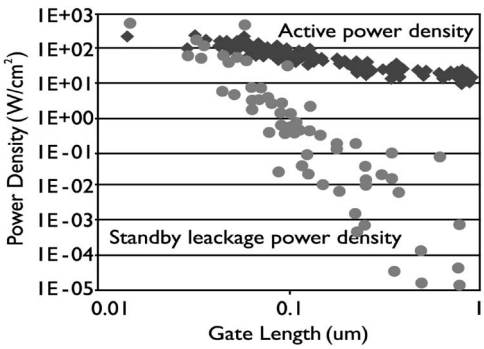

Fig. 2. Power density trends for the active power and the standby leakage power with CMOS (channel length) scaling.

Among the leakage power reduction techniques, the reverse body biasing (RBB) technique, which increases the threshold voltage ($V_{\rm th}$) of transistors during standby mode, has widely been employed to suppress the subthreshold leakage

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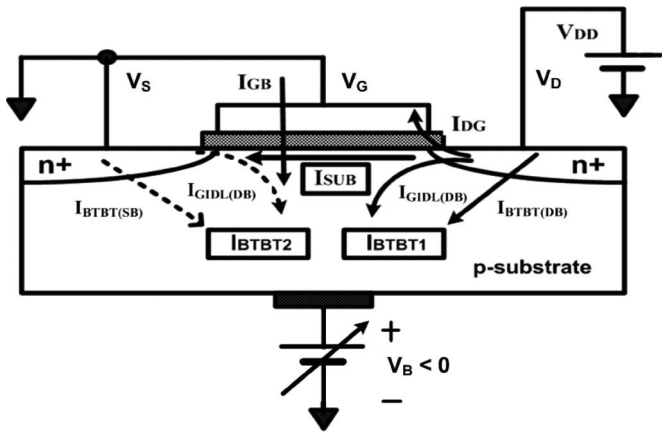

Fig. 3. Standby leakage current components under reverse body bias.

current $(I_{\rm SUB})$. However, this technique also aggravates short channel effects (SCEs), such as drain-induced barrier lowering (DIBL), gate-induced drain leakage (GIDL), and band-to-band tunneling (BTBT) current. In particular, GIDL and BTBT current significantly increase under the reverse body bias condition since the state-of-the-art MOSFETs are fabricated with high overall doping concentration, lowered source/drain junction depths, halo doping, high-mobility channel materials, etc. Furthermore, the reduction of the gate oxide thickness $(t_{\rm ox})$ causes a drastic increase in the gate tunneling leakage current due to carriers tunneling through the gate oxide, which is a strong exponential function of the voltage magnitude across the gate oxide [2], [9]. Consequently, to minimize the leakage power in standby mode, those leakage components have to be taken into account when the RBB technique is used.

The adaptive RBB technique has been proposed [6]–[9]. However, the previous techniques require significant circuit modification and performance overhead for leakage reduction, and they have not been complete or robust enough to apply to very large scale integration (VLSI) systems since all the leakage-current components and minimum supply voltage are not considered for leakage power reduction. While [16] shows that the leakage power can significantly be decreased using both optimum power supply voltage and optimal body bias voltage, it requires a lot of circuit overhead. Therefore, this paper proposes a new standby leakage power reduction technique applicable to VLSI systems by exploiting the body bias voltage scaling only while all the other leakage currents are taken into account. The proposed approach significantly reduces the required hardware compared with [16] by optimizing the body bias voltage only at the cost of efficiency of the standby current minimization.

II. Standby Leakage Current Components in MOSFET Under RBB (Reverse Body Bias)

Fig. 3 shows the leakage current $(I_{\rm leakage})$ components under the reverse body-bias condition. The total leakage current in the OFF-state n-MOSFET is given by

$$I_{\rm leakage} = I_{\rm SUB} + I_{\rm BTBT(DB)} + I_{\rm BTBT(SB)} + I_{\rm GIDL(DB)} + I_{\rm GIDL(SB)} + I_{\rm GB} + I_{\rm DG} \quad (1)$$

where $I_{\rm SUB}$ is the subthreshold leakage current, $I_{\rm BTBT(DB)}$ and $I_{\rm BTBT(SB)}$ are the BTBT leakage currents (drain-to-bulk and source-to-bulk reverse-bias p-n junction leakage currents), $I_{\rm GIDL(DB)}$ and $I_{\rm GIDL(SB)}$ are the GIDL currents, $I_{\rm GB}$ is gate-to-bulk oxide tunneling leakage current, and $I_{\rm DG}$ is drain-to-gate oxide tunneling leakage current.

The subthreshold leakage current is the weak inversion conduction current dominated by the diffusion current flowing between the drain and the source when $|V_{\rm GS}| < |V_{\rm th}|$. This weak inversion conduction current can be expressed based on [11]

$$I_{\rm sub} = \mu C_{\rm dep} \frac{W}{L} V_T^2 \left(\exp \frac{V_{\rm GS} - V_{\rm th}}{nV_T}\right) \left(1 - \exp \frac{-V_{\rm DS}}{V_T}\right) \quad (2)$$

where $C_{\rm dep} = \sqrt{\varepsilon_{\rm si} q N_{\rm sub}/(4\phi_B)}$ denotes the capacitance of the depletion region under the gate area, $\varepsilon_{\rm si}$ is the permittivity of Si, q is the electron charge, $N_{\rm sub}$ is the doping concentration of the p-substrate, ϕB is the built-in potential, V_T is the thermal voltage that is equal to kT/q, $C_{\rm ox}$ is the oxide capacitance per unit area between the gate metal and the bulk surface, and n is the subthreshold parameter and is expressed as $1 + C_{\rm dep}/C_{\rm ox}$.

As shown in (2), when the MOSFET is off $(V_{\rm GS} = 0\ {\rm V})$, the subthreshold current exponentially increases with the decrease of the threshold voltage. On the other hand, the transistor threshold voltage equation considering the body effect is given by

$$V_{\rm th} = V_{\rm th0} + \gamma \left(\sqrt{|2\Phi_F + V_{\rm SB}|} - \sqrt{|2\Phi_F|}\right) \quad (3)$$

where $\gamma = \sqrt{2q\varepsilon_{\rm si} N_{\rm sub}}/C_{\rm ox}$ is the body-effect coefficient, Φ_F is the Fermi potential and is equal to $(kT/q)\ln(N_{\rm sub}/n_i)$, where n_i is the intrinsic electron concentration, and $V_{\rm SB}$ is the source-to-bulk potential difference. Since the subthreshold leakage current $(I_{\rm SUB})$ is the major leakage component, the RBB technique is used in this paper to reduce the total leakage current in standby-mode CMOS circuits by increasing the transistor threshold voltage. However, it is important to watch how other leakage current components change when the RBB is used to estimate the total leakage.

The BTBT leakage current, which is also called reverse-bias p-n junction leakage currents, is the current flow between the source/drain (S/D) and the substrate through the parasitic reverse-biased p-n junction diode during the OFF-state MOSFET. If both S/D and substrate regions are heavily doped, then BTBT significantly increases since the electric field across the junction depletion region increases. If the high electric field $(> 10^6\ {\rm V/cm})$ is formed across the reverse-biased junctions of the source/drain (S/D) regions so that the voltage drop across the junction is bigger than the bandgap of silicon, particularly with increasing S/D voltage or reverse body bias, then a significant amount of BTBT current flows through the S/D to the substrate junctions. In nanometer devices, higher channel and S/D doping with shallow junction depths are required to minimize SCEs, which cause a significant increase in BTBT current [10].

The GIDL current, which is also called the surface BTBT current, is the drain-to-substrate leakage due to the BTBT current in very high field depletion region in the gate-drain overlap region. When the drain of an n-MOSFET is biased at the supply voltage ($V_{\rm DD}$) and the gate is biased at either zero or negative voltage, a depletion region is formed under the gate and drain overlap region. In the same way as the BTBT current, if the high electric field is formed in the narrower depletion region as a result of the reverse bias between channel and drain, then a significant amount of surface BTBT current flows through the drain-to-substrate junctions due to the twisting of bandgaps. With higher supply voltage, thinner oxide thickness, lightly doped drain, reverse body bias (RBB) technique, and high mobility channel materials having smaller bandgaps, the GIDL current is enhanced [12], [13].

$I_{\rm GB}$ is the gate-to-bulk oxide tunneling leakage current, and $I_{\rm DG}$ is the drain-to-gate oxide tunneling leakage current. As the gate oxide thickness scales below 2 nm, the direct tunneling (DT) gate leakage exponentially increases due to quantum mechanical tunneling. The DT gate leakage current can not only increase the standby power dissipation but also limit the proper logic gate operation. Recently, a high-k dielectric base on Hafnium and dual metal gate has been introduced to increase the transistor performance. The high-k dielectric material reduces the gate leakage as the gate dielectric thickness can actually be increased while the gate capacitance is increased [14].

III. Optimal Body-Bias Voltage and Supply Voltage

As explained in the previous section, the main components of standby leakage power are the gate tunneling leakage power, the subthreshold leakage power, and the reverse biased junction BTBT leakage power. For convenience, let us denote that $I_{\rm BTBT1} = I_{\rm GIDL(DB)} + I_{\rm BTBT(DB)}$, $I_{\rm BTBT2} = I_{\rm GIDL(SB)} + I_{\rm BTBT(SB)}$, $I_{\rm gate} = I_{\rm GB} + I_{\rm DG}$, and $I_{\rm BTBT} = I_{\rm BTBT1} + I_{\rm BTBT2}$. Therefore, the total standby leakage power is given by

$$P_{\rm leakage} \approx I_{\rm gate}V_{\rm gate} + I_{\rm SUB}V_{\rm SUB} + I_{\rm BTBT}V_{\rm BTBT} \qquad (4)$$

where $V_{\rm gate}$, $V_{\rm SUB}$, and $V_{\rm BTBT}$ are the voltage sources of each leakage component. Fig. 4 shows the effect of body bias voltage and supply voltage on the standby leakage current for a 32 nm n-MOSFET Berkeley Predictive Technology Model. The gate leakage current is not significantly affected by $V_{\rm Body}$ since $I_{\rm DG}$ is not function of $V_{\rm Body}$, as shown in Fig. 4(a) [9]. However, it exponentially increases with the increase of the supply voltage. In Fig. 4(b), as the supply voltage decreases from 0.9 to 0.5 V and the body bias voltage ($V_{\rm Body}$) decreases from 0 to -2.5 V, the subthreshold leakage current decreases while the BTBT leakage current increases. As shown in (2), the subthreshold leakage current is an exponential function of the threshold voltage ($V_{\rm th}$). Therefore, the RBB technique is an effective way to increase the threshold voltage ($V_{\rm th}$) to suppress the subthreshold leakage current ($I_{\rm SUB}$) in standby-mode CMOS

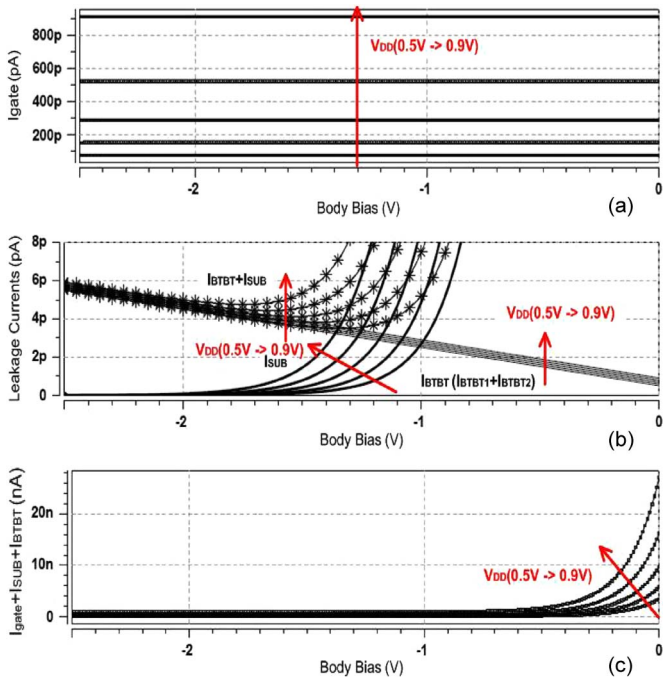

Fig. 4. Standby ($V_{\rm GS} = 0$ V) leakage currents of a 32-nm n-MOSFET with $t_{\rm ox} = 0.9$ nm and $W/L = 128$ nm/32 nm as a function of body bias voltage and supply voltage: (a) $I_{\rm gate}$. (b) $I_{\rm SUB}$, $I_{\rm BTBT}$, and $I_{\rm BTBT} + I_{\rm SUB}$. (c) Total Leakage current $= I_{\rm BTBT} + I_{\rm SUB} + I_{\rm gate}$.

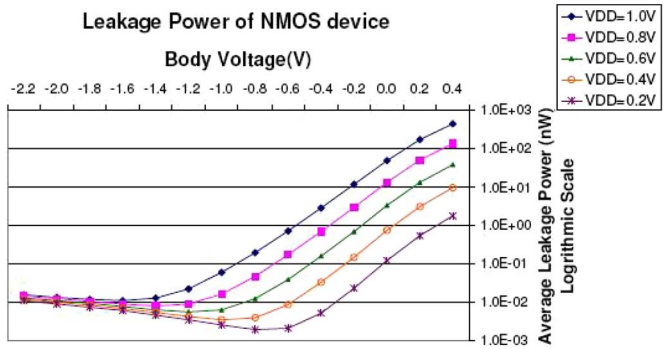

Fig. 5. Leakage power of NMOS device under reverse body.

circuits. With the increase of reverse body bias, $V_{\rm SB}$ becomes more positive, which results in higher threshold voltage and hence exponential decrease of the subthreshold current, as explained in (2) and (3). The plot of $I_{\rm BTBT} + I_{\rm SUB}$ in Fig. 4(b) explains why the leakage power consumption of a chip does not continue to monotonically decrease with increasing reverse body bias.

Fig. 5 shows the effect of body bias voltage and supply voltage on the leakage power for an NMOS transistor of 32-nm CMOS technology. At around -0.8 to -2.2 body bias voltage, the leakage power increases due to the highly increased $I_{\rm BTBT}$. $I_{\rm gate}$ has less effect on the power variation. As a result, there is an optimal reverse body bias point that makes the minimal total standby leakage power of a device for each different supply voltage.

Therefore, the optimal body bias voltage that reduces the total leakage current is determined by the relationship between

$I_{\rm SUB}$ and $I_{\rm BTBT}$. In [6], $I_{\rm SUB}$ and $I_{\rm BTBT}$ are given in simplified form as follows:

$$I_{\rm SUB} \approx A_S e^{B_S V_{\rm Body}} \tag{5}$$

$$I_{\rm BTBT} \approx A_b e^{-B_b V_{\rm Body}} \tag{6}$$

where A_b, B_b, A_S, and B_S are the technology-dependent constants, and $V_{\rm Body}$ is the body bias voltage.

The minimal leakage power with respect to an optimal $V_{\rm Body}$ is calculated by the following equation:

$$\frac{\partial P_{\rm leakage}}{\partial V_{\rm Body}} = 0. \tag{7}$$

Note that $I_{\rm gate}$ is ignored because the gate tunneling leakage changes little as $V_{\rm Body}$ changes, as shown in Fig. 4(a). From (4)–(7), the condition for minimal leakage power is obtained as follows:

$$B_S I_{\rm SUB} = B_b I_{\rm BTBT}. \tag{8}$$

The ratio of B_b and B_S for the minimal leakage current determines the ratio of $I_{\rm SUB}$ and $I_{\rm BTBT}$, as given in (8). Under the assumption of $B_b/B_S = 1$, $I_{\rm SUB}$ must be equal to $I_{\rm BTBT}$ to reduce the leakage power. The optimal $V_{\rm Body}$ to reduce the sum of $I_{\rm SUB}$ and $I_{\rm BTBT}$ is found from Fig. 4(b), and it is smaller than $V_{\rm Body}$ to make $I_{\rm SUB}$ equal to $I_{\rm BTBT}$. However, near the value of -1 V of $V_{\rm Body}$, the total leakage current $(I_{\rm SUB} + I_{\rm BTBT} + I_{\rm gate})$ is almost equal to $I_{\rm gate}$, as shown in Fig. 4(c), i.e., $V_{\rm Body}$ that makes $I_{\rm SUB}$ equal to $I_{\rm BTBT}$ can be selected as a near-optimal value.

The significant leakage component, when the body-bias voltage is at the optimal value of $V_{\rm Body}$, is the gate leakage $I_{\rm gate}$. Therefore, the supply voltage must be decreased as much as possible to reduce $I_{\rm gate}$. The reduction of supply voltage decreases the optimal reverse $V_{\rm Body}$, as shown in Figs. 4(b) and 5.

IV. Circuit Implementation

A. Subthreshold Leakage Current Suppression Using Stack Effect

The subthreshold leakage current is reduced when there are two or more stacked off-transistors. By turning off more than one transistor in a stack of transistors, it forces the intermediate node voltage to have a value higher than zero. This causes a negative $V_{\rm GS}$, $V_{\rm BS}$ (more body effect), and $V_{\rm DS}$ reduction (less DIBL) in the top transistor, thereby helping reduce the subthreshold leakage current flowing through the stack considerably, which is known as the stack effect, and this results in reduced subthreshold leakage current. Figs. 6 and 7 illustrate the leakage current trends of each stacked transistors as a function of the stacked transistor number [15], [16].

B. Proposed $V_{\rm Body}$ Control System

In the previous section, the optimal $V_{\rm Body}$ points are found theoretically and through simulations/measurements of a MOSFET. In this section, the hardware implementation of the proposed $V_{\rm Body}$ control system that minimizes the overall power dissipation is introduced. This hardware allows the independent and adaptive adjustment and maintenance of the body-bias voltages when the operating conditions change. The proposed scheme in Fig. 8 consists of the leakage monitoring circuit, the current comparator, and the charge pump.

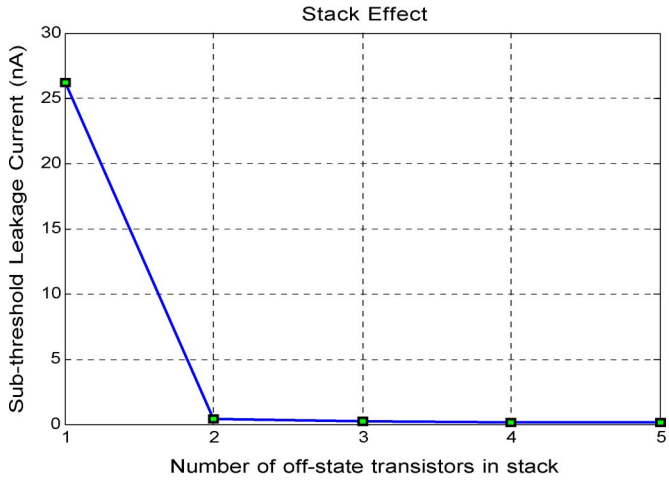

Fig. 6. Leakage current decrease with an increasing number of off transistors in stack (where $V_{\rm DD} = 0.9$ V is applied to 32-nm n-MOSFETs with 0.9-nm oxide thickness and $W/L = 128$ nm/32 nm).

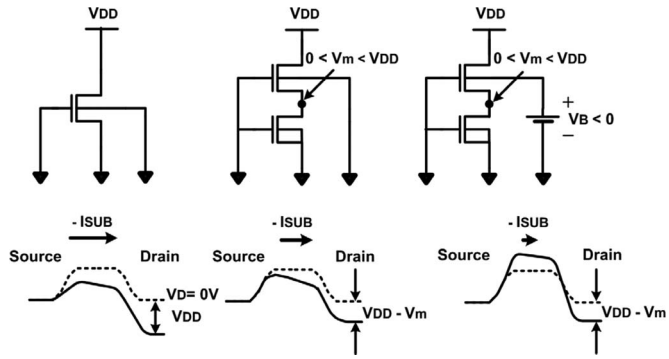

Fig. 7. Subthreshold leakage current differences among (a) a single off-transistor, (b) a stack of two off-transistors, and (c) a stack of two off-transistors with reverse body bias. The barrier height increases for a stack of two off-transistors shown in (b) due to both negative $V_{\rm GS}$ and $V_{\rm DS}$ reduction ($V_{\rm DS} = V_{\rm DD} - V_{\rm m} < V_{\rm DD}$), and the barrier height further increases for a stack of two off-transistors with reverse body bias shown in (c) due to the stronger body effect than in (b) (increased $V_{\rm SB}$).

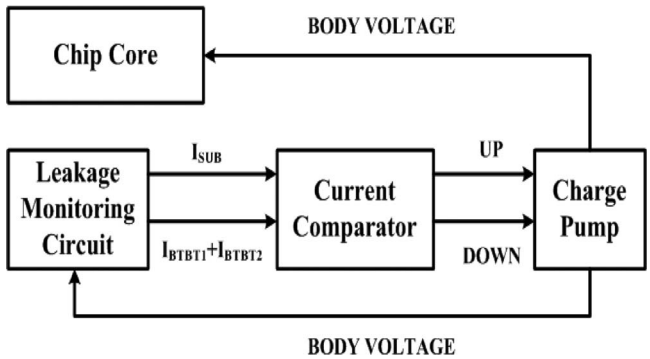

Fig. 8. Block diagram of the proposed $V_{\rm Body}$ control system.

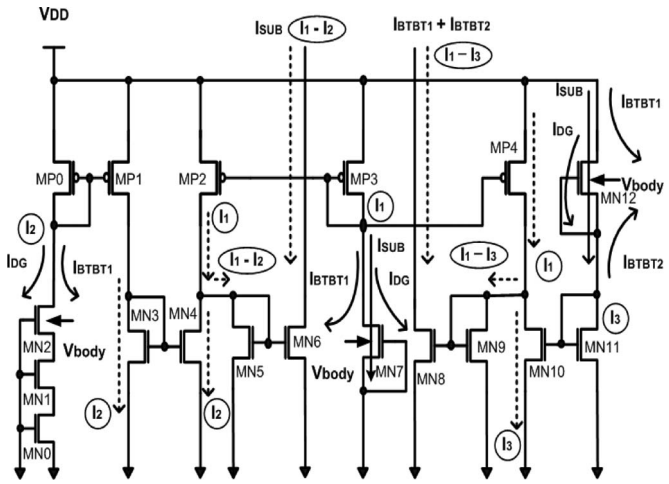

Fig. 9. Proposed leakage monitoring circuit for n-MOSFETs.

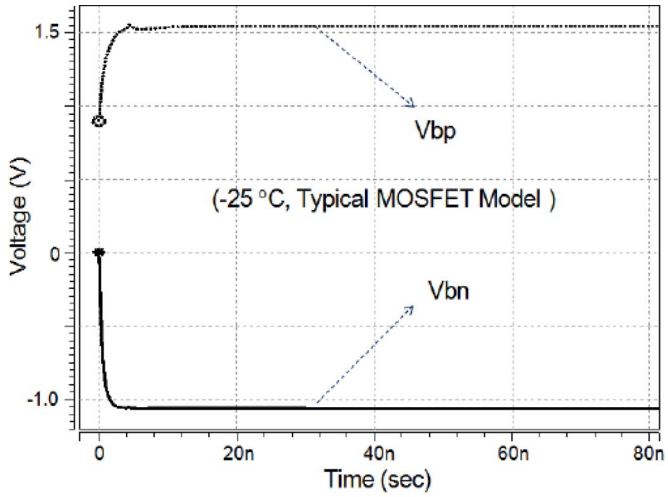

Fig. 10. Body bias voltage generated in the optimal body bias voltage controller.

In the proposed scheme, a current comparator is used to determine the optimal body bias voltage target assuming the power supply is regulated outside the chip. The body bias voltages for n-MOSFET and p-MOSFET are automatically set by the control system to ensure that the chip dissipates minimal power in standby mode. The proposed scheme uses the current-mode circuit technique to process the active signals in the current domain, and it offers a number of advantages, such as better sensitivity, high speed, and low-power dissipation. Since the circuits used in the proposed scheme are fully analog circuits, and the feedback loop continuously works, no control circuits are required. This is one of the main advantages of the proposed approach.

The leakage monitoring circuit separates the subthreshold leakage $(I_{\rm SUB})$ and the BTBT leakage current $(I_{\rm BTBT1,2})$ from the total leakage components. Fig. 9 shows a new leakage monitoring circuit for n-MOSFETs, where the transistors of MN2, MN7, and MN12 are the replica transistors to generate leakage components, and MP0/MP1, MP2/MP3, and MN10/MN11 form current mirrors.

By using triple off-transistors in a stack, the subthreshold current flowing from drain to source of the MN2 transistor can be ignored. Therefore, the amount of drain current of the MN2 transistor denoted as I_2 is approximately the same as the sum of $I_{\rm DG}$ and $I_{\rm BTBT1}$. The drain current of MN7, which is denoted as I_1, consists of $I_{\rm DG}$, $I_{\rm BTBT1}$, and $I_{\rm SUB}$. In the source of the MN12 transistor, the current I3 consisting of $I_{\rm DG}$, $I_{\rm BTBT2}$, and $I_{\rm SUB}$ is generated. The leakage monitoring circuit for p-MOSFETs is made up with the same structure as the monitoring circuit for n-MOSFETs.

Two current differential amplifiers are employed based on the generated leakage components. $I_{\rm SUB}$ (current I_1–current I_2) is obtained through MN4, MN5, and MN6 transistors, whereas $I_{\rm BTBT} = I_{\rm BTBT1} + I_{\rm BTBT2}$ (current I_1–current I_3) is obtained through MN8, MN9, and MN10 transistors.

The separated leakage components are applied to the current comparator to generate a pulse width proportional to the magnitude of each leakage. The current comparator is designed using the current mirrors, as shown in Fig. 11, where MN6 and MN8 in the leakage monitoring circuit are connected to the current comparator. The current comparator offers good sensitivity, high speed, and low-power dissipation. In Fig. 11, the comparator compares a current I_1 and a current I_3 with a current I_2 and a current I_4, respectively: I_1 and I_4 are generated by $I_{\rm BTBT}$, and I_2 and I_3 are generated by $I_{\rm SUB}$. There are three modes of operation of the current comparator.

1) If $I_{\rm BTBT} = I_{\rm SUB}$, $I_1 = I_2$, and $I_3 = I_4$, then $I_5 = I_6 = 0$, maintaining the body-bias voltage.
2) If $I_{\rm BTBT} > I_{\rm SUB}$ and $I_1 > I_2$, then $I_6 > 0$, charging the output capacitor of the charge pump and increasing the body bias voltage.
3) If $I_{\rm BTBT} < I_{\rm SUB}$ and $I_3 > I_4$, then $I_5 > 0$, discharging the output capacitor of the charge pump and decreasing the body bias voltage.

The charge pump discharges or charges its output capacitor, depending on two signals from the current comparator and its own bias voltage. The final output stage consists of an op-amp and a buffer. The current comparator-based circuit provides the optimal body bias voltage to match the subthreshold leakage with the BTBT leakage currents. The body-bias voltages for n-MOSFETs or p-MOSFETs are changed to the optimal body points within 10 ns, as shown in Fig. 10. In this paper, we concentrate on the N-MOSFET leakage current minimization based on an N-well P-type substrate process.

If the process is a P-well N-type substrate process, then the circuits that generate the optimum body bias voltage is complementary of the circuits shown in Figs. 9 and 11. The range of the body biasing voltage in this paper is between -0.9 and 0 V, and the sign of the $V_{\rm Body}$ is easily inverted before $V_{\rm Body}$ is applied to the substrate. Therefore, $V_{\rm DD}$ and $V_{\rm SS}$ are same for the whole system in this case.

V. Experimental Results

The proposed optimal $V_{\rm Body}$ control system using 32-nm MOSFET technology was implemented and evaluated using ISCAS85 benchmark circuits designed in the same technology. Table I shows the summary of the results for the proposed approach at different operating temperature ranges, i.e., from 25 °C to 100 °C. Analysis of the results shows that the maximum of 1491× reduction in leakage power is achieved from

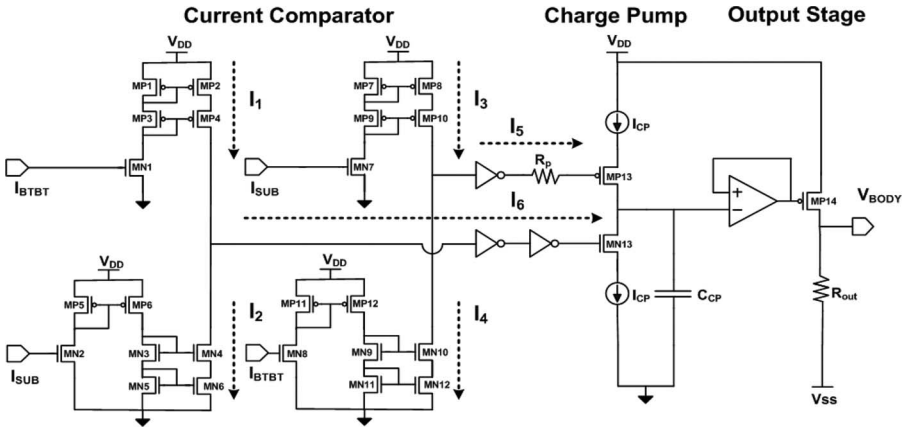

Fig. 11. Schematic of the proposed V_{Body} control system.

TABLE I
EXPERIMENTAL RESULTS FOR STANDBY LEAKAGE POWER

Circuit	# of gates	Function	Leakage(μW):Temperature=25°C		
			Zero Body Bias	*Optimal Body Bias*	*% of Reduction*
C432	160	27-channel interrupt controller	5.880	0.013	452.31%
C499	202	32-bit SEC circuit	14.415	0.030	480.50%
C1908	880	16-bit SEC/DED circuit	14.997	0.040	374.93%
C1355	546	32-bit SEC circuit	21.488	0.039	551.00%
C5315	2307	9-bit ALU	49.687	0.125	397.50%
Circuit	**# of gates**	**Function**	**Leakage(μW):Temperature=100°C**		
			Zero Body Bias	*Optimal Body Bias*	*% of Reduction*
C432	160	27-channel interrupt controller	14.200	0.012	1183.33%
C499	202	32-bit SEC circuit	36.761	0.036	1021.14%
C1908	880	16-bit SEC/DED circuit	35.641	0.043	828.86%
C1355	546	32-bit SEC circuit	53.703	0.036	1491.75%
C5315	2307	9-bit ALU	119.260	0.135	883.41%

the proposed method. Table I confirms the simulation results of each benchmark circuit at different temperatures.

The power consumption of the optimal body voltage generator circuit is 41 μW at the same power supply voltage (0.9 V) as the core power supply, which is very small compared with the power consumption of the general digital cores. Therefore, it makes sense to utilize the proposed technique only for the case where the core power is large enough to ignore the power overhead.

The optimal body bias is also adjusted according to the temperature variations in the proposed approach, and the results demonstrate that the leakage power of the proposed circuit is far less sensitive to temperature variations.

The experimental results demonstrate that the proposed system is very effective and viable in reducing the standby power in big circuits with minimal hardware overhead and minimal power overhead.

VI. CONCLUSION

As the technology scaling goes down below 90 nm, the standby leakage power dissipation has become a critical issue. Therefore, the new circuit design technique for minimizing the leakage power must be developed along with the device scaling.

To reduce the standby leakage power, this paper has presented a novel design technique that generates the optimal V_{Body} scaling during standby mode. By monitoring the BTBT leakage current (I_{BTBT}) and the subthreshold leakage current (I_{SUB}), the optimal body-bias voltage is automatically generated and continuously adjusted by the control loop. By tuning the body bias voltage using the leakage-monitoring circuit, the circuit can be biased at the optimal point where the subthreshold leakage current and the BTBT leakage current are balanced to accomplish the minimum leakage power. The results show that the proposed control system is a viable solution for high-energy reduction in nanoscale CMOS circuits.

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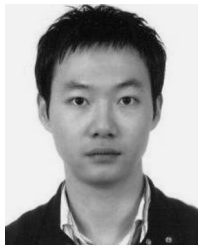

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