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Extended Operation of Flying Capacitor Multilevel Inverters

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***Abstract*—Recent research in flying capacitor multilevel inverters (FCMIs) has shown that the number of voltage levels can be extended by changing the ratio of the capacitor voltages. For the three-cell FCMI, four levels of operation are expected if the traditional ratio of the capacitor voltages is 1:2:3. However, by altering the ratio, the inverter can operate as a five-, six-, seven-, or eight-level inverter. According to previous research, the eight-level case is referred to as maximally distended (or full binary combination schema) since it utilizes all possible transistor switching states. However, this case does not have enough per-phase redundancy to ensure capacitor voltage balancing under all modes of operation. In this paper, redundancy involving all phases is used along with per-phase redundancy to improve capacitor voltage balancing. It is shown that the four- and five-level cases are suitable for motor drive operation and can maintain capacitor voltage balance under a wide range of power factors and modulation indices. The six-, seven-, and eight-level cases are suitable for reactive power transfer in applications such as static var compensation. Simulation and laboratory measurements verify the proposed joint-phase redundancy control.**

***Index Terms*—Converter, flying capacitor, inverter, multilevel, rectifier, voltage balancing.**

I. Introduction

In RECENT years, there has been considerable development in multilevel power conversion, especially for application to medium-voltage drives. The flying capacitor multilevel inverter (FCMI) topology [1]–[6] is relatively new compared to the diode-clamped [7]–[9] and series H-bridge [10], [11] inverters. Although the FCMI is not as common, it has some distinct advantages over the diode-clamped topology including the absence of clamping diodes and the ability to regulate the flying capacitor voltages through redundant state selection even if the number of voltage levels is greater than three [5]. Unlike the series H-bridge inverter, isolated voltage sources are not required. Considering these advantages, the FCMI is finding many practical applications in industry [2].

The reason that capacitor voltage balancing is not an issue in the FCMI is that there are several conduction paths within each phase that can produce the same voltage levels. This per-phase redundancy can be used to choose the path with the best balancing characteristics at any point in time. It is possible to change the ratio of capacitor voltages and sacrifice this redundancy in order to improve the power quality by increasing the number of voltage levels [3]. However, some of the redundant states are then not available for capacitor balancing. Therefore, a tradeoff between power quality and capacitor voltage balancing can be established. In this paper, a three-cell flying capacitor inverter is used to exemplify this tradeoff. The typical four-level performance is extended to five-, six-, seven-, and eight-level. The loss in capacitor voltage balancing control is compensated by using joint redundancy involving all phases (in effect adjusting the common-mode line-to-ground voltage). It is shown that five-level operation can be used for motor drive applications, while six-, seven- and eight-level operation can be used for applications involving reactive power compensation.

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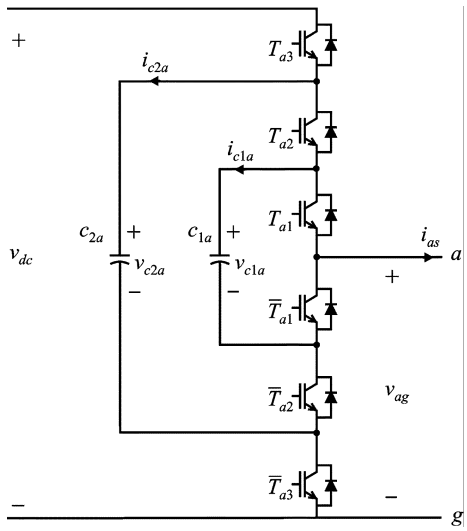

Fig. 1. Three-cell FCMI inverter topology (a-phase).

II. Extended Flying Capacitor Inverter

Fig. 1 shows one phase of the three-cell flying-capacitor inverter topology. For this inverter, each capacitor is charged to a different voltage and by changing the transistor switching states, the capacitors and dc source are connected in different ways and produce various line-to-ground output voltages. For the analysis presented herein, the line-to-ground voltage and capacitor currents are of interest. From the topology KVL and KCL equations, these quantities can be expressed as

$$v_{ag} = (T_{a3})v_{dc} + (T_{a2} - T_{a3})v_{c2a} + (T_{a1} - T_{a2})v_{c1a} \quad (1)$$

$$i_{c1a} = (T_{a2} - T_{a1})i_{as} \quad (2)$$

$$i_{c2a} = (T_{a3} - T_{a2})i_{as}. \quad (3)$$

Based on these fundamental equations, the line-to-ground voltage and capacitor currents can be determined for all combinations of transistor signals as shown in Table I.

TABLE I
THREE-CELL FCMI OUTPUT VOLTAGES

T_{a1}	T_{a2}	T_{a3}	v_{ag}	i_{c1a}	i_{c2a}
0	0	0	0	0	0
0	0	1	v_{dc}- v_{c2a}	0	i_{as}
0	1	0	v_{c2a}- v_{c1a}	i_{as}	- i_{as}
0	1	1	v_{dc}- v_{c1a}	i_{as}	0
1	0	0	v_{c1a}	- i_{as}	0
1	0	1	v_{dc}- v_{c2a}+ v_{c1a}	- i_{as}	i_{as}
1	1	0	v_{c2a}	0	- i_{as}
1	1	1	v_{dc}	0	0

TABLE II
THREE-CELL FCMI OUTPUT VOLTAGES WITH DIFFERENT RATIOS

T_{a1}	T_{a2}	T_{a3}	E:2E:3E	E:2E:4E	E:3E:5E	E:3E:6E	E:3E:7E
0	0	0	0	0	0	0	0
0	0	1	E	2 E	2 E	3 E	4 E
0	1	0	E	E	2 E	2 E	2 E
0	1	1	2 E	3 E	4 E	5 E	6 E
1	0	0	E	E	E	E	E
1	0	1	2 E	3 E	3 E	4 E	5 E
1	1	0	2 E	2 E	3 E	3 E	3 E
1	1	1	3 E	4 E	5 E	6 E	7 E
			four-level	five-level	six-level	seven-level	eight-level

As with other inverter topologies, the three-phase implementation involves three branches of the structure shown in Fig. 1 connected in parallel on the dc side and typically connected to a wye-configured load on the ac side. Since the load neutral may not be accessible, the line-to-line voltages may be of interest and can be expressed in terms of the line-to-ground voltage by [3]

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \tag{4}$$

The load's line-to-neutral voltages can also be determined directly from the line-to-ground voltages using [3]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \tag{5}$$

From Table I, it can be seen that the line-to-ground voltage depends on the values of v_{c1a}, v_{c2a}, and v_{dc}. By changing the ratio of these voltages, it is possible to alter the number of voltage levels that the inverter can produce. This concept was previously introduced for the FCMI topology as well as combinational "hybrid" topologies [12], [13]. Table II shows the line-to-ground voltage for several different dc voltage ratios. Therein, each column represents a different ratio listed as $(v_{c1a} : v_{c2a} : v_{dc})$, and examples of four-, five-, six-, seven-, and eight-level cases are shown. It should be pointed out that these are only a small collection of voltage ratios and other ratios exist which will yield four-, five-, six-, seven-, and eight-level operation. A computer simulation was performed considering every possible voltage ratio in order to determine which ratios are best in terms of capacitor voltage ripple and switching loss. Table II contains the set of ratios which had the best performance for the specific number of voltage levels.

From Table II, it can be seen that there is considerable redundancy for the four-level case; having three possibilities for both intermediate levels E and $2E$. Although the redundant states have the same output voltages, they have different effects in terms of the capacitor currents. Therefore, a straightforward choice can be made which will improve the capacitor balance situation when the E or $2E$ level is required. For the five-level case, there is redundancy for all intermediate levels. However, it turns out that there is not enough redundancy to regulate the capacitor voltages. This problem will be solved by considering joint redundancy among all phases in a later section. As the number of voltage levels increases, the amount of redundancy goes down. For the eight-level case, each switching state has a unique voltage level and so there is no per-phase redundancy available.

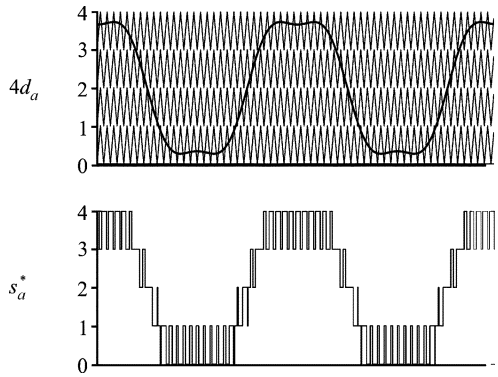

Fig. 2. Five-level triangle modulation.

III. MULTILEVEL VOLTAGE-SOURCE MODULATION

Voltage-source modulation can be accomplished in a multilevel inverter system using the sine-triangle method [7]. The first step is to define duty cycles for each phase as [14], [15]

$$d_a = \frac{1}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \tag{6}$$

$$d_b = \frac{1}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{7}$$

$$d_c = \frac{1}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{8}$$

where θ_c is the electrical angle which could be related to commanded frequency f^* by

$$\theta_c = \int_0^t 2\pi f^* dt \tag{9}$$

and m represents the modulation index which has a range from 0 to 1.15 [14], [15]. The three duty cycles are compared to a set of triangle waveforms to produce commanded switching states for each phase. As an example, Fig. 2 demonstrates the generation of the switching state for the a-phase. Therein, the a-phase commanded switching state s_a^* is the number of triangle waveforms that the duty cycle is above. Incidentally, in a digital signal processor (DSP) implementation, there is an alternate method of producing the switching states which uses state machine timers instead of triangle waveforms [15]. The output of the modulator is input to a capacitor balancing control described in the following sections.

IV. Capacitor Voltage Balancing Method

In order to obtain reasonable distinct multilevel output voltage results, the voltages on all six capacitors (two per phase) must be maintained at constant values. However, the load currents have different effects on the charging and discharging of the capacitors and will tend to unbalance the capacitor voltages. In this case, the redundant switching states become the key component for balancing the capacitor voltages.

Since there are several conduction paths within each phase which can produce the same voltage levels while having different capacitor charging characteristics, per-phase redundancy can be used to choose the path with the best balancing performance. However, according to Table II, as the number of achieved voltage levels increases, the number of available per-phase redundant states decreases. In this case, incrementing or decrementing the switching states of all three phases s_a^*, s_b^* and s_c^* can also be used to balance capacitor voltages since this results in changes in the zero-sequence line-to-ground voltage, which does not affect the load voltages according to (4) and (5). The concept behind this joint-phase redundant state selection (JRSS) method is that the line-to-ground voltages (v_{ag}, v_{bg}, v_{cg}) of all phases may be changed simultaneously without affecting the load voltages since the terms that are common in all phases will cancel when looking at the line-to-neutral voltages (v_{as}, v_{bs}, v_{cs}) or line-to-line voltages (v_{ab}, v_{bc}, v_{ca}). For example, the state involving (v_{ag} =0, $v_{bg} = E$, $v_{cg} = E$) could be changed to ($v_{ag} = E$, $v_{bg} = 2E$, $v_{cg} = 2E$) or ($v_{ag} = 2E$, $v_{bg} = 3E$, $v_{cg} = 3E$) or ($v_{ag} = 3E$, $v_{bg} = 4E$, $v_{cg} = 4E$). Because the corresponding load voltages are the same for each of these cases, the selection of the appropriate joint state can improve the capacitor balancing situation. In this paper, two joint-phase redundant state selection algorithms are introduced as described in the following sections.

A. On-Line Joint-Phase RSS

In general, this JRSS algorithm works as follows. For any desired three phase switching states s_a^*, s_b^* and s_c^*, all available redundant states, which can produce the same load voltages are evaluated and compared. These states include joint-phase redundant states and per-phase redundant states. The number of joint-phase redundant states N_{JRSS} can be expressed by

$$N_{\mathrm{JRSS}} = n - [\mathrm{MAX}(s_a^*, s_b^*, s_c^*) - \mathrm{MIN}(s_a^*, s_b^*, s_c^*)] \quad (10)$$

where n is the number of voltage levels. The first joint-phase redundant state to be considered can be obtained from

$$s_{Jx}^* = s_x^* - \mathrm{MIN}(s_a^*, s_b^*, s_c^*) \quad (11)$$

where x is the phase (a, b, or c). The other states are obtained by adding 1 to all three phases until all redundant states are evaluated. The number of per-phase redundant states N_{PRSSx} is related to the ratio of the capacitor voltages. Table III shows an example in a five-level inverter when the capacitor voltage ratio is set to 1:2:4.

Each combination of redundant states will be evaluated in the following way. First, assuming that phase currents do not change during one DSP switching period T_s (which is valid when the switching frequency is high), each switching period can be split into four windows [15]. The predicated capacitor voltage change during one window time can be calculated as

$$\Delta v_{cyx} = \frac{i_{cyx} \cdot t_{\mathrm{window}}}{C_y} \quad (12)$$

where x is the phase (a, b, or c), y is the capacitor (1 or 2), t_{window} is the time for one window. The capacitor currents i_{cyx} are determined from phase current sensors and the inverter switching path according to (2) and (3). The predicted capacitor voltages for the next window are determined as

$$\tilde{v}_{cyx} = v_{cyx} + \Delta v_{cyx}. \quad (13)$$

The square error for each potential state is evaluated by comparison to ideal voltages as

$$\varepsilon = \sqrt{\sum_{x=a}^{c} \sum_{y=1}^{2} \left(v_{cyx}^* - \tilde{v}_{cyx}\right)^2} \quad (14)$$

and the state with the least error is chosen. This process is repeated and (12)–(14) are evaluated every time when the commanded switching states are changed. Fig. 3 shows the detailed flow chart of implementation. This algorithm minimizes the error between capacitor voltages and their ideal values, and thus gives the best possible choice to improve the overall balancing of voltages of the six capacitors.

TABLE III
Number of Per-Phase Redundant States in a Five-Level Inverter (1:2:4)

s_a^*	N_{PRSSa}	(T_{a1} T_{a2} T_{a3})
0	1	(0 0 0)
1	2	(0 1 0), (1 0 0)
2	2	(0 0 1), (1 1 0)
3	2	(0 1 1), (1 0 1)
4	1	(1 1 1)

B. Look-Up Table Joint-Phase RSS

This algorithm follows multilevel modulation by a redundant state selection table for capacitor voltage balancing. The procedure of how to form this table is similar with the on-line JRSS method except the evaluation part.

The inputs (address) of the table are the commanded switching states from the modulator as well as digital flags representing the state of the system. This method requires that the direction of the three-phase load currents be known. Then the direction of capacitor currents can be determined considering transistor switching state according to (2) and (3). Let F_{iyx} represent the capacitor current direction flag, which equals to 1 for positive current and 0 for negative current. These flags are used to determine whether a choice is improving or impairing the capacitor balancing situation. Let F_{vyx} represent the capacitor voltage flag, which is defined as

$$F_{vyx} = \begin{cases} 1, & v_{cyx} \geq v_{cyx}^* \\ 0, & v_{cyx} < v_{cyx}^* \end{cases} \quad (15)$$

to show if the capacitor is overcharged or undercharged.

Since there are two capacitors in one phase, for each switching state, its overall effect on six capacitors should be considered. To take into account different balancing effects on

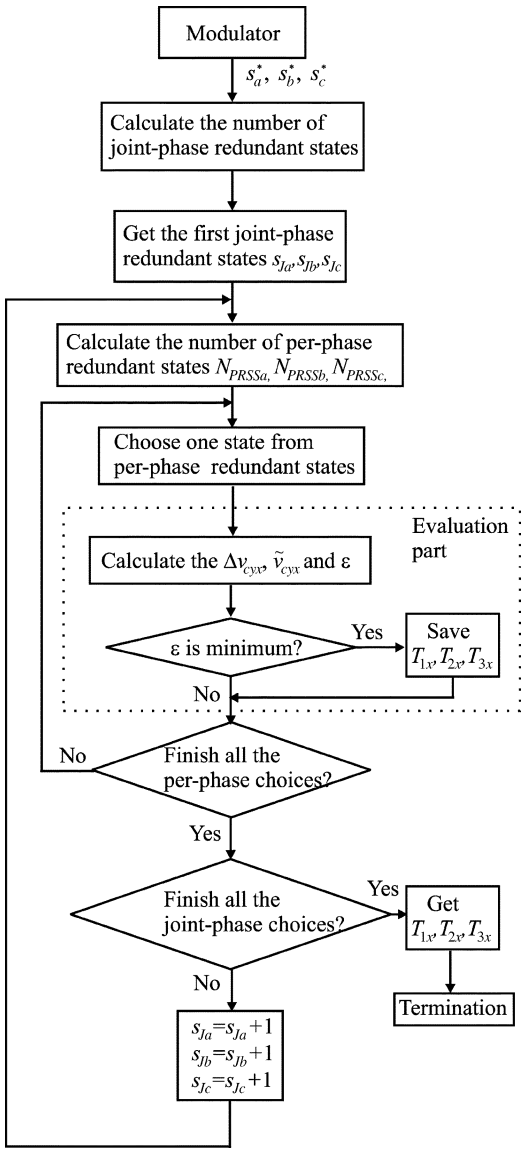

Fig. 3. Flow chart of on-line joint-phase RSS method.

all the capacitors, four more flags are used. The same-phase capacitor priority flag $F\Delta_{cx}$ tells which one of the two capacitors in the same phase need to be balanced first defined as

$$F\Delta_{cx} = \begin{cases} 0, & \frac{ABS(v_{c1x}-v_{c1x}^*)}{v_{c1x}^*} \geq \frac{ABS(v_{c2x}-v_{c2x}^*)}{v_{c2x}^*} \\ 1, & \frac{ABS(v_{xc1}-v_{xc1}^*)}{v_{c1x}^*} < \frac{ABS(v_{c2x}-v_{c2x}^*)}{v_{c2x}^*}. \end{cases} \quad (16)$$

Herein, relative deviations were used because the goal of the capacitor voltage balancing was to keep the capacitor voltages close to their nominal values. However, absolute deviations can also be used where the capacitors are treated equally for the same amount of voltage deviations. The all-phase capacitor priority flag $Ind\Delta_c$ tells which capacitor in six capacitors should be balanced first, and is determined by choosing the one capacitor with the maximum voltage deviation.

With the desired switching states and all the above flags available, a balancing performance priority is chosen to describe the capacitor charging and discharging characteristics of each state. The following principles are employed.

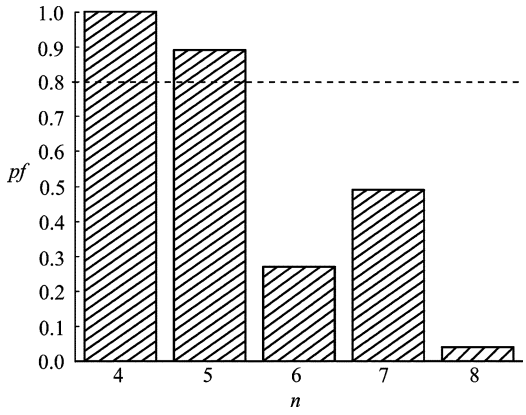

Fig. 4. Maximum power factor versus number of levels.

- If the capacitor current direction is positive (out of capacitor) and the capacitor is overcharged, this redundant state will help regulate the capacitor voltage. Similarly, if the current direction is negative and the capacitor is undercharged, the redundant state will also help regulate the capacitor voltage. These redundant states will be given a high priority P_h.
- When the capacitor current tends to unbalance the capacitor voltages, a low priority of $P_l = 0$ will be provided.
- When the capacitor current is zero, a medium priority P_m is given.

In order to reduce the size of the table and simplify implementation, the algorithm can be divided into two steps. The first step focuses on the capacitor which should be balanced first of all six capacitors, with the current direction flag and capacitor voltage flag of this capacitor. From all possible redundant states considering joint-phase redundant states, the one which can help balancing best by the above principle is chosen. If there are two possibilities with the same effect on balancing, the one which can help the other capacitor in the same phase is chosen. After obtaining the redundant states for this phase, the redundant states for the other two phases are easy to find.

With the updated switching states, the conduction paths for transistor can be determined by considering only per-phase redundant states. The flag $F\Delta_{cx}$ tells which one of the two capacitors in each phase has a higher priority. Different values of P_h and P_m are assigned to capacitors of high and low priorities. For high priority capacitors, $P_h = 6$ and $P_m = 3$, while for low priority capacitors, $P_h = 2$ and $P_m = 1$. The value of P_l is always 0.

The performance index for each per-phase redundant state can then be calculated as the sum of priority indices (P_h, P_m, or P_l) of the two capacitors in the same phase. The switching state with the highest performance priority is then selected. The performance indices for each switching state in all possible situations are pre-calculated and compared so that the best state can be obtained directly from a table based on the digital flags.

C. Operating Modes of the Distended FCMI

The proposed algorithms were evaluated through detailed simulation. The JRSS method works better for lower modulation indices since that leads to more available joint states. As a worst-case analysis, consider the results of Fig. 4. Therein, the

modulation index is set to a maximum and the maximum power factor (without loosing capacitor voltage balance) is shown for the various numbers of levels for the three-cell FCMI. From Fig. 4, it can be seen that the four-level case will maintain balance under all circumstances. The five-level will work for power factors up to 0.89 lagging. This makes the five-level suitable for motor drives where the power factor is typically below 0.8 lagging at full modulation index. For six- seven- and eight-level operation, capacitor voltage balance is only possible for lower power factors. In this case, this performance is only achievable for reactive power applications such as static var compensation.

V. Proposed Inverter Performance

In this section, the extended FCMI inverter operation is compared to the traditional FCMI operation in terms of switching losses, commanded common-mode voltage, and capacitor size. Advantages and limitations of the proposed scheme are evaluated using detailed computer simulation.

A. Switching Losses

The traditional flying-capacitor multilevel inverter employs three cells to produce four output voltage levels. With the same number of cells, the proposed control can extend the operation to produce five, six, seven, and even eight levels, while keeping the capacitor voltages balanced. With more voltage levels, the system total harmonic distortion (THD) and output filter size can be greatly reduced, which results in more compact system design and lower costs. The number of levels is extended by changing the voltage ratio which means that the device voltage pairs will have different voltages (whereas all devices block the same voltage when the traditional voltage ratio is used). Besides the different voltage ratings, the proposed control uses joint-phase RSS instead as well as per-phase RSS (whereas the traditional control uses only per-phase RSS). The use of per-phase and joint-phase redundant state selections for capacitor balancing makes the commutations between adjacent levels require more than one single device pair so the switching pattern is not optimized for minimal switching losses. To compare the switching losses of the proposed control to the traditional method five-level inverter system was used in the base simulation. The inverter was simulated using 1200-V, 50-A IBGT/diode dual modules which have the properties $V_{ce,sat} =$ 3.3 V, $V_{d,sat} = 3.0$ V, $E_{on} = 6.94$ mJ, $E_{\text{off}} = 8.72$ mJ, and $E_{rr} = 3.33$ mJ, and 600-V, 50-A IBGT/diode dual modules which have the properties $V_{ce,sat} = 2.8$ V, $V_{d,sat} = 3.0$ V, $E_{on} = 1.36$ mJ, $E_{\text{off}} = 3.14$ mJ, and $E_{rr} = 0.429$ mJ. The dc voltage was set to 1200-V and the PWM clock frequency was set to 5 kHz. An R–L load was placed on the inverter operating with 40-kVA, 32-kW, and 60-Hz. Both the traditional four-cell FCMI and the proposed three-cell FCMI with voltage ratio of 1:2:4 simulated. The results showed that the switching losses increase from 83-W to 113-W when using the proposed control. It can be seen that a small amount of switching losses are sacrificed in order to balance the flying capacitors. However, due to the absence of one pair of transistors, the conduction losses decreased from 435-W to 309-W. Overall the efficiency of proposed method is slightly higher that the efficiency of traditional method.

TABLE IV
Induction Machine Ratings and Parameters

$poles = 4$	$phases = 3$
$V_{LL,rated} = 230$ V	$I_{L,rated} = 12.5$ A
$f_{rated} = 60$Hz	$pf_{rated} = 0.75$
$P_{rated} = 3.7$ kW	$\omega_{rm,rated} = 183.2$ rad/s
$r_s = 0.21\ \Omega$	$L_{ls} = 1.43$ mH
$r_r' = 0.113\ \Omega$	$L_{lr}' = 2.58$ mH
$M = 36$ mH	

B. Commanded Common-Mode Voltage

The traditional FCMI control utilizes per-phase RSS for capacitor voltage balancing and is therefore invariant to the commanded common-mode line-to-ground voltage. For the simulation and lab experiments in the sections below, a third harmonic commanded voltage is used, as per (6)–(8), so that the maximum modulation index may be commanded in the modulator. However, the JRSS method alters the common-mode line-to-ground and it ultimately depends on the capacitor voltage balancing. This brings up the question of whether the commanded common-mode voltage will affect the states which are selected by the JRSS method and in turn affect the capacitor voltage balancing. To investigate this possibility several common-mode voltages were simulated in the modulator including continuous SPWM method and discontinuous DPWM1, DPWM2, DPWM3, DPWMMIN, DPWMMAX methods [16]. Through these detailed simulations, it was found that there was no significant differences in capacitor voltage balancing, capacitor voltage ripple, or switching losses using various common-mode voltages.

C. Capacitor Size

A detailed simulation was used to compare the capacitor size of the proposed inverter with that of a traditional FCMI. For a base comparison, the five-level case was chosen. The traditional solution uses a four-cell FCMI structure with dc voltage ratios of (1:2:3:4) whereas the extended FCMI uses a three-cell structure with a dc voltage ratio of (1:2:4). In this study, the total dc voltage was set to 600-V and the dc link capacitor was set to 750 μF (a typical size considering the ac load current). By selecting standard sizes, the traditional method uses 1000-μF 150-V, 470-μF 300-V, and 330-μF 450-V capacitors per phase in order to ensure each capacitor has a voltage ripple of less than 2%. The proposed method requires a 1000-μF 150-V and a 1500-μF 300-V capacitor in each phase to ensure the same voltage ripple. According to the datasheets, the traditional method requires flying capacitors that have a volume of 97.1% of the dc link capacitance whereas the proposed method uses flying capacitors with a volume of 171.9% of the dc link capacitor. This increase in capacitor volume comes from an increase in the rms current due to the JRSS switching. Another aspect to consider is that the proposed method uses six IGBTs instead of eight. When the volume of the added IGBTs is considered, the proposed method has a slightly smaller volume and the overall cost is roughly the same. Furthermore, the added IGBTs in the traditional method will also require added heat sinks and added gate drive circuitry.

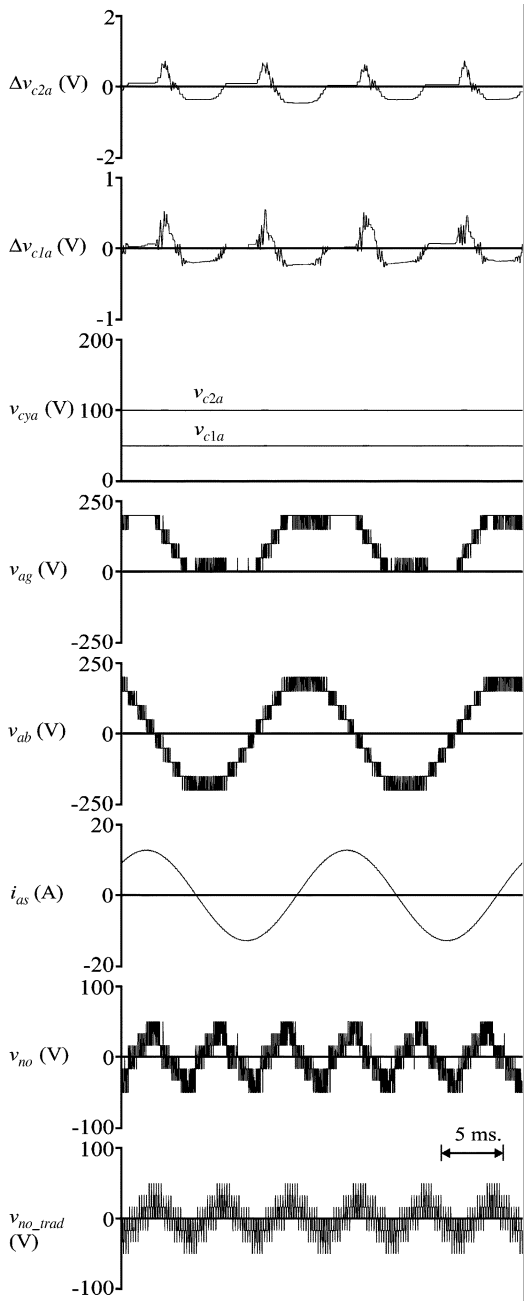

Fig. 5. Five-level steady-state operation.

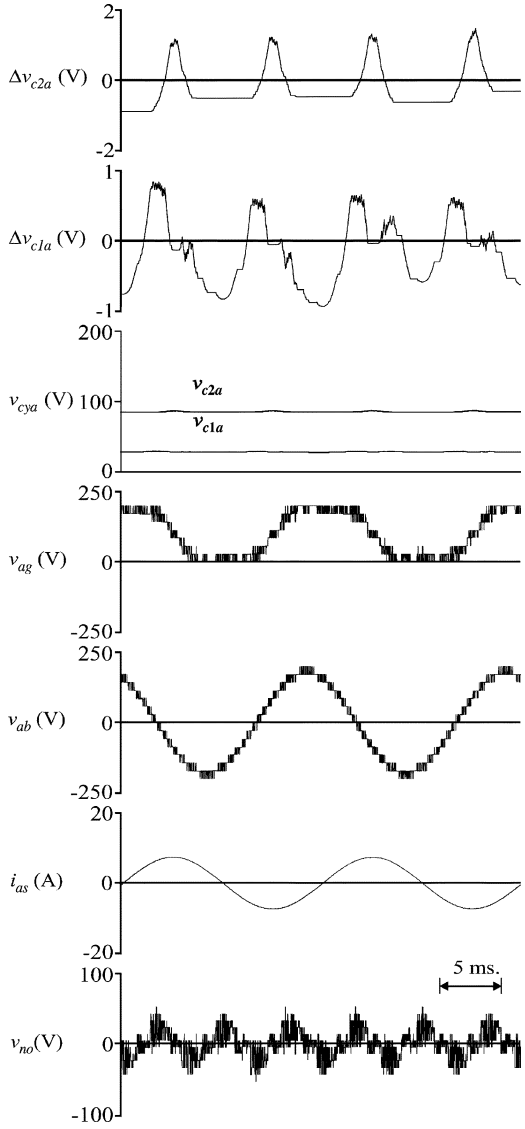

Fig. 6. Eight-level steady-state operation.

VI. Computer Simulation Results

A. Steady-State Study

A computer simulation has been created to verify the proposed method. In this simulation, a three-phase induction motor with parameters [17] showed in Table IV is connected to the inverter as a load. The dc voltage is set to $v_{dc} = 200$ V. The capacitance values of the capacitors are $C_{1x} = C_{2x} = 3300$ μF and the commanded fundamental frequency f^* is 60 Hz.

For the first study, the ratio of capacitor voltages is set to 1:2:4 to obtain five level steady-state operation. The modulation index is near maximum value 1.14. The motor runs with commanded rotor speed of 186.6 rad/s and a load torque of 8 $N \cdot \mathrm{m}$. Fig. 5 shows the capacitor voltage deviations, capacitor voltages v_{c1a}, v_{c2a}, a-phase line-to-ground voltage v_{ag}, line-to-line voltage v_{ab} and motor current i_{as}, As can be seen, capacitor voltages are maintained at a fairly constant level with $v_{c1a} = 50$ V and $v_{c2a} = 100$ V, which satisfies the ratio requirement. The capacitor voltage deviations jump around 0 V, the voltage ripple for each capacitor is around 2%. The capacitor voltage balance can also be seen in that the line-to-ground voltage has five distinct levels. The effect of JRSS is seen in the bus clamping of the line-to-ground voltage v_{ag} to the highest and lowest levels. However, since the line-to-ground voltages of the other phases are also changed at the same time, the line-to-line voltages are not affected. From the line-to-line voltages, the effective nine-level waveform can be seen (four positive levels, four negative levels, and one zero-level). Also, the resulting sinusoidal current lags the output voltage by 41° making the power factor $pf = 0.75$. The last traces in Fig. 5 are the common-mode (line to dc link midpoint) voltages for the extend FCMI and a traditional FCMI operating under the same conditions. By comparison, it can be seen that the extended FCMI has the same common-mode voltage level steps, but at a higher frequency due to JRSS capacitor voltage balancing. This is a drawback of the

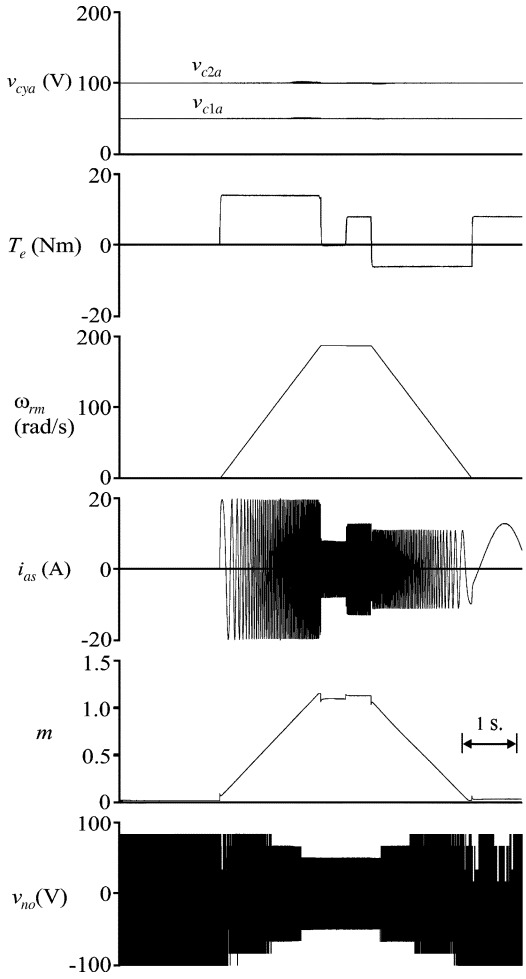

Fig. 7. Five-level dynamic motor drive operation.

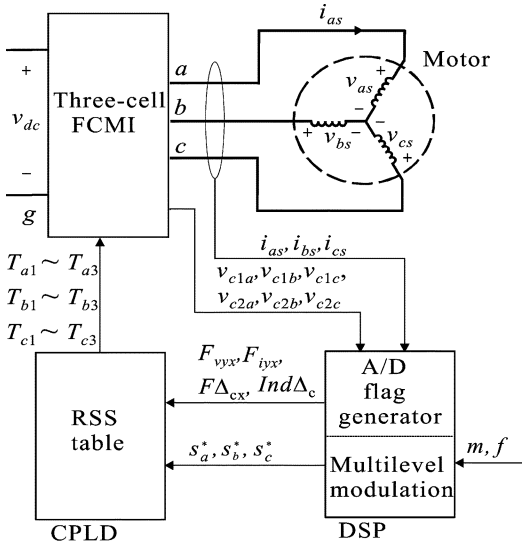

Fig. 8. Five-level inverter implementation.

proposed method since higher frequency common-mode voltages could lead to higher frequency common-mode currents.

Fig. 6 shows eight-level operation with the same variables as the five-level operation study. In this case, the ratio of capacitor voltage is set to 1:3:7, which corresponds the capacitor voltage $v_{c1a} = 28.6$ V and $v_{c2a} = 85.7$ V shown in the figure. To lower the power factor, the induction motor speed was set to the no-load value of 188.5 rad/s. Again, capacitor balance is evident considering the even levels of v_{ag} and v_{ab}. The line-to-ground voltage v_{ag} demonstrate the effectiveness of the redundant state selection. The line-to-line voltage v_{ab} waveform exhibits high power quality with fifteen voltage levels. The current lags the output voltage by approximately 90° since the slip is set close to 0.

B. Dynamic Studies

Motor drive operation performance is shown in Fig. 7. Therein, the three-cell FCMI inverter with a 1:2:4 voltage ratio drives an induction motor with vector control and an outer speed loop [18]. At the beginning of this dynamic study, the motor speed and load torque are set to zero. Two seconds later, after the machine flux has built up, the speed command is ramped up to 186.6 rad/s. A step change in load from 0 to 8 N·m is applied at 4.5 s, and then the commanded speed is lowered to zero with the load on the motor. All the other operating conditions are the same as in the steady-state operation study. In this study, capacitor voltages v_{c1a}, v_{c2a}, torque T_e, motor speed ω_{rm}, current i_{as}, and modulation index m are shown. As can be seen, the redundant state selection regulates the capacitor voltages. The motor speed ω_{rm} waveform follows the commanded speed. The torque, speed, and capacitor voltages all indicate good balance throughout this dynamic study as the modulation index and power factor change over a wide range.

VII. Laboratory Validation

In order to validate the proposed concept, a three-cell five-level FCMI inverter was constructed in the laboratory. Fig. 8 shows a block diagram of how the balancing algorithm was implemented. The modulation is programmed in a DSP which generates the desired switching states, as described above, which are labeled s_a^*, s_b^*, and s_c^*. Analog-to-digital conversion is performed on the phase current and capacitor voltages in order to determine the current direction and capacitor voltage flags. This information along with the desired switching state forms the address of the desired state in the redundant state selection table. Redundant states were calculated off-line and programmed into a complex programmable logic device (CPLD).

The ratio of the capacitor and dc source voltages was set to 1:2:4. A 3.7-kW induction motor with the same parameter in steady-state study was used as a load. The dc voltage v_{dc} was supplied from an isolated rectified three-phase source. All the other operation conditions are the same as in the five-level steady-state simulation study. Also, the same variables as in the five-level steady-state simulation study are shown in Fig. 9 for comparison. As can be seen, the voltages and currents exhibit typical five-level inverter performance. The laboratory results showed that the capacitor voltages can be regulated at $v_{c1a} =$ 50 V and $v_{c2a} = 100$ V. At steady state, the power factor of the machine was 0.753 lagging with 2.73-kW input power. The low frequency harmonics seen in the current waveform were due to induction motor saturation. Since the devices used in the simulation study do not take the drop voltages into account, there were minor discrepancy between the line-to-ground voltage and line-to-line voltage of the simulation and laboratory results.

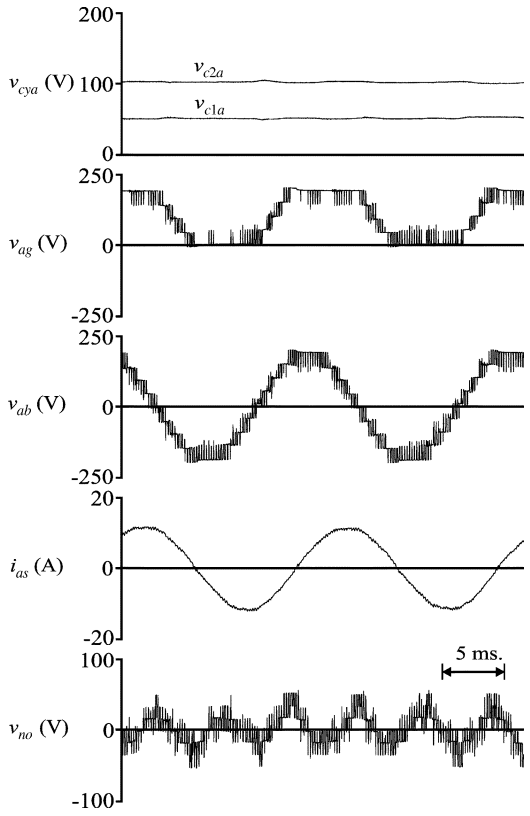

Fig. 9. Five-level inverter laboratory test results.

VIII. Conclusion

This paper has studied extended operation of a three-cell flying capacitor multilevel inverter. Redundant switching states, vital to capacitor voltage balancing, are sacrificed to achieve a higher number of output voltage levels. Two joint-phase redundant state selection algorithms were proposed to keep the capacitor voltages constant. Simulation results demonstrate the effectiveness of each algorithm. One algorithm was validated with laboratory experiments on a motor drive system. In that study, a three-cell flying capacitor inverter which typically operates in the four-level mode was extended to five-level operation. It was also demonstrated through simulation that the three-cell inverter can achieve eight-level operation for applications involving reactive power compensation.

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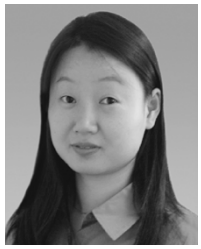

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