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A Novel Real-Time Approach to Unified Power Flow Controller Validation

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***Abstract*—This paper presents the development of a real-time hardware/software laboratory to interface a soft real-time power system simulator with multiple unified power flow controllers (UPFC) via hardware-in-the-loop (HIL) to study their dynamic responses and validate control and placement approaches. This paper describes a unique laboratory facility that enables large-scale, soft real-time power system simulation coupled with the true physical behavior of a UPFC as opposed to the controller response captured by many other real-time simulators. The HIL line includes a synchronous machine, a UPFC, and a programmable load to reproduce the physical dynamics of the UPFC sub-network.**

***Index Terms*—Real-time-simulation, unified power flow controller.**

I. Introduction

ONE of the most promising network controllers for the bulk power system is the family of power electronics-based controllers, known as "flexible AC transmission systems" (FACTS) devices. FACTS devices work by modifying power flow in individual lines of the power grid, maintaining voltage stability, and damping oscillations. The rapid development of the power electronics industry has made FACTS devices increasingly attractive for utility deployment due to their flexibility and ability to effectively control power system dynamics. The unified power flow controller, or UPFC, is the most versatile of the FACTS devices. The primary function of the UPFC is to control the transmission line power flow; the secondary functions of the UPFC can be voltage control, transient stability improvement, and oscillation damping.

Although considerable UPFC research work has concentrated on developing control strategies via simulation, there is a general lack of experimental verification of many of the proposed controls. In order to fully understand how to effectively incorporate UPFCs into existing power systems, a hardware prototype for verification is necessary in addition to software simulation. Experimental studies provide valuable data to evaluate models, test proposed control algorithms, and analyze dynamic performance. Furthermore, experimental studies provide the basis with which to predict the device performance in the actual power system operation.

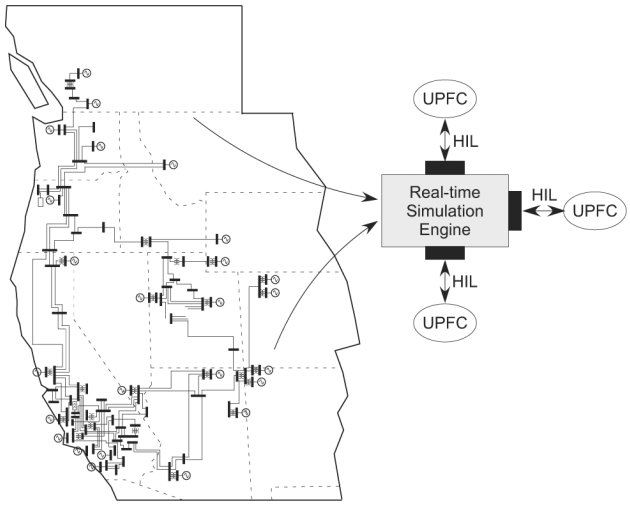

Fig. 1. Real-time hardware/software laboratory conceptualization.

Traditional software simulation has the disadvantage of being unable to exactly replicate real operational conditions. On the other hand, a small laboratory power system is not capable of fully capturing the depth and breadth of large-scale power system dynamics. One way to bridge the gap between simulation and real conditions is to combine real-time simulation and hardware-in-the-loop (HIL) [1]. The contribution of this work is the development of a hardware/software laboratory to successfully replicate both large-scale power system behavior as well as the hardware validation of the UPFC performance. This laboratory was developed to bridge the gap between system simulation with software models of the UPFC and UPFC hardware testing that typically involves only a single machine infinite bus (SMIB) system as shown in Fig. 1. This is a unique laboratory that integrates an actual hardware UPFC into a system that has more complex dynamics than the single oscillatory mode induced in an SMIB system. Furthermore, this system allows testing of any possible interactions between UPFCs.

This system was first conceptually proposed in [2]. This paper described initial efforts in developing the UPFC hardware and outlined a series of experiments that the system would make

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possible when fully deployed. The progress of the system development was updated in [3]. Reference [3] contains several flowcharts that depict information flow in the HIL system. These preliminary reports do not include the real-time simulation results of the multi-UPFC mutli-generator system presented in the current paper, nor do they discuss many of the various implementation issues required to successfully merge large-scale real-time power system simulation with multiple hardware-in-the-loop lines.

II. UPFC Real-Time Hardware/Software Laboratory

The UPFC real-time hardware/software laboratory (RTHSL) has a soft real-time simulation engine which performs nonlinear transient simulation of a large-scale power system. A soft real-time system minimizes the number of missed deadlines. The simulation engine is interfaced through the HIL to the UPFCs at their interconnection points. This approach allows the UPFCs to be easily relocated within the simulated test system and different controls to be validated. The development of the RTHSL allows researchers the unique capabilities of validating UPFC controls, placement algorithms, and analyze interactions between multiple UPFCs.

In most HIL applications, the hardware portion of the system is typically an isolated controller or component in which the interface with the real-time system is the control inputs and outputs. In the developed UPFC real-time hardware/software laboratory (RTHSL), the HIL interface is far more complex than typical HIL applications.

In an actual transmission system, the UPFC is connected in series with a transmission line and active and reactive power will flow through the series transformer windings. Therefore, the laboratory UPFC must be tested in a situation with actual active and reactive power flows. Therefore, the HIL application must include an auxiliary system for each UPFC under test to produce power flow. Furthermore, as part of a large-scale power system simulation, the active and reactive power flow in the auxiliary system is governed by the simulation and therefore must be able to communicate and be synchronized to the real-time simulation. There must be an auxiliary system for every UPFC connected into the RTHSL to reproduce the physical environment to which the UPFC responds.

III. Real-Time Simulator

With the evolution of power system simulation technology, real-time simulation is driven by the need for the applications such as online dynamic security assessment [4], dispatcher training, protection relay testing [5], FACTS, and HVDC controllers testing [6]–[8]. Several real-time simulators have been developed or are in various stages of development. Some have been developed to serve as large-scale, commercial, general-purpose simulators [5], [9], [10], while others are smaller-scaled simulators for academic environments [6], [7], [11].

The RTHSL is significantly different from commercially available real-time systems. The RTDS system (product of RTDS Technologies) is a leading real-time commercial simulator based on EMTDC/PSCAD, which is organized into individual racks of DSPs connected to each other [12], [9]. Each rack is identical and contains the necessary hardware for processing, communication, and user interface. The compiler in the RTDS produces all the parallel processing code required by the DSPs and automatically assigns jobs to the individual DSPs. The RTDS system provides full EMTP-type simulation including transmission line transients, power electronics switching dynamics, etc., but only provides HIL capabilities for testing protective relay systems and FACTS control settings. There is no direct interface from the RTDS to control actual active and reactive power flow through a UPFC. Because of the real-time simulation detail, a single RTDS module is constrained to a system size of only a moderate number of system buses, and large-scale system simulation requires additional modules. Therefore, in order to simulate large-scale power systems, numerous racks are required, making the cost of simulation very expensive.

In [5], a hybrid simulator (a combination of analog and digital) is developed and used for testing digital EHV-line relays. The developed simulator has the flexibility of modeling FACTS and HVDC converters digitally by computer simulation or analog by physical simulation with original converter controllers. This simulator has the disadvantage of being able to simulate only a limited number of power system buses.

The RTHSL is not intended to replicate the abilities of the RTDS or other real-time simulations, but rather to complement these systems by performing soft real-time large-scale system simulation (in per unit/per phase), but providing the capability to physically simulate the transmission line active and reactive power flows such that actual physical devices, such as UPFC controllers, can be tested and validated. RTHSL enables soft real-time simulation with no specialized hardware support and no specialized operating system support for real-time scheduling, meaning it can be run on a commercial, off-the-shelf (COTS) Unix system such as Linux as long as it complies with the respective standards. The simulation algorithm itself has no requirement beyond the fact that it must run fast enough by itself on the given system's CPU and memory architecture to satisfy the real-time constraints of the system. The framework imposes few additional constraints on the hardware and operating system.

A. System Model

Large-scale power systems are usually modeled as differential-algebraic equations (DAE) [13]:

$$\dot{x} = f(x, y)\; x(0) = x_0 \tag{1}$$

$$0 = g(x, y). \tag{2}$$

In the general DAE form, $f(\cdot, \cdot)$ represents the differential equations that describe the system dynamic model, $g(\cdot, \cdot)$ are the algebraic constraints that follow the natural physical rules and include the power flow equations, x are the state variables including the generator states, and y are the algebraic variables including the network voltage magnitudes and phase angles.

The power injection model is proposed in finding the interfacing variables between FACTS devices and differential/algebraic solver simulation programs in [14]–[16]. This is the approach that has been adopted for the interface between the hardware and software systems in the RTHSL. To achieve real-time simulation, sparsity and a preprocessing step that flattens the computation by removing loops and conditionals are used. The algorithms used by the simulator are fully described in [17].

B. Real-Time Simulation

A new approach was developed to symbolically perform the LU decomposition at compile time, avoiding the expensive indexing and multiplications associated with the LU decomposition in each NR solution. This was accomplished by writing a MATLAB program that generated the C source code files comprising the solver [17]. Memory accesses performed by the C program were "flattened" so that memory was accessed through a single pointer for each matrix instead of through multiple levels of indirection. The real-time simulation is run on a commercial iHawk Xeon eight core multiprocessor system from Concurrent Computer Corp.

RTHSL's approach is to enable a soft-real-time HIL simulation to be built by first relaxing the real-time constraints on the simulation algorithm itself. It cannot always be guaranteed that a nonlinear system with an arbitrary set of values for the system's real-world variables will have a bounded number of steps to convergence with an iterative solver. Once the power system has been allowed to converge to a relatively steady state, convergence of future time steps will be very fast (two or three iterations); small changes in the real-world values will not impact this fast convergence. However, when the system encounters a contingency such as the removal of a line, a change in generator voltage, or a change in power flow through the FACTS device under test, it initially violates the real-time constraint, but then catches up within several time steps. It is this average behavior that leads to a soft real-time constraint on the simulation system. Since the system is simulating, and sampling, a continuous phenomena, the experimental setup is able to tolerate missed simulation time outputs with minimal loss of accuracy.

C. Interface

The interface used is very similar to the "power injection model" of the UPFC [18]. The general idea of the power injection model is to decouple the power system into two sub-networks: a system sub-network and a UPFC sub-network. The power injected by the UPFC is used as the interface variable between the two sub-networks. As shown in Fig. 2, a UPFC is placed on line $i-j$ in a transmission system. This yields a fictional bus k which plays the role as the interface to AC transmission system. The UPFC is used to maintain a pre-specified power flow through line $i-j$ and to regulate the voltage of the sending end bus i to a specified value. Using power flow terminology, the sending bus i is a "PV" bus and the fictional bus k is a "PQ" bus in the simulation. At the fictional bus k, P_2 and Q_2 are the series power flows in the UPFC and this is used as the injected powers in the algebraic power balance equations. At the sending end bus i, the power injection model utilizes the

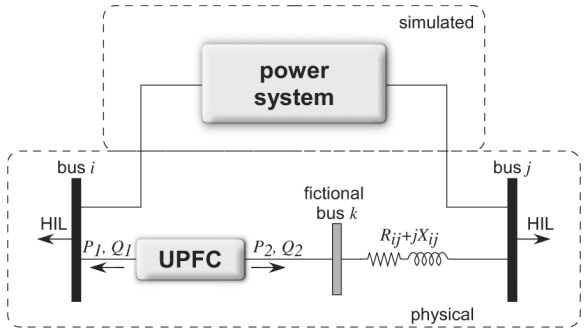

Fig. 2. Power injection model of the UPFC.

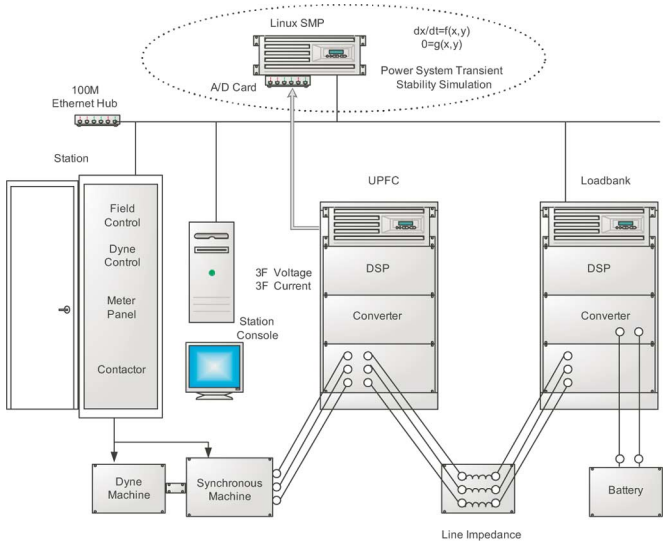

Fig. 3. Auxiliary HIL system.

shunt active power flow as the load in the algebraic power balance equations. By specifying the voltage magnitude at bus i, the algebraic power balance equations, when solved, will produce the shunt reactive power flow. The UPFC power injection model is easily incorporated into simulator, because the UPFC is modeled as an "external" network to the transmission network.

IV. Hardware System

The auxiliary HIL system is shown in Fig. 3. The hardware system consists of a synchronous machine (with field and frequency control) to provide the sending end power to bus 1, a controllable load bank to draw the required power (P_2 and Q_2), a line impedance to simulate the transmission line, and the UPFC. The analog transmission line consists of lumped inductors and resistors to simulate the transmission line. The inductance and resistance values were chosen to emulate a long transmission line. The advantage of this approach is that like an actual transmission line, the impedance will vary with frequency. The disadvantage is that actual physical effects, such as mutual coupling and capacitive line-charging, are not represented.

The UPFC is not connected to, nor does it receive any signals from, the real-time simulator; from the UPFC point of view, it is connected with, and reacts to, power and voltage changes at the sending and receiving ends. The synchronous machine field

control and the programmable loadbank both receive command settings from the simulation engine, but the UPFC acts independently from the local sensor data from the line. The auxiliary system is not part of either the UPFC or the simulation engine; it is required purely to implement the HIL physical conditions.

A. Synchronous Generator

The UPFC control algorithm reacts to physical voltages and currents. Therefore, the auxiliary external system must provide the physical conditions that an actual UPFC device would encounter. Throughout the real-time simulation, the active and reactive power flows into and out of the UPFC sending and receiving end buses are continually calculated from the measured voltages and currents. These represent the power flows throughout the system to which the UPFC would react if it were deployed in a physical system. The UPFC sending end is therefore connected to a synchronous machine and the receiving bus is connected to a programmable dynamic load. Working together, the synchronous generator and programmable load receive instructions from the power simulation engine and produce actual voltages and currents to which the UPFC reacts.

The receiving end is driven by a 3.7-kW synchronous machine. The 14.9-kW dynamometer supplies power to the synchronous machine. The synchronous exciter supplies the field to produce the voltage dictated by the simulation engine. The data acquisition, dynamometer, and field control interface is accomplished with a Labview [19] software interface. An internet domain socket-based Labview program is developed to communicate with the simulation engine and implement the synchronous machine voltage control by regulating the field current. The machine terminal voltage acts as the sending end bus of the UPFC in the HIL line.

B. Programmable Load

The programmable load is designed to reproduce the voltage and angle that would be seen by the UPFC receiving end bus based on the dynamic power simulation engine. Since the receiving end of the UPFC is modeled as a "PQ" bus, the programmable load is designed to function in the same manner. The load is simulated using a STATCOM coupled with a battery and a static resistive load. The static resistive load is used to center the active power flow on the HIL line to a nominal value. The battery energy storage system (BESS) can then be charged or discharged to change the active power flow by $\pm 25\%$ of the nominal value. This value can be increased by using a larger BESS. The STATCOM is used to vary the voltage and/or the reactive power (depending on which control approach is used). By rapidly modulating the active and reactive power flow of the STATCOM/BESS in accordance with the dynamic simulation, the receiving end of the UPFC will experience varying power flow on the line as it would if it were actually deployed in a system and responding to a transient. The STATCOM is interfaced with a BESS that consists of 9 VLRA super-gel batteries supplying 108-V dc to provide variable active and reactive power.

In practice, the variations of power and voltage magnitude by the generator and the load have their own dynamics which may affect the simulation results. However, take extreme care to ensure that these effects are minimized. The biggest contra-

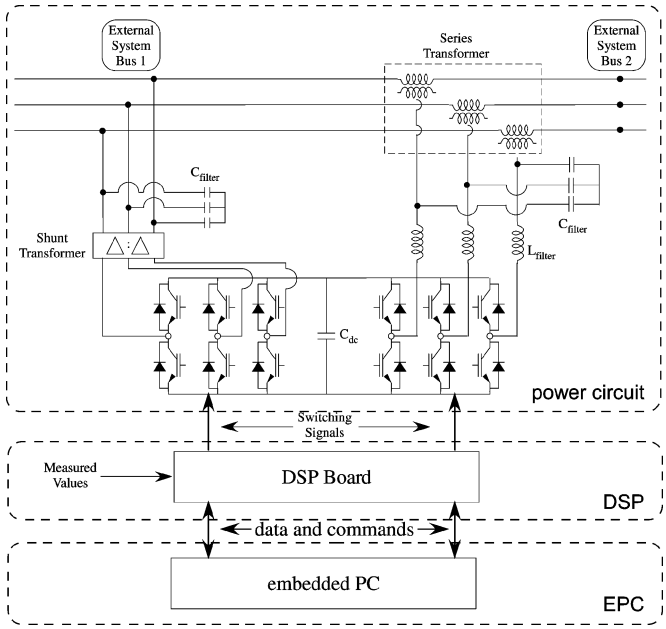

Fig. 4. UPFC.

effect that has been observed is the time lag incurred between the simulation engine signal and the response of the HIL. This time delay, however, is typically quite small and has not been observed to produce large inaccuracies in response.

C. UPFC

The UPFC physical configuration is shown in Fig. 4. The UPFC is comprised of three levels:

1) a high power subsystem system;
2) a DSP-based data-acquisition and PWM generation system; and
3) an embedded PC (EPC) control system

1) High Power System: The UPFC high power circuit includes a shunt circuit branch and a series branch. Each branch consists of a three-phase voltage-source-converter (VSC), an LC filter, and a transformer. The shunt converter and series converter share a common DC link supported by a DC capacitor.

The six-pulse bridge voltage-source-converters (VSC) converts the DC link voltage into three staircase waveforms through IGBT switching. The power modules used are Fuji 100 A/600 V IGBTs with the expected power rating (10 kW) and AC voltage rating (230 volts). The DC-link capacitor releases the transmitted energy through the series device during transients. The active power flow can vary from 3 kW to 6 kW (50% to 100%), resulting in line current changes from 20 A to 40 A. To reduce the fluctuation of the DC-link voltage to no more than 10% during transients, the minimum required capacitance is given by [20]

$$C_{\rm dc} = \frac{3L\left(I_1^2 - I_0^2\right)}{2 \times 10\% \times V_{\rm dc0}^2} \tag{3}$$

$$= \frac{3 \times 0.001 \times \left(40^2 - 20^2\right)}{2 \times 0.1 \times 94^2} = 2000\ \mu\text{F} \tag{4}$$

where L is the equivalent inductance of the series branch.

The AC side of the VSC is connected with an LC filter to reduce the inverter output harmonics. The low pass LC output filter is designed to eliminate the high frequency harmonics in the PWM voltage V_i and pass the fundamental filtered voltage V_f. The transfer function from V_i to V_f is given by

$$H(s) = \frac{1}{1 + LCs^2}. \tag{5}$$

The selection of the inductance L and capacitance C is based on consideration of the harmonic voltages that need to be filtered and the active power losses. The harmonic levels in the voltage are mainly determined by the switching frequency. Harmonic frequencies always exist at and around multiples of the switching frequency. Because of the relative ease in filtering harmonic voltages at high frequencies, it is desirable to use as high a switching frequency as possible. However, the disadvantage of using high switching frequencies is the increase in switching losses and increased computational burden on the DSP. The typical value of switching frequency is less than 6 kHz. Therefore, the frequency modulation ratio is selected as 27 and switching frequency is 1.62 kHz.

With a switching frequency of 1.62 kHz, the cut-off frequency of the filter $(\omega_c = 1/\sqrt{LC})$ is taken to be 300 Hz, which yields

$$LC = \frac{1}{\omega_c^2} = \frac{1}{(2\pi \cdot 300)^2} = 2.81 \times 10^{-7}. \tag{6}$$

Reducing filter losses requires the smallest inductance L possible. For example, the series branch of the UPFC has a 5-kVA transformer with a secondary voltage of 120 volts. Thus, the rated impedance is

$$Z = \frac{V^2}{P} = \frac{120^2}{5 \times 10^3} = 2.88\ \Omega. \tag{7}$$

If L is limited to be 10% of the rated impedance, then

$$L < \frac{10\% \cdot Z}{\omega} = 0.76\ \text{mH}. \tag{8}$$

By combining (6) and (8), then C is also limited such that $C > 370\ \mu$F. Therefore, the parameters of the LC filter are chosen to be $L = 0.5$ mH and $C = 500\ \mu$F.

Fig. 5 shows the frequency response of the LC filter. The top and middle subfigures are the Bode diagram. The bottom subfigure shows the frequency scan result. Based on the Bode figure, the fundamental waveform is bypassed and all higher harmonics (which are dominated by the switching frequency) are effectively removed. Fig. 6 shows the filtered and unfiltered output waveforms.

The transformers connect the shunt and series VSCs into the AC transmission system. The shunt transformer is a 5-kVA Y-Δ , three-phase dry-type transformer with a high-side (Y) voltage of 230 volts and low-side (Δ) voltage of 125 volts. The series transformer consists of three separate single phase transformers, each rated 2 kVA with high-side voltages of 125 volts and low-side voltages of 50 volts. The high voltage side transformers are connected in delta.

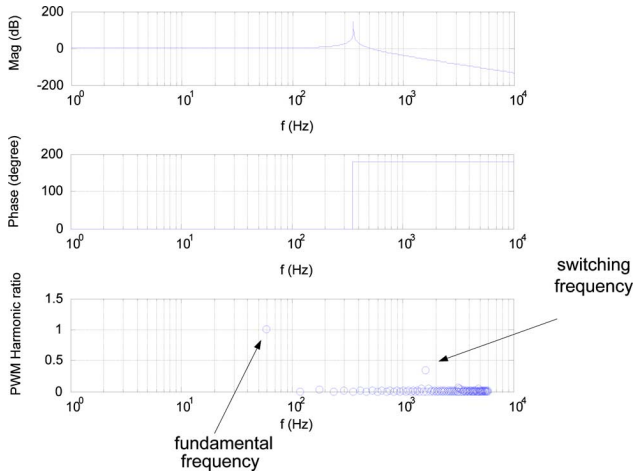

Fig. 5. LC filter frequency response.

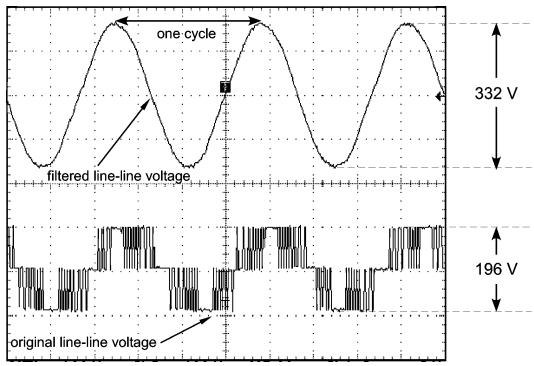

Fig. 6. VSC original line-line voltage and the filtered voltage.

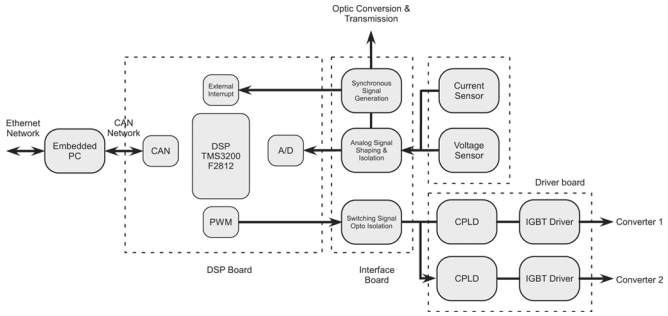

Fig. 7. UPFC in-rack data acquisition and control system.

2) DSP-Based Control System: The in-rack UPFC data acquisition and PWM generation system is shown in Fig. 7. A MSK2812 digital signal processing (DSP) board from Technosoft is used. The main task of the data acquisition system is to acquire and preprocess the analog signals that are measured through voltage and current sensors from the UPFC. Real-time signal processing, such as digital filtering and phase calculations, is also implemented in the DSP. The processed data are exported to the embedded PC via CAN bus communication.

The data acquisition hardware consists of a DSP board, an analog interface board, and a synchronous signal generation circuit. The UPFC utilizes 16 input channels: eight for the series

converter and eight for the shunt converter. The software structure of the DAS is interrupt driven. The ADC interrupt handler is periodically (1 kHz) triggered by an end of conversion (EOC) of the A/D converter. The three-phase voltage and current sensor readings from the ADC result registers are filtered and then scaled.

The communication between the DSP and the embedded PC (EPC) is via a controller area network (CAN) bus. CAN is a serial multi-master communication protocol that efficiently supports distributed real-time control with a high level of data integrity, and communication speeds of up to 1 Mps. The CAN bus architecture is widely used in the automotive and other industrial fields that require reliable communication. The CAN bus is configured in the "extended" mode which supports 29-bit-length identifiers.

After the Park transformation to convert the readings from the abc frame to the dq frame, the values are then used to calculate the RMS values, and the active and reactive powers. The resulting values are then packed into three CAN protocol frames and sent to the CAN transmit mailboxes.

The DSP translates the updated control parameters (such as the UPFC modulation gain k and phase shift angle α) sent from the embedded PC via the CAN bus to the IGBT switching signals. Three DSP on-chip timers are used to manage the DSP on-chip PWM modules to generate 12-channel PWM switching signals. The switching signals are first isolated in the interface board and then sent to the driver boards. Generally, the logic-level control signals are not powerful enough to directly switch the IGBTs; therefore, a Semikron IGBT driver module is used. Moreover, a CPLD-based logic of fault signal detection and the control button reaction from the front panel is implemented on driver boards. The main task of the DSP code is to generate PWM switching signal based on on-chip PWM modules. A sinusoidal look-up table, which is used to generate the modulation waveform, is calculated offline and stored in the program memory. The triangle carrier waveform is generated using on-chip PWM modules.

3) UPFC Embedded PC: The third major component of the UPFC design is the embedded PC for high level control. The embedded PC is a Linux-based real-time system that provides the dynamic control algorithm implementation and several access interfaces for users. It has an independent human machine interface which provides data logging and online interaction with the control procedure to manually change the UPFC control settings (if desired). Since the UPFC control algorithm resides in the embedded PC, different control strategies can be easily programmed in C++ for rapid modification and implementation.

The UPFC is a combination of a shunt and series branches connected through the DC capacitor. The series inverter injects a voltage with controllable magnitude and phase angle in series with the transmission line to control the active and reactive power flow in the transmission line. The shunt inverter provides the active power drawn by the series branch plus the converter losses and can independently provide reactive compensation to the system. The UPFC model is a combination of the synchronous static compensator (STATCOM) and static series synchronous compensator (SSSC) models [21]:

$$\frac{1}{\omega_s}\frac{d}{dt}i_{d_1} = \frac{k_1 V_{\rm dc}}{L_{s_1}}\cos(\alpha_1+\theta_1) + \frac{\omega}{\omega_s}i_{q_1} - \frac{R_{s_1}}{L_{s_1}}i_{d_1} - \frac{V_1}{L_{s_1}}\cos\theta_1 \tag{9}$$

$$\frac{1}{\omega_s}\frac{d}{dt}i_{q_1} = \frac{k_1 V_{\rm dc}}{L_{s_1}}\sin(\alpha_1+\theta_1) - \frac{R_{s_1}}{L_{s_1}}i_{q_1} - \frac{\omega}{\omega_s}i_{d_1} - \frac{V_1}{L_{s_1}}\sin\theta_1 \tag{10}$$

$$\frac{1}{\omega_s}\frac{d}{dt}i_{d_2} = -\frac{R_{s_2}}{L_{s_2}}i_{d_2} + \frac{\omega}{\omega_s}i_{q_2} + \frac{k_2}{L_{s_2}}\cos(\alpha_2+\theta_1)V_{\rm dc} - \frac{1}{L_{s_2}}(V_2\cos\theta_2 - V_1\cos\theta_1) \tag{11}$$

$$\frac{1}{\omega_s}\frac{d}{dt}i_{q_2} = -\frac{R_{s_2}}{L_{s_2}}i_{q_2} - \frac{\omega}{\omega_s}i_{d_2} + \frac{k_2}{L_{s_2}}\sin(\alpha_2+\theta_1)V_{\rm dc} - \frac{1}{L_{s_2}}(V_2\sin\theta_2 - V_1\sin\theta_2) \tag{12}$$

$$\frac{C}{\omega_s}\frac{d}{dt}V_{\rm dc} = -k_1\cos(\alpha_1+\theta_1)i_{d_1} - k_1\sin(\alpha_1+\theta_1)i_{q_1} - k_2\cos(\alpha_2+\theta_1)i_{d_2} - k_2\sin(\alpha_2+\theta_1)i_{q_2} - \frac{V_{\rm dc}}{R_{\rm dc}}. \tag{13}$$

The currents i_{d1} and i_{q1} are the dq components of the shunt current. The currents i_{d2} and i_{q2} are the dq components of the series current. The voltages $V_1\angle\theta_1$ and $V_2\angle\theta_2$ are the shunt and series voltage magnitudes and angles, respectively. The UPFC is controlled by varying the phase angles (α_1, α_2) and magnitudes (k_1, k_2) of the converter shunt and series output voltages, respectively, and

L_{s_1}, L_{s_2}	shunt and series transformer inductances;
R_{s_1}, R_{s_2}	shunt and series transformer resistances;
$R_{\rm dc}$	resistance representing converter losses;
ω, ω_s	bus and synchronous frequency (in radians).

Many different UPFC control methods have been proposed that are based on (10)–(13) [22]–[31]. One of the simplest to implement is the decoupled PI control shown in Fig. 8. This control adjusts the switching signal reference to track desired active and reactive power outputs, sending bus (1) voltage magnitude, and the dc link voltage. This control works well for slowly changing (or constant) changes in reference values. The PI control shown in Fig. 8 is just one of many controls that can be implemented in the RTHSL. The PI control parameters are give in Table I. These parameters are selected based on the parameters in [21] and have been adjusted slightly according to the current laboratory set-up. To ensure predictable performance, the UPFC hardware was developed and tested in PSCAD (an EMTP-type simulation package) prior to the actual hardware assembly [32].

V. FACTS Real-Time Hardware/Software Laboratory Implementation Issues

There are several issues unique to the hardware/software interface that must be addressed for the full system to run prop-

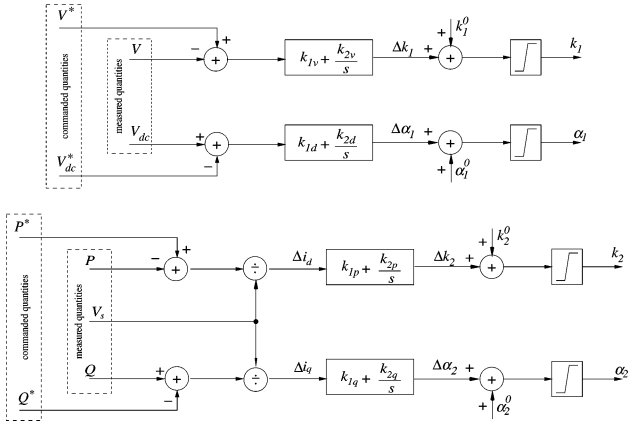

Fig. 8. UPFC control.

TABLE I
PI PARAMETERS

$K_{1v} = 0.15$	$K_{2v} = 0.05$	$K_{1d} = 0.1$	$K_{2d} = 0.05$
$K_{1p} = 0.015$	$K_{2p} = 0.1$	$K_{1q} = 0.015$	$K_{2q} = 0.05$

erly and provide accurate results. The first of these issues is the proper synchronization of all components to a common frequency. The second issue is the per-unit conversion necessary to convert the actual measured values to the correct per-unit base for integration into the real-time power system simulator.

A. Synchronization

The converters in the UPFC require a reference signal to synchronize the phase shift of the output voltage source. The reliability and accuracy of the synchronous signal plays an important role in the control system performance because all of the PWM modulation indices are synchronized to the interruption of this signal in the DSP. The analog reference signal is a sinusoidal waveform produced by the voltage sensor. A zero crossing circuit is used to get the desired square waveform. A flip-flop trigger is used to eliminate the multiple noisy crossing points. Thus, an ideal clean square waveform is produced with acceptable accuracy loss, but with a microsecond-level time delay. Improperly synchronized waveforms may cause numerous undesirable effects including undamped oscillations, loss of controllability, and loss of accuracy in the simulation. The synchronizing signal is not wire-connected to the programmable load because of signal attenuation and EMI noise. Therefore, an HFBR fiber optic connection is used. Fig. 9 shows the synchronization waveform.

B. Per-Unit Conversion

To be used in the numerical solution, the data exchanged between the physical hardware and the real-time simulator must be converted to per-unit. In the software dynamic simulation, the bases are pre-defined and all variables, including voltage, active power, and reactive power, are calculated in per-unit. The implementation challenge arises in converting the actual power and voltage bases to the proper per-unit injected powers for the power injection model. The per-unit conversion requires that the UPFC integrate seamlessly to represent the per-unit power flow

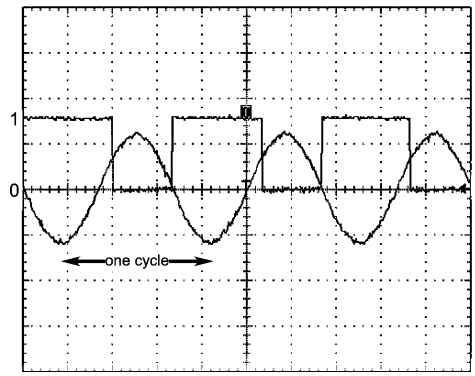

Fig. 9. Output of synchronization circuit.

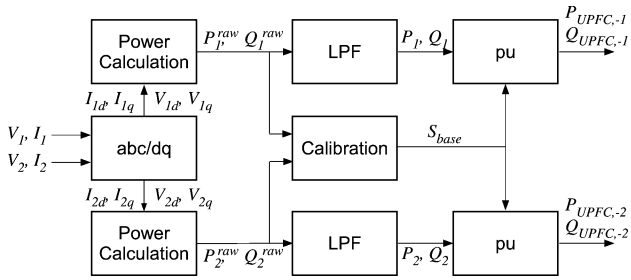

Fig. 10. System per-unit conversion.

from the simulation regardless of the rating of the line upon which it is placed.

The power base is variable and depends on the initial power flow on the line upon which the UPFC is placed in the network. Therefore, a self-calibration must be utilized to determine the power base. At the simulation initiation, the simulation engine waits several seconds before sampling and calculating the initial steady-state power flow on the HIL line to be used as the per-unit power base. Fig. 10 shows the per-unit process.

The "abc/dq" block represents the transformation of the abc phase components into the constant dq components in the rotating reference frame. The "Power Calculation" block is where the voltage and current measurements are used to calculate the instantaneous power. The "calibration" block contains an averaging filter to calculate the power base $S_{\rm base}$. The low pass filter (LPF) is used to eliminate any noise in the calculation of the power values. The "pu" block finishes the normalization action through dividing the filtered power value by $S_{\rm base}$. The values $P_{\rm UPFC-1}$ and $Q_{\rm UPFC-2}$ are the per-unit active and reactive powers that are passed to the simulation engine to update the numerical solution.

VI. RESULTS

The RTHSL can be used to test various placements and control strategies for the UPFCs in a large power system. The UPFCs can be easily "moved" from one place to another to validate their impact on cascading failures and to test whether or not there are any unforeseen control interactions.

A. Manual Control

Fig. 11 shows the experimental results for manual power flow control. The top-left trace is the actual UPFC power flow in the

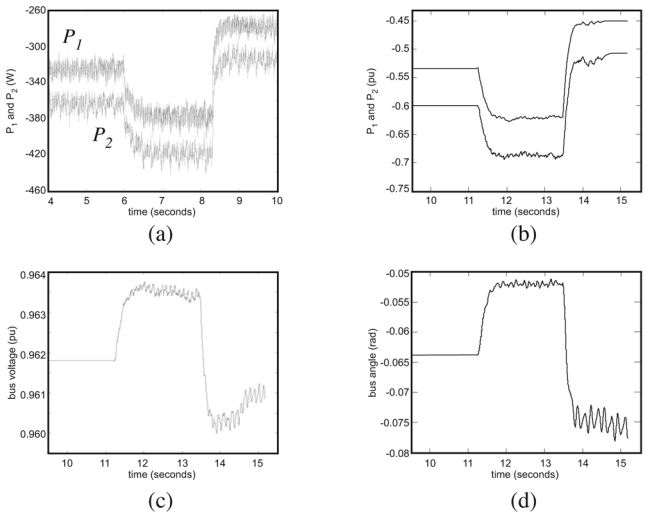

Fig. 11. Manual power flow control (a) measured active power, (b) filtered active power, (c) simulated voltage magnitude, and (d) simulated voltage angle.

HIL line. The top-right trace is the filtered power flow injected into the simulation engine. The bottom two traces are separately the simulated bus voltage and bus angle. These traces are used to validate that the scaling and interface between the HIL and the simulation are working properly. In this scenario, the UPFC is given two commanded active power changes: a decrease and then an increase. The simulated system reacts to the changes in the power flow and voltage settings of the UPFC. This appropriate reaction is shown in the lower figures in which the simulated voltages and angles respond to the changes in active power. For example, the bus voltage magnitude increases and then decreases in accordance with the active power changes. Note also how the step change in active power induced low-frequency oscillations in the system; this is what would be expected in an actual system even though these are simulated.

B. One UPFC

The RTHSL can also be used to study the impact of UPFC controllers on cascading failures. In this paper, one particular cascading scenario of the 118-bus system will be described in detail. The 118-bus test system is shown in Fig. 12. In this cascading fault scenario, a three-phase high impedance fault occurs on bus 37 and is cleared by removing line 37–39. This initiates a cascading failure as successive lines become overloaded and trip offline. Subsequently, line 37–40 overloads and trips, followed by line 40–42 after which the system becomes unstable.

An offline time domain simulation of this cascade is shown in Fig. 13. Note that the fault is applied at time $t = 0$ and line 37–39 is tripped shortly afterward. The power flow on line 37–40 immediately exceeds the line rating (shown by the upper dashed line). Corrective relay action trips the line after nearly 4 s. At this point, power on line 40–42 exceeds its rating (shown by the lower dashed line). Note that negative indicates that power is flowing from bus 42 to bus 40. At 5.5 s, line 40–42 is tripped and the system goes unstable shortly before 6 s.

An analysis of this system indicates that if a single UPFC is placed on line 37–40 with an active power setting of 0.55 pu,

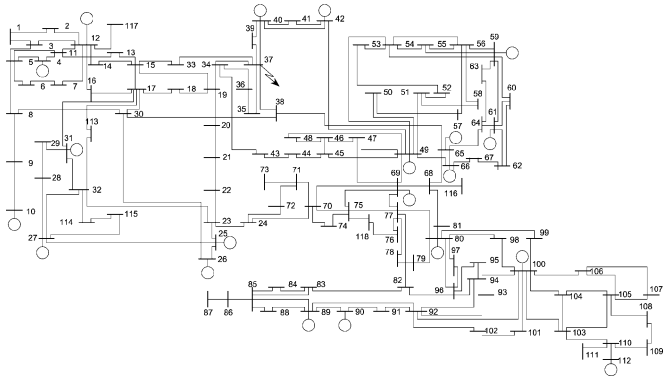

Fig. 12. IEEE 118-bus test system.

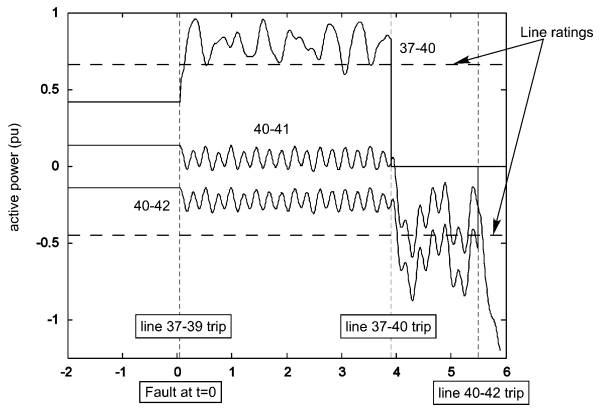

Fig. 13. Offline time domain simulation of cascading failure.

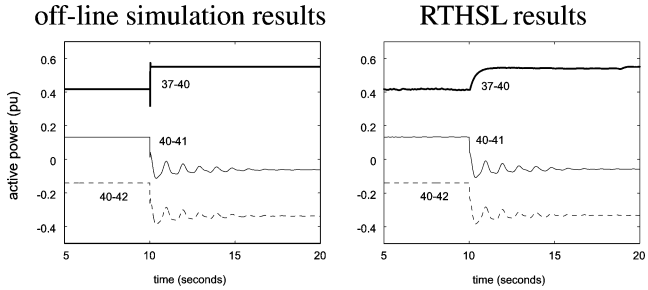

Fig. 14. Comparison of cascading failure avoidance.

then the cascaded outage can be avoided. This setting is determined using a maximum flow graph model described in [33]. Note that both the active power flows on line 37–40 and 40–42 are maintained below their ratings. This scenario is then validated via the RTHSL with the UPFC on line 37–40. The results of the experimental hybrid simulation are shown in Fig. 14. The offline simulation shows much faster response than the experimental results due to difference in controllers. It is possible to finely tune the PI parameters through "trial and error" much easier in simulation than in the actual system. Even with slightly different parameters, however, the results show a good correspondence.

C. Two UPFCS

Similarly, two UPFCs are applied to the same scenario case. The two UPFCs are placed on line 37–40 and line 15–19. When line 37–39 is tripped at 1 s, the line active power setting

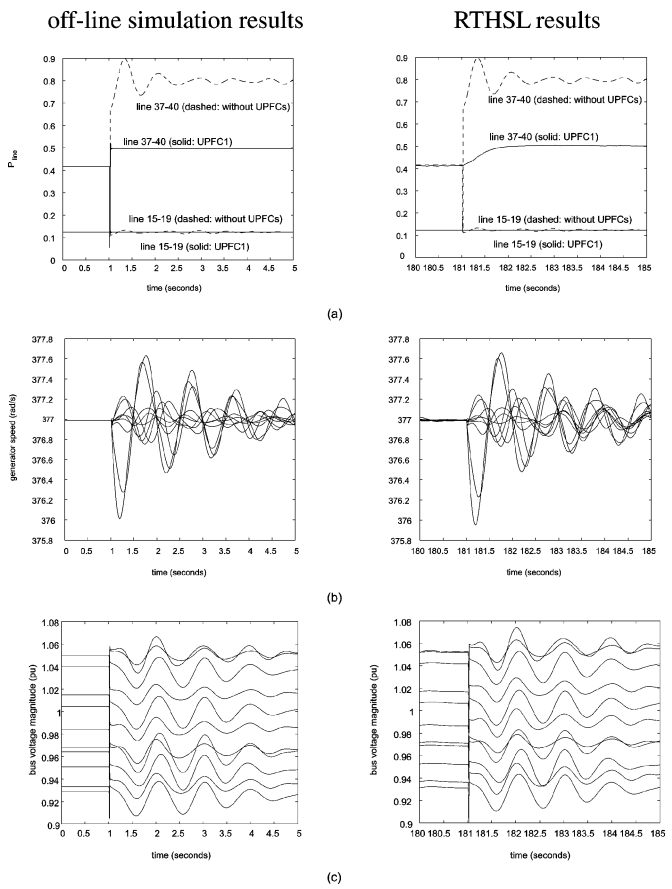

Fig. 15. Comparison of cascading failure avoidance—two UPFCs. (a) Line active power (pu). (b) Selected generators angular frequency (rad/s). (c) Selected voltage magnitudes (pu).

on UPFC1 (line 37–40) is changed from 0. 417 to 0.497, and UPFC2 (line 15–19) is kept at the original line active power setting. The result of an offline simulation and the experimental RTHSL are shown in Fig. 15. The subfigure (a) presents line active power in the cases with UPFC and without UPFC, (b) presents generator speed deviations, respectively, and (c) presents bus voltage magnitudes. Not all results are shown due to space constraints, but a wide enough selection of generator speeds and bus voltage magnitudes are shown to provide sufficient confidence in the accuracy of the results. The offline simulation and HIL simulation both show that the two UPFCs can cooperate to regulate line active power to the commanded value immediately after the initiating line outage. Any potential line overloads are prevented and all of the generators remain stable. Note that the offline simulation results and HIL simulation result are nearly identical similar, except that the oscillation is damped slightly more rapidly in the offline simulation than in the HIL simulation. This is due to the difference in controllers between the simulated and actual UPFC controllers.

These results indicate that the RTHSL laboratory is functioning as designed and can be used to validate a variety of experiments including control development, UPFC placements, and device interactions.

VII. Conclusion

This paper presents a novel real-time laboratory capable of rapidly validating UPFC controls and placements. The primary advantages of the developed RTHSL are:

- large-scale real-time simulation;
- full UPFC dynamics (not just controller performance);
- ability to rapidly test UPFC control interactions and placements;
- ease of control integration;
- ability for both manual and automated (DSP-based) control.

References

[1] M. Bacic, "On hardware-in-the-loop simulation," in *Proc. 44th IEEE Conf. Decision and Control (CDC-ECC'05)*, Dec. 2005, vol. 44, pp. 3194–3198.

[2] K. Wang, M. L. Crow, and Y. Cheng, "Development of a FACTS real-time hardware-in-the-loop simulation," in *Proc. 39th North American Power Symp.*, Sep. 2007.

[3] K. Wang, M. L. Crow, Y. Cheng, and B. McMillin, "A hardware-in-loop FACTS control system design for real-time power system simulation," in *Proc. IEEE Power & Energy Soc. General Meeting*, Calgary, AB, Canada, Jul. 2009.

[4] F. Rahimi, "Specifications for on-line dynamic security assessment," presented at the Dynamic Security Assessment Working Group of the IEEE Power Engineering Society, San Francisco, CA, Jul. 25, 1994.

[5] P. Mercier, C. Gagnon, M. Tetreault, and M. Toupin, "Real-time digital simulation of power systems at Hydro-Quebec," in *Proc. 1st Int. Conf. Digital Power System Simulators (ICDS'95)*, Apr. 1995.

[6] V. Dinavahi, R. Iravani, and R. Bonert, "Design of a real-time digital Simulator for a D-STATCOM system," *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 1001–1008, Oct. 2004.

[7] P. Lok-Fu, M. O. Faruque, N. Xin, and V. Dinavahi, "A versatile cluster-based real-time digital simulator for power engineering research," *IEEE Trans. Power Syst.*, vol. 21, no. 2, pp. 455–465, May 2006.

[8] F. Tian, C. Yue, Z. Wu, and X. Zhou, "Realization of electromechanical transient and electromagnetic transient real time hybrid simulation in power system," in *Proc. IEEE/PES 2005 Transmission and Distribution Conf. Exhib.: Asia and Pacific*, 2005, pp. 1–6.

[9] R. Kuffel, J. Giesbrecht, T. Maguire, R. P. Wierckx, and P. G. McLaren, "RTDS—A fully digital power system simulator operating in real-time," in *Proc. Int. Conf. Energy Management and Power Delivery (EMPD'95)*, 1995, vol. 2.

[10] D. Jakominich, R. Krebs, D. Retzmann, and A. Kumar, "Real time digital power system simulator design considerations and relay performance evaluation," *IEEE Trans. Power Del.*, vol. 14, no. 3, pp. 773–781, Jul. 1999.

[11] J. Shu, X. Wei, and Z. Weimin, "A parallel transient stability simulation for power systems," *IEEE Trans. Power Syst.*, vol. 20, no. 4, pp. 1709–1717, Nov. 2005.

[12] [Online]. Available: http://www.rtds.com.

[13] M. Crow, *Computational Methods for Electric Power System*, 2nd ed. Boca Raton, FL: CRC, 2009.

[14] M. Noroozian *et al.*, "Improving power system dynamics by series-connected FACTS devices," *IEEE Trans. Power Del.*, vol. 12, no. 4, pp. 1635–1641, Oct. 1997.

[15] H. Zhengyu *et al.*, "Application of unified power flow controller in interconnected power systems-modeling, interface, control strategy, and case study," *IEEE Trans. Power Syst.*, vol. 15, no. 2, pp. 817–824, May 2000.

[16] K. M. Son and R. H. Lasseter, "A newton-type current injection model of UPFC for studying low-frequency oscillations," *IEEE Trans. Power Del.*, vol. 19, no. 2, pp. 694–701, Apr. 2004.

[17] W. Siever, D. Tauritz, A. Miller, B. McMillin, M. Crow, and S. Atcitty, "Symbolic reduction for high-speed power system simulation," *Simulation: Trans. Soc. Modeling and Simulation Int.*, vol. 84, no. 6, pp. 297–309, Jun. 2008.

[18] D. J. Gotham and G. T. Heydt, "Power flow control and power flow studies for systems with FACTS devices," *IEEE Trans. Power Syst.*, vol. 13, no. 1, pp. 60–65, Feb. 1998.

[19] [Online]. Available: http://www.ni.com/labview.

[20] H. Fujita, Y. Watanabe, and H. Akagi, "Transient analysis of a unified power flow controller and its application to design of the DC-link capacitor," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 735–740, Sep. 2001.
[21] L. Dong, M. L. Crow, Z. Yang, and S. Atcitty, "A reconfigurable FACTS system for university laboratories," *IEEE Trans. Power Syst.*, vol. 19, no. 1, pp. 120–128, Feb. 2004.
[22] H. Wang, "A unified model for the analysis of FACTS devices in damping power system oscillations—Part III: Unified power flow controller," *IEEE Trans. Power Del.*, vol. 15, no. 3, pp. 978–983, Jul. 2000.
[23] B. C. Pal, "Robust damping of interarea oscillations with unified power-flow controller," *Proc. Inst. Elect. Eng., Gen., Transm., Distrib.*, vol. 149, no. 6, pp. 733–738, Nov. 2002.
[24] B. Chaudhuri, B. C. Pal, A. Zolotas, I. Jaimoukha, and T. Green, "Mixed-sensitivity approach to H_∞ control of power system oscillations employing multiple FACTS devices," *IEEE Trans. Power Syst.*, vol. 18, no. 3, pp. 1149–1156, Aug. 2004.
[25] M. M. Farsangi, Y. H. Song, and K. Y. Lee, "Choice of FACTS device control inputs for damping interarea oscillations," *IEEE Trans. Power Syst.*, vol. 19, no. 2, pp. 1135–1143, May 2004.
[26] N. Tambey and M. L. Kothari, "Damping of power system oscillations with unified power flow controller (UPFC)," *Proc. Inst. Elect. Eng., Gen., Transm., Distrib.*, vol. 150, no. 2, pp. 129–140, Mar. 2003.
[27] M. Ghandhari, G. Andersson, and I. A. Hiskens, "Control lyapunov functions for controllable series devices," *IEEE Trans. Power Syst.*, vol. 16, no. 4, pp. 689–694, Nov. 2001.
[28] S. Robak, M. Januszewski, and D. D. Rasolomampionona, "Power system stability enhancement using PSS and Lyapunov-based controllers: A comparative study," in *Proc. IEEE 2003 Power Tech Conf.*, Bologna, Italy, 2003, vol. 3, p. 6.
[29] C.-C. Chu and H.-C. Tsai, "Application of Lyapunov-based adaptive neural network UPFC damping controllers for transient stability enhancement," in *Proc. 2008 IEEE Power & Energy Soc. General Meeting*, Jul. 20–24, 2008.
[30] A. Bidadfar, M. Abedi, M. Karari, and C.-C. Chu, "Power swings damping improvement by control of UPFC and SMES based on direct Lyapunov method application," in *Proc. 2008 IEEE Power & Energy Soc. General Meeting*, Jul. 20–24, 2008.
[31] M. Januszewski, J. Machowski, and J. W. Bialek, "Application of the direct Lyapunov method to improve damping of power swings by control of UPFC," *Proc. Inst. Elect. Eng., Gen., Transm., Distrib.*, vol. 151, no. 2, pp. 252–260, Mar. 2004.
[32] [Online]. Available: http://www.pscad.com.
[33] A. Armbruster, M. Gosnell, B. McMillin, and M. Crow, "The maximum flow algorithm applied to the placement and distributed steady-state control of UPFCs," in *Proc. North Amer. Power Symp.*, Ames, IA, Oct. 2005.

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