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Dynamic Response Improvement in a Buck Type Converter Using Capacitor Current Feed-Forward Control

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***Abstract*—The dynamic performance of dc-dc power electronic converters is mainly determined by the output filtering capacitor and inductor, control loop(s) compensator(s), and the voltage conversion ratio. Normally, a larger capacitance and/or a smaller inductance are not recommended because of the extra cost and size of the capacitor and/or the increment of the inductor current ripple. The capacitor current feed-forward method has gained popularity due its fast dynamic response, simpler structure, and less sensing losses. In applications where a large voltage conversion ratio is needed, dynamic response for a load step-down scenario is worse than that of a load step-up condition. In order to alleviate this situation, a buck derived dc-dc converter is chosen. By combing the capacitor current feed-forward control and the buck derived converter topology, a novel control scheme is proposed in this paper. Simulation results containing the voltage overshoot and settling time are presented. The proposed approach is a high performance, simple structure, and low cost/volume strategy for load step-down dynamic improvements.**

I. INTRODUCTION

In digital signal processing (DSP) and point-of-load (POL) applications, dynamic response of the dc-dc converter (usually buck type converter) is a stringent requirement due to the large and sudden changes of the digital loads. According to [1-2], the supplying voltage to the digital devices is less than 1 V and the output current is around 200 A. The lower the output voltage and/or the higher the load current, the more the challenge will be for the high dynamic response dc-dc converter designs.

Several factors affect dynamic response characteristics of dc-dc converters. A larger output filtering capacitor may reduce output voltage deviations. However, this could increase the system volume and cost. Smaller inductor in the power stage may benefit to the recovery of the output voltage; unfortunately, this will boost the inductor current ripple which would add system magnetic and switching losses. Other two important factors influencing the dynamic response are the control loop(s) and the dc-dc converter topology. By an optimized design on the control loop compensator [3-4], the dynamics can be improved. However, this improvement is limited by the slow voltage loop. A faster hysteretic voltage/current mode control loop could be sensitive to the noise and would have the EMC problem. The static state error is another disadvantage [5] associated with hysteresis controllers. The second-order boundary control [6] method shows a good dynamic response improvement. However, the implementation is not very simple and the control speed is limited by the multiplier used in the controller. The separated controller strategy [7] tries to break the bandwidth limitation of linear controllers by adding a non-linear controller for the transient dynamics control. As pointed in [8], without a proper design, there may appear a chattering phenomena between the linear and non-linear controller which could cause very high frequency switching actions leading to extra noise and efficiency deterioration.

In low-voltage, high-current digital load applications, load step-down dynamic improvement is more important than that of the load step-up counterpart [9-10]. Two buck derived convert topologies focusing on load step-down dynamic response improvements are discussed in [9-10]. They both have a similar dynamic performance. One advantage of [10] is its simpler circuit structure. However, in general, the control strategies applied in [9-10] are not easy to implement. They all have two sets of controllers, one for steady-state control, and one for transient control. A smooth transition between these two controllers would be a great challenge for an optimized controller design.

In this paper, the buck derived converter topology proposed in [10] is chosen for dynamic response improvements. Instead of two sets of complex controllers implemented in [10], we propose a capacitor current feed-forward controller for both steady-state and the transient controllers. The proposed controller significantly simplifies the control design without decreasing the dynamic response performance thanks to the fast capacitor current feed-forward characteristics. In section II, the operation modes of the selected buck-derived topology are analyzed in details; including both the steady-state and transient-state operations. In addition, the novel current feed-forward based controller is given and the steady-state and dynamic control schemes are presented. In section III, based on the proposed controller, the simulation model is built in Matlab/Simulink and PLECS environments. The theoretical analysis is verified by the simulation results. In section IV, the experimental results are given which matches the theoretical analysis and simulation results. In section V, the evaluation of the proposed approach is summarized.

II. PRINCIPLE OF PROPOSED CONTROLLER

A. Topology Description

Fig. 1 shows the buck derived dc-dc converter. In Fig. 1,

auxiliary switch S_a and auxiliary diode D_a are used for the dynamic response control. During steady-state operation, S_a is always kept closed; at the same time, since D_a is reverse biased, it is off. Fig. 2 shows the steady-state equivalent circuit which is similar to the standard buck converter.

Therefore, under steady-state conditions, this converter operates like a conventional buck converter. When a load step-down occurs, in order for the inductor energy to be released quickly, both main and auxiliary switches S and S_a will be switched off. The equivalent circuit will change to Fig. 3. Therefore, the inductor current slew rate can be expressed by:

$$\frac{di_L}{dt} = \frac{-V_{in} - V_o}{L} \tag{1}$$

For the standard buck converter, during the same transient, the inductor current slew rate is smaller than that of the derived buck topology. This is shown in equation (2).

$$\frac{di_L}{dt} = \frac{-V_o}{L} \tag{2}$$

The greater the current slew rate, the faster the energy release which translates to a faster dynamics response. It should be noted that *D* and *Da* can be replaced by MOSFET or IGBT power switches. As discussed above, for low-voltage and high-current DSP and/or POL applications, the converter input voltage is usually much higher than that of the output voltage. Therefore, by comparing (1) with (2), one can conclude that the buck derived topology would greatly improve the load step-down dynamics because of its much larger inductor current slew rate.

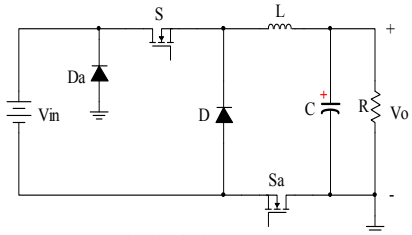


Fig. 1. Diagram of a buck derived dc-dc converter.

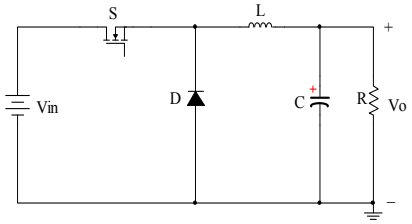


Fig. 2. Equivalent circuit for steady-state operation.

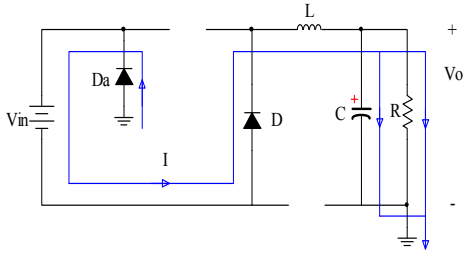


Fig. 3. Equivalent circuit for load step-down transient operation.

B. Controller Design

Current-mode control has several advantages including high audio susceptibility, simpler compensation design, and higher gain bandwidth [11]. As discussed in [12], by measuring the capacitor current instead of the inductor current, the dynamics response can be improved significantly. The capacitor current is fed forward to the controller, as sensing the capacitor current needs smaller current sensing transformer/ resistor instead of sensing the inductor or load currents [12].

In the buck derived topology, the equivalent circuits for the steady-state and the load step-down transient-state are different; therefore, the controller design is not the same as that of the standard buck converter. Fig. 4 shows the proposed controller. It is comprised of two segments. One is the conventional capacitor current feed-forward controller; the other is the transient controller. The transient controller is for dynamic improvement creating a smooth transition between the steady-state and the transient-state. Fig. 5 is one implementation example of the proposed controller. The control-logic block is used to avoid undesired SR latches states. From Fig. 5 we can see that the proposed controller is quite simple.

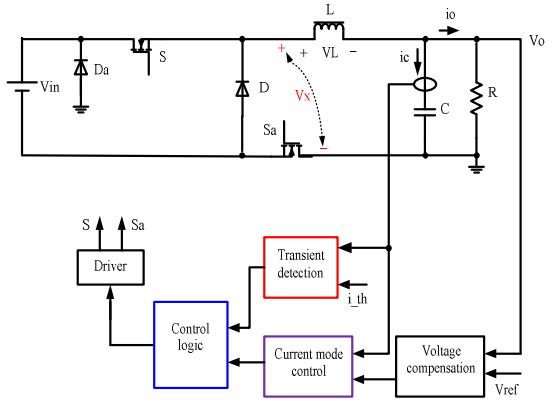


Fig. 4. Principle of the proposed controller.

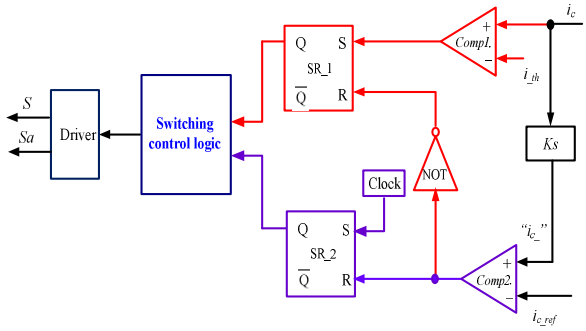


Fig. 5. Implementation of proposed controller.

Fig. 6 shows the state flow of the proposed controller. In steady-state operation, the auxiliary switch S_a is always closed and the main switch S is commanded by a PWM control signal. When there is a load step-down change, which leads to $i_c > i_{c\_th}$ (i_{c_th} is the threshold of the dynamic capacitor current), the transient control operates. Through

the transient control scheme, the two switches are all opened. While operating in the transient response mode, when the capacitor current decreases to the reference value i_{c_ref}, the transient control will end and the control scheme will switch back to the steady-state control.

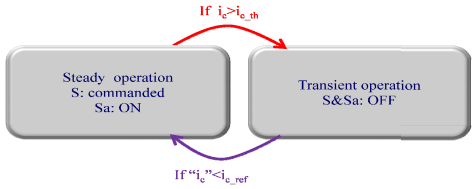


Fig. 6. Diagram of state flow.

Fig. 7 shows the switching sequence of the proposed control approach. At t_0, the load step-down change starts, then the capacitor current increases rapidly. At t_1, the capacitor current reaches the threshold value i_{c_th}, considering Fig. 5, two switches S and S_a are both at OFF state, at the same time diode S_a is turned on. At time t_2, the capacitor current reaches its peak value and after t_2, the capacitor current will decrease. At t_3, the capacitor current reduces to threshold value i_{c_th}. Based on Fig. 4, at t_3, two switches S and S_a will keep their states. Diode D_a will keep its ON state. At *t4*, signal "i_c" reaches the reference value i_{c_ref}, the switch S_a is turned on and diode D_a is turned off. The switching state of switch S will keep at its previous state and will change its state when clock signal S_2 comes, which is shown in Fig. 6. By the proposed controller, the voltage deviation during the load step-down change will be significantly reduced. This will be shown in the next section.

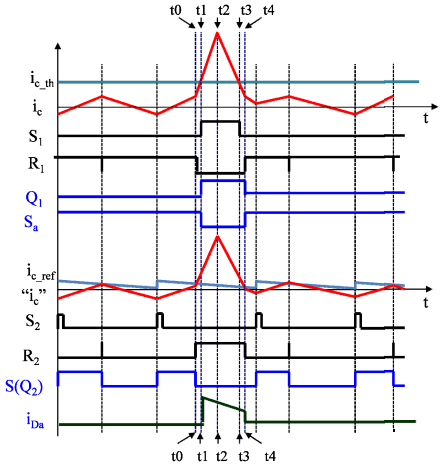


Fig. 7. Switching sequence of proposed controller.

III. Simulation of Dynamic Response Improvement

A. Control Logic and Key Waveforms

To verify the proposed control strategy, a MATLAB simulation model incorporating capacitor ESR, inductor dc resistance, switches and diode turn-on resistance was built. The circuit parameters are listed in Table I.

TABLE I
Circuit Parameters

Item	Symbol	Value	Unit
Input voltage	V_{in}	24	V
Output voltage	Vo	5	V
Capacitance	C	20	uF
Inductance	L	50	uH
Switching frequency	f_s	100	kHz
Load resistance	R	5	Ω

Fig. 8 shows the control logic of the proposed controller. From top to bottom, the traces are the capacitor current sensing signal (i_c) and compensation signal (i_{c_ref}); Reset inputs signal of the *RS* latch 2 (R2); Set inputs of the RS latch (S_2); main switch gate driving signal (S_g); auxiliary switch gate driving signal (S_{ag}); and the auxiliary diode current (i_{Da}). Fig. 9 is the key waveforms including the switching voltage (V_x) across diode D (see Fig. 5); the inductor current (i_L); capacitor current (i_c); and the output voltage (V_o). The trace representing V_x includes some negative values when the load step change happens. This is due to the special feature of the buck derived topology (higher slew rate for the inductor current).

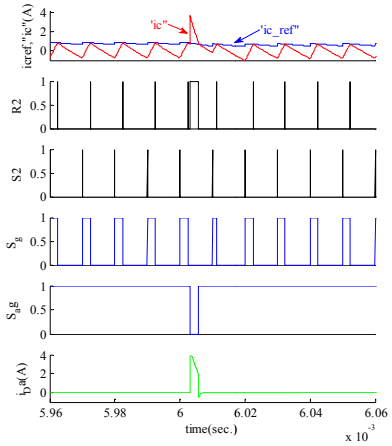


Fig. 8. Control logic with transient control.

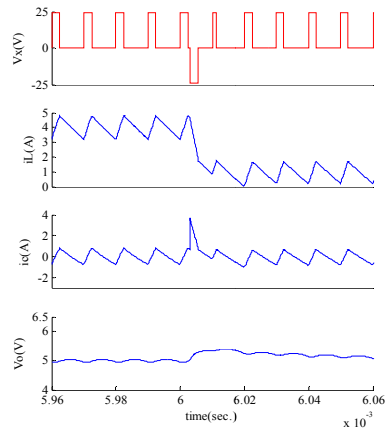


Fig. 9. Key waveforms with transient control.

B. Dynamic Response Improvement

As analyzed in section II, the dynamic response is related to the speed of inductor energy release (for a load step-down change). At the same time, the value of the inductor current affects the voltage deviation and voltage recovery time during the dynamic period. Since the energy stored in the inductor can be expressed in equation (3).

$$E_L = \frac{1}{2}LI^2 \tag{3}$$

From equation (3), it can be seen that if the inductor current ripple cannot be neglected, the voltage deviation and voltage recovery time will be affected by the inductor current ripple as well. If the load step-down change happens at the valley of the inductor current, the voltage deviation will be at the smallest value; we call it the best case of the dynamic response. Fig. 10 shows the inductor currents of this load step-down situation for both with and without the proposed transient controllers. In Fig. 10, the load step-down happens at the minimum inductor current value. It can be expected that the dynamic response in the case is faster, and the voltage deviation is smaller.

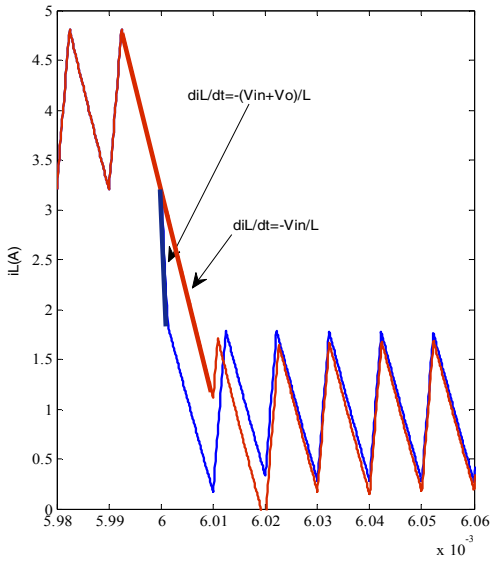


Fig. 10. Inductor current for best case of dynamic response.

Fig. 11 shows the simulation result for the best case of the dynamic response. Both scenarios (with and without the proposed transient controller) are given for the comparison purpose. The voltage overshoot and recovery time are estimated which are presented in Fig. 11 as well. If the load step-down change happens at the peak value of the inductor current, the voltage deviation will be largest; we call it the worst case of the dynamic response. Fig. 12 shows the inductor currents of this load step-down situation for both with and without the proposed transient controllers. In Fig. 12, the load step-down happens at the maximum inductor current value.

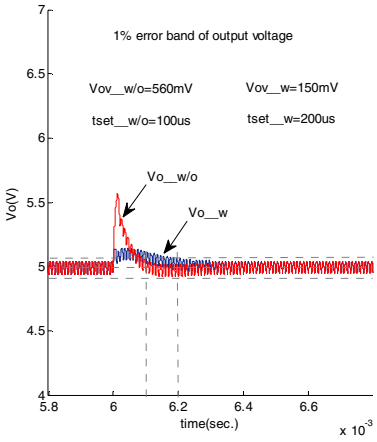


Fig. 11. Best case comparison of dynamic response.

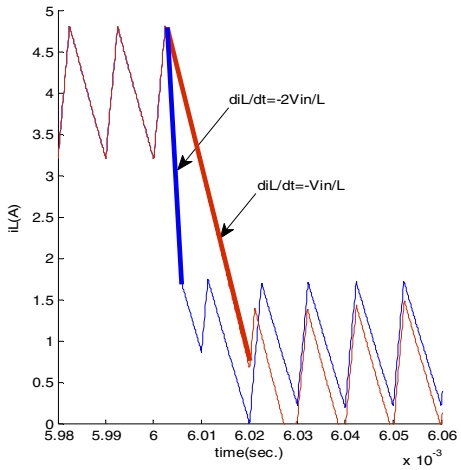


Fig. 12. Inductor current for worst case of dynamic response.

Fig. 13 shows the simulation results for the worst case of the dynamic response. Both scenarios (with and without proposed transient controllers) are given for the comparison purpose. The voltage overshoot and recovery time are estimated which are presented in Fig. 13 as well.

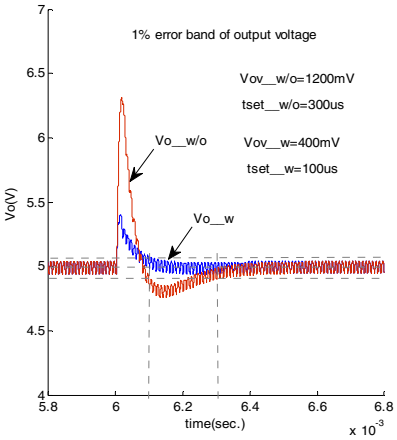


Fig. 13. Worst case comparison of dynamic response.

Table II lists the summary of the best and worst cases which are shown in Fig. 11 and Fig. 13. The load step-down change is 75% of the full load and the recovery time is defined within 1% error band limitation. From Table II, it can be seen that the inductor current ripple has a significant influence to the dynamic response if the current ripple cannot be neglected. Table II shows the case of the current ripple is about 20% of the average inductor current.

TABLE II
BEST CASE AND WORST CASE COMPARISON

Control	Without proposed controller		With proposed controller	
	Voltage overshoot (mV)	Recovery time (us)	Voltage overshoot (mV)	Recovery time (us)
Best case	560	100	150	200
Worst case	1200	300	400	100

IV. EXPERIMENTAL RESULTS

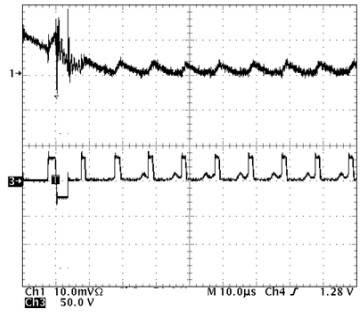
A. Experimental Results

In order to verify the proposed control strategy, an experimental hardware is developed. The full load resistance is set to be 1 Ω and the load step-down change is from 1 Ω to 10 Ω. The remaining circuit parameters are listed in Table III. In the hardware circuit, the switches are MOSFETs components and the Diodes are fast recovery power diodes. The tolerance of filtering inductance is ±20%. The output capacitor is ceramic stacked type which presents much lower ESR.

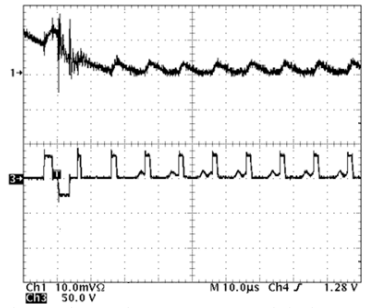
TABLE III
EXPERIMENTAL PARAMETERS

Item	Symbol	Value	Unit
Input voltage	V_{in}	24	V
Output voltage	V_o	5	V
Switching frequency	f_s	100	kHz
Inductor	L	15	uH
Capacitor	C	27	uF

Fig. 14 shows the key waveforms of control principle. In Fig. 14, ch1 is the inductor current (5A/div), and ch3 is the gate driving signal of main switch S (V_{gs}) Fig. 14(a) shows that the load step-down change occurs at peak inductor current value. Fig. 14(b) shows the case that the load step-down change happens at non-peak inductor current value. It can be seen that the main switch is turned off during the transient duration.



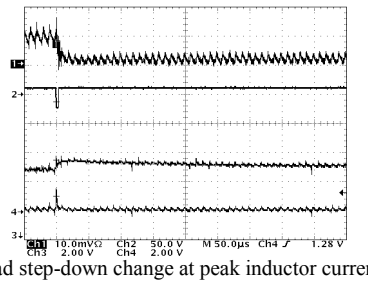
(a) Load step-down change at peak inductor current.



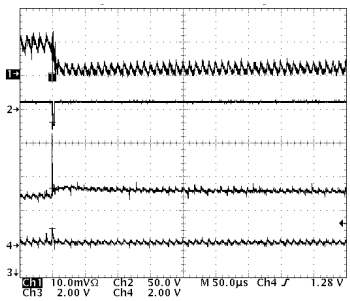
(b) Load step-down change at non-peak inductor current.

Fig. 14. Inductor current and main switch gate driving signal with the proposed controller.

Fig. 15 shows the circuit key waveforms with the proposed control scheme. In Fig. 15, Ch1 is the inductor current (5 A/div), ch2 is the gate driving signal of auxiliary switch S_a (V_{gsa}), ch3 is the output voltage (V_o), and ch4 is the capacitor current sensing signal. Fig. 15(a) shows the case that the load step-down change happens at peak inductor current value case. Fig. 15(b) shows the case that the load step-down change happens at valley inductor current value case.



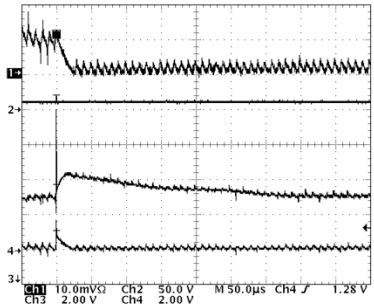
(a) Load step-down change at peak inductor current.



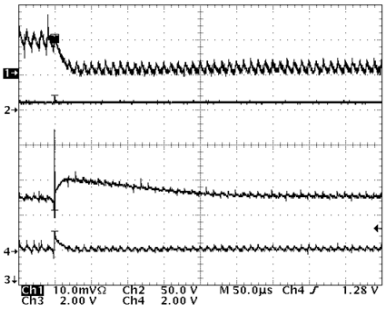
(b) Load step-down change at valley inductor current.

Fig. 15. Key waveforms with proposed scheme.

For comparison purposes, the circuit key waveforms without the proposed controller are shown in Fig. 16. Two different cases are presented in Fig. 16(a) and (b), respectively.



(a) Load step-down change at peak inductor current.



(b) Load step-down change at valley inductor current.

Fig. 16. Key waveforms without the proposed scheme.

Table IV shows the summary of two cases load step-down happens at peak and valley inductor current values for both if the scenarios of with and without the proposed controllers.

TABLE IV
COMPARISON STUDY

Comparison Study	Proposed controller		Without proposed controller	
	Case 1	Case 2	Case 1	Case 2
Overshoot Voltage (mV)	400	500	1200	1500
Recovery time (us)	65	120	220	300

Case 1: load step-down change happens at peak inductor current value. Case 2: load step-down change happens at valley inductor current value.

By comparison, from Table IV, we can see that with the proposed approach, the voltage overshoot and recovery time present more than 60% improvements compared with the conventional method.

B. Cost and Efficiency Evaluations

The additional cost for proposed strategy includes two auxiliary power components and a few SR flip-flop comparator and logic gates. However, the additional cost is not too much compared with reported approaches. The overshoot voltage reduction will lead to less output capacitor requirement and benefit the system reliability and cost reduction. The efficiency could be the concerned issue because of the additional auxiliary switch is added in the main power circuit. However, the auxiliary switch is always kept ON during the steady-state which is the normal operation mode. Since the ON resistance of the MOSFET is very small, the conduction losses of the auxiliary switch will be much smaller than the switching loss in the circuit. So, the efficiency will not be significantly affected. It was less than 1% additional power loss in the tested circuit.

V. CONCLUSION

The capacitor current feed-forward control method has been presented. By applying this proposed control scheme to a buck derived converter, the dynamic response is greatly improved. The voltage overshoot and recovery time present more than 60% improvements compared with the conventional method. The advantages of the proposed approach are higher performance, simpler structure, lower cost, and higher reliability.

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