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Open Forum

Radiation Resistance Testing of MOSFET and CMOS as a Means of Risk Management

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Index Terms—**CMOS, MOSFET.**

I. RADIATION EFFECTS

A. Cumulative Effects

Radiation effects in electronic components can be classified into two categories: cumulative effects and Single Event Effects (SEE). Cumulative effects are the sum of microscopic defects resulting from the deposition of (radiative) energy in the device and isolation material (e.g., SiO_2). Ionizing radiation damages devices by generating electron-hole pairs which can be segregated by a local electric field. Subsequently, the holes can be trapped in the oxide or migrate to Si-SiO_2 interface where they assume undesired interface states. Both trapped holes and interface states accumulate and influence the semiconductor's characteristics. The cumulative dose of energy deposited in the materials is called the total ionizing dose (TID) and expressed in terms of SI unit, Gray (Gy[1]). The linear energy transfer (LET) describes the radiative energy deposited but on an area per unit mass of material [i.e., $\mathrm{MeVcm^2 mg^{-1}}$]. Finally, the Non-Ionizing Energy Loss (NIEL) describes the induced damage, as a function of particle nature and energy, and it is used to correlate effects seen in radiation environments.

A very brief summary of the cumulative and single event effects (SEE) is given with Table I as a guide.

1) Single Event Effects (SEE): Single event effects are generally understood to be direct ionization by a single particle, with sufficient transfer of energy, that the intended operation of the device is disturbed. The damaging energy deposited in the device may be directly from the particle itself or via secondary particle-material interactions. Most of the documented SEEs to date are associated with heavy particle irradiation tests. Since undesired SEEs are stochastic, one can only speak of the probability of occurrence. The sub-classification of SEEs is briefly summarized as follows.

1) Permanent SEEs are also known as hard errors. SEEs can occur in CMOS devices. The physical source of the error is often a short-circuit like current on a power line at a sensitive point in the circuit. Single Event Burnouts (SEBs) have been observed in MOSFETs, BJTs, and diodes; again a short-circuit across a high-voltage junction can impair the part. SEEs occur in MOSFETs and they are the result of ionization energy that is deposited momentarily increasing the electric field across the oxide beyond the breakdown limit. Stuck Bit errors have been noted in SRAM and DRAM chips and describe memory point faults without possibility to rewrite the correct value
2) Static SEEs are generally not destructive and regard the overwriting of one or more bits of information on a logic circuit by the charge collected following ionization. These effects are often called SEUs, with SEFIs referring to loss of information bits that control a specific function of the circuit.
3) Transient SEEs are spurious signals that propagate within a circuit as a result of ionization. This effect occurs in a wide range of parts. Its impact depends on the initial amplitude of the current pulse, as well as the time of the event with respect to the circuit's function. One example is a rail-to-rail voltage pulse in an op-amp.

II. RISK MANAGEMENT APPROACH

Whether for military, research (space, accelerator physics) and/or civilian use, *risk avoidance* against radiation-induced damage is not possible with COTS parts. Thus the sensible approach is *risk management*. We recommend a sensible risk management approach as follows:

1) know the radiation environment of the intended application to the extent possible;
2) know the effects of ionizing radiation on the component(s) of interest;
3) know the requirements of the application;
4) identify the candidate or chosen components;
5) test the components;
6) design-in safety factor margins to the extent possible.

In this respect, ionizing radiation is much like other environmental factors (e.g., temperature, electromagnetic noise) and the radiation tolerance on a single part should be defined via, a top-down, system requirement approach. This means that the radiation effect on the COTS part, with respect to system functionality should determine the requirement. Since system reliability is the primary goal in most applications, determination of an appropriate "safety factor" is a major challenge. The safety factor itself is a function of uncertainties in estimated radiation levels, availability of documented test data and realistically, the variability of COTS part "batch" in question. Ultimately, for a given failure mechanism such as SEU, we would like to determine the error rate as the product of the expected radiation flux and the effect-specific failure rate from documented tests.

III. IRRADIATION TESTING

To show our capability to perform irradiation testing and services, and research potential risk management solutions, testing of COTS parts has been started. In addition, we sought to establish a reference standard from which to evaluate potential radiation shielding materials. A brief summary of our test program to date is provided in the following.

A Motorola 2n7000 MOSFET Amplifier and a ST-Microelectronics HCF4081BE CMOS were irradiated at the UMRR 200 kW nuclear reactor facility. Due in part to less regulatory preparations required for γ–irradiation testing (in contrast to neutron irradiation), γ-tests were conducted first. The reactor was run at high power for about 2 h (> 10 kW), and then shut down. Gamma-rays were produced

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[1] Another unit, the "rad" (1 Gy $= 100$ rad) is the traditional unit.

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TABLE I
SUMMARY OF RADIATION EFFECTS ON ELECTRONIC COMPONENTS

Type	**Observed in**	**Metric(s)**	**Comments**
Cumulative Effects			
Total Ionizing Dose (TID)	CMOS; MOSFETS	TID; Failure possible at 30kRad dose; typically 30-50kRa	CMOS and MOSFETS relatively unaffected by displacement damage
Displacement damage	Bipolar components	Non-Ionizing Energy Loss (NIEL); 1MeV neutron equivalent	Bipolar components relatively unaffected by ionizing radiation
Single Event Effects (SEE)		Linear Energy Transfer (LET); heavy ion environments	
Permanent SEEs			
Single Event Latchup (SEL)	CMOS		
Single Event Gate Rupture (SEGR)	MOSFET, BJT, diodes		Electric filed across oxide > breakdown limit
Stuck Bits	SRAM, DRAM		Memory point permanently altered; no rewrite possible
Static SEEs		Generally not destructive	
Single Event Upset (SEU)	SRAM, DRAM	As low as 1MeV/cm^{2}mg; see Cf. [1] for additional information	Collected charge from ionization overwrites logic information
Single Event Functional Interrupt (SERI)	Complex circuits		Induced error affects control of function
Transient SEEs	Most parts; op-amps		

by the decay of the fission products[2] . Many of these products were short-lived, so the γ–ray fluence[3] decays exponentially. The initial radiation level is of the order of 50 kRad/hr in the first two hours after shutdown, and decreases to an approximately constant level of 1.5–2 kRad/hr about two days after shutdown.

The MOSFET components proved to be very sensitive to γ–ray exposure, and were irradiated at low fluences of about 1.5–2 kRad/h, to a maximum total dose of 100 kRad. The CMOS components proved more resistant to radiation, and were irradiated to up to 300 kRad total dose at dose rates of 50 kRad/h. The components were placed in a polybromide vial (0.8 in ID × 2.1 in high × 0.04 in wall). The dose rate was checked with a portable dose rate meter and independently confirmed using a thermoluminescent dosimeter (TLD). Two vials were coated with two liners of different thickness of a tungsten carbide-polymer composite, produced by Hanford Nuclear Services (HNS), West Plains, MO. This composite material can be exposed to TIDs of up to 1 MGy without being damaged, and is a promising material for shielding applications. Finally, a polybromide vial was coated with a Pb liner and used as a shielding material reference. The four vials were lined (annular tube) as follows:

1) unlined and thus bare;
2) lead lining approximately 1/16 in;
3) HNS thin polymer 1/8 in on the thinner side (slightly eccentric);
4) HNS thick polymer about $\frac{1}{4}$ in.

The four vials were placed in a sample holder (cylindrical) and reproducibly oriented in the UMRR core gridplate[4] .

The irradiations were conducted utilizing a continuous γ–energy range from approximately 1 eV to 1 MeV. Typically, irradiation testing

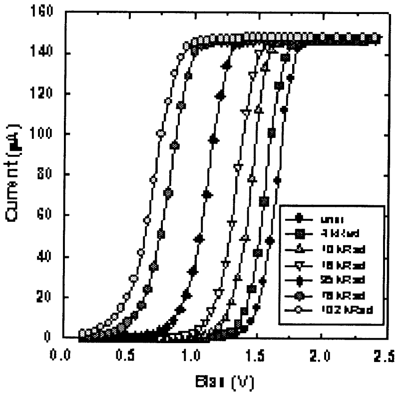

Fig. 1. Drain-source current versus applied gate voltage for a Motorola 2N7000 MOSFET. The component was irradiated in a thin walled polyethylene vial, which did not significantly attenuate gamma radiation. Dose rate was 1.7 kRad/h.

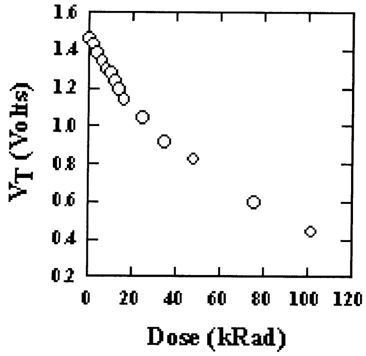

Fig. 2. Threshold voltage versus TID of the same MOSFET as Fig. 1.

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[2] UMRR uses low enrichment uranium fuel

[3] Fluence is the product of flux and irradiation time

[4] Each vial receives a slightly different dose due to its lining and orientation with respect to the γ-flux

TABLE II
CHANGE IN MOSFET THRESHOLD VOLTAGE AS A FUNCTION OF TID FOR DIFFERENT SHIELDING MATERIALS. VALUES WERE OBTAINED FROM LINEAR FITS TO CURVES LIKE IN FIG. 2 FOR TIDS BELOW 20 KRAD

Shielding Material	**V_T variation, (Volts/kRad)**
None	0.0181
1/16” Pb	0.0112
1/8” polymer	0.0102
¼” polymer	0.0116

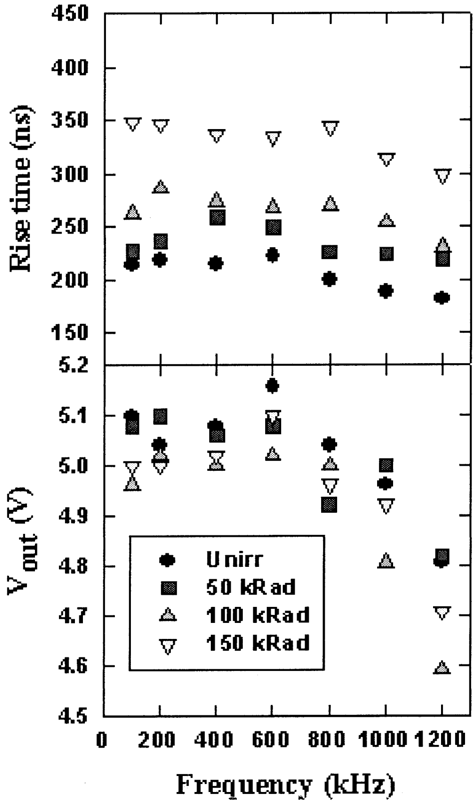

Fig. 3. Rise time and voltage of the wave output by a HCF4081BE CMOS AND gate as a function of the frequency of an input square wave, and of TID. Dose rate was 50 kRad/h. Data refer to components contained in a polyethylene vial, which negligibly attenuated gamma radiation.

of components is carried out using a Cobalt-60 radioisotope that emits γ-ray at 1.17 and 1.33 MeV. Due to γ–material interactions within the material encapsulating the source (plastic) or a given shielding liner, γ-rays are also given off at lower energies, typically 1–5 eV. While quasimonoenergetic beams like cobalt allow testing at specific energies, irradiation tests using a continuous source from research reactors provide a different, yet relevant environment as well.

All components were irradiated with grounded terminals at a constant temperature of 18–20 °C. Electrical testing of the MOSFETs was carried out with the source and drain terminals kept at fixed voltages of ± 1.58 V. The gate bias was varied between 0.15 and 2.4 V with respect to the source voltage. Electrical testing of the CMOS was carried out by supplying a fixed voltage of $+5$ V to one input of the AND gates and a square wave with amplitude of 5 V with a pulse generator to the other gate. The shape of the output wave was measured with a digital oscilloscope. Prior to irradiation, the components were individually tested and found to have characteristics equivalent to within $\pm 20\%$.

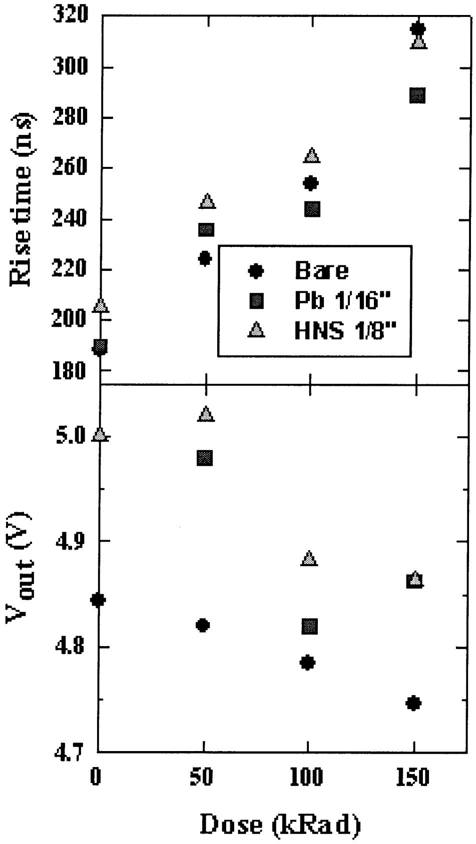

Fig. 4. Rise time and output voltage as a function of TID for HCF4081BE CMOS components contained in bare polyethylene vials (circles), in vials coated with a 1/16 in thick Pb sheet (squares), and in vials coated with a 1/8 in thick HNS polymer. Data refer to input square wave frequency of 1000 kHz.

IV. EXAMPLE RESULTS TO DATE

A representative gate bias-drain current response to TID of the MOSFETs is shown in Fig. 1. The component was placed inside a polyethylene vial, which did not attenuate the incident γ–radiation. The operational shift in the bias voltage with increasing TID is evident.

In Fig. 2, the variation in threshold voltage as a function of TID is reported for the same MOSFET component as in Fig. 1. The threshold voltage decreases nearly linearly with increasing TID, for TIDs below about 20 kRad.

The linear decay of the threshold voltage at low TIDs was employed to gauge the efficiency of the screening material. The slopes of linear best fits to the curves as those of Fig. 2 are reported in Table II for all screening materials tested in our measurements. The second column of Table II reports the changes in threshold voltage with TIDs obtained from linear fits to the low-dose section of curves like those reported in Fig. 2. These values are directly related to the efficiency of the shielding materials, lower values indicating higher shielding efficiency.

CMOS components proved more resistant to irradiation. They were exposed to higher radiation fluences and higher dose rates. Fig. 3 reports the variations induced by γ-irradiation in the rise time and voltage of the output of an AND gate of the HCF4081BE CMOS, as a function of the frequency of the input square wave. Within experimental error, the output voltage at high frequencies decreases with increasing TID. The reponse time of the CMOS (rise time) increases with increasing TIDs.

The variation of risetime and output voltage as a function of nominal TID is reported in Fig. 4 as a function of shielding material. We observe that shielding strongly affects the output voltage, but has little effect on the rise time changes. Additional measurements are planned to clarify this difference.

V. CONCLUSION

The free use and application of nonradiation hardness-qualified COTS parts in ionizing environments present a wide spectrum of potential problems encompassing individual components to systems. The wide range of functionality under irradiation is testimony to the realities of radiation performance variability and traceability. In light of these circumstances, risk avoidance is nearly impossible; rather, one should take a sound risk management approach, based on systematic testing.

UMRR is now beginning a testing program of selected COTS parts. To date, the following has been achieved:

1) completed irradiation testing of MOSFET and CMOS in bare, lead-clad and polymer clad polybromide vials,
2) in the case of the MOSFET, with increasing TID, we found that less bias (gate) voltage was required to maintain the same current level
3) the CMOS is relatively more radiation resistant; the output voltage at high frequencies decreases, and there is a higher rise time (i.e., the response time increases).
4) data concerning the shielding properties of the HNS polymer-tungsten carbide composite [2] have been acquired and they are being compared to the shielding of a Pb liner.
5) irradiation testing with a high-density polymer-depleted uranium composite is being planned.

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