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Werner Bradinal

Christoph Moeller

Timothy A. Philpot

Missouri University of Science and Technology, philpott@mst.edu

Mike Rose

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A NEW CHIP-SET FOR ASTRA DIGITAL RADIO

Werner Bradinal, Christoph Moeller, Tim Philpot and Mike Rose
Philips Semiconductors, Southampton, England

ABSTRACT

This chip-set provides the channel and source decoding functions for ASTRA¹ Digital Radio (ADR) receivers. An overview of the system is given together with a summary of the main features of the ICs. The chip-set offers a flexible, but optimum solution to meet the requirements for low cost consumer sets.

INTRODUCTION

The new ASTRA Digital Radio (ADR) system combines proven transmission technology with MPEG Audio (MPEG1, Layer II) source coding. This combination offers the potential for a large number of digital audio channels via 64 available transponders on the ASTRA 1A-1D satellites. With an installed base of around 17 million satellite dishes in Europe, ADR opens up an exciting new market opportunity to provide consumers with a huge choice of CD quality radio channels and data services. The system offers both free-to-air and pay radio (Digital Music Express²) services, with DMX alone offering more than fifty thematically organised channels covering a broad spectrum of musical tastes.

ADR is a digital transmission system using the audio subcarriers on the ASTRA 1A-1D satellites. With the combination of QPSK subcarrier modulation, an audio data rate of 192 kbits/s per stereo channel and 48 kHz sampling frequency, the system can deliver wide audio bandwidth (20 Hz to 20 kHz) with a dynamic range of >90 dB.

Figure 1 shows the block diagram of an ADR receiver built around the new chip-set, complete with smart card interface block for the pay-radio service. The complete demodulation, decoding and audio processing function has been split between two ICs:

- ADR/DMX digital receiver³
- MPEG Audio source decoder⁴

This functional partitioning has been chosen so that the dedicated ADR functions are all contained within one IC

1. ASTRA is a trademark of Société Européenne des satellites
2. DMX is a trademark of Digital Music Express
3. This IC is commercially available as SAA2530
4. This IC is commercially available as SAA2502

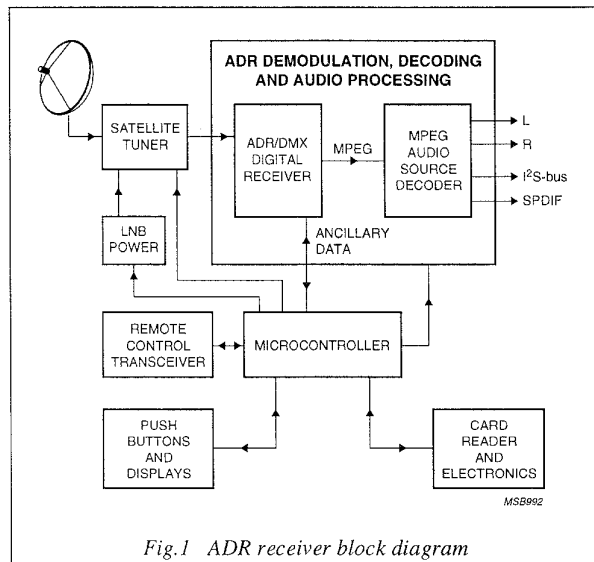


Fig.1 ADR receiver block diagram

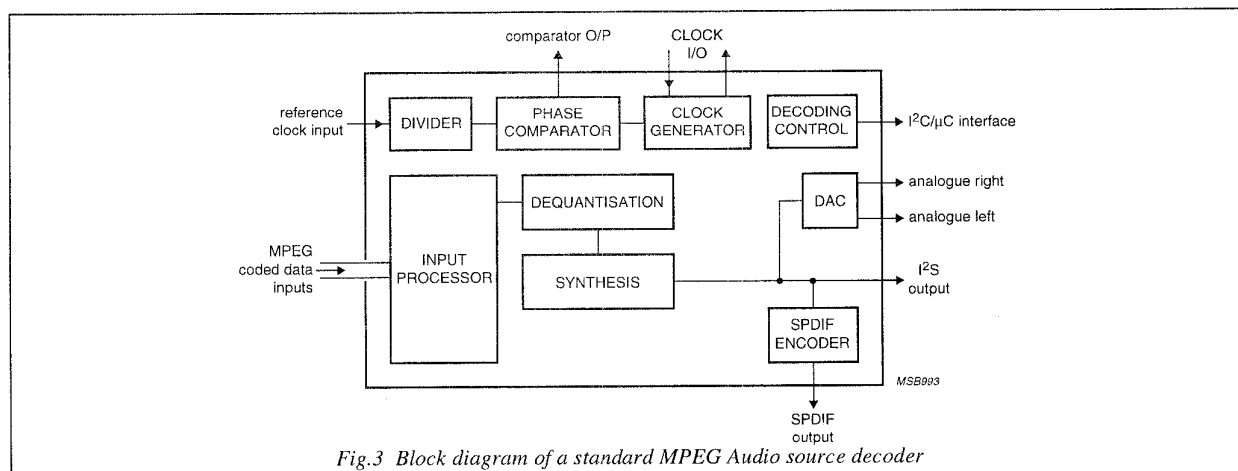
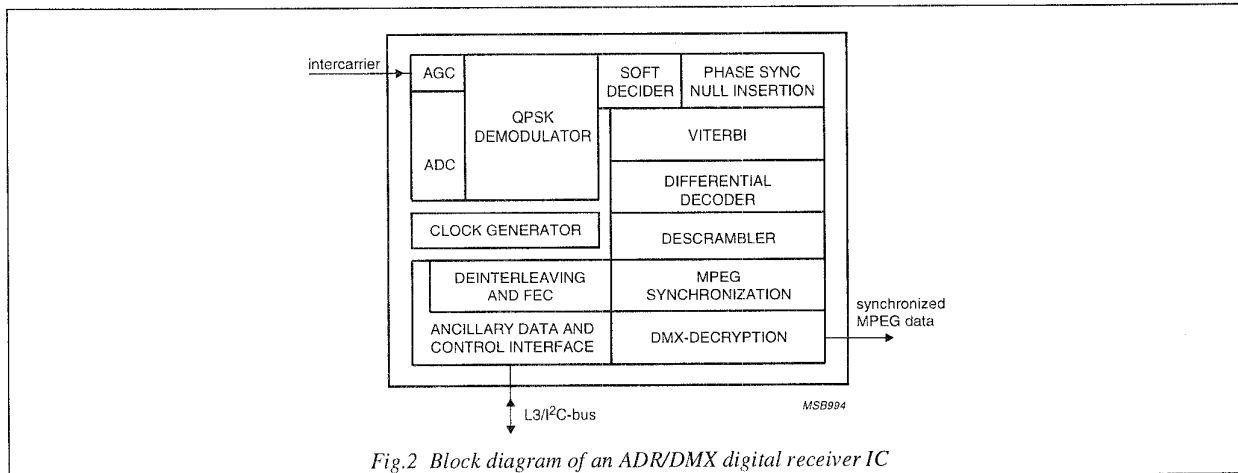
and a 'standard' MPEG Audio decoder can be used for source decoding/audio processing.

CHANNEL DECODING FUNCTION

The block diagram of the ADR/DMX digital receiver IC is shown in Figure 2. The device accepts the ADR baseband Sound IF (SIF) input signal from a standard satellite tuner. Automatic gain control (AGC) is applied to the input amplifier to ensure that the 8-bit Flash analog-to-digital converter is always driven with the optimum input level.

A narrowband QPSK demodulator performs subcarrier selection, matched filtering, carrier and symbol locking to generate in-phase (I) and quadrature (Q) components. These I/Q signals are then fed to the Viterbi decoder block which performs forward error correction (FEC). This is followed by the differential decoding and descrambling of the data stream.

In order to receive a DMX pay-radio transmission the data stream must also be processed by the decryption block within the IC. The decoded (de-interleaved and forward error corrected) ancillary data is output for processing by the system microcontroller. The MPEG Audio output interface provides data, clock and synchronization information to the sound decoder.



SOURCE DECODING

The MPEG Audio data stream is processed by a 'standard' source decoder. The device proposed for this chip-set (see Fig.3) offers a number of features and benefits which are particularly important for ADR receivers. These include:

- CRC protection of scale factors
- internal dynamic range compression algorithm
- analog audio output
- SPDIF and I²S outputs
- low power consumption
- programmable audio post-processor.

The MPEG Audio data stream is processed using the slave mode input. A 256f_s (12.288 MHz) clock is supplied from the ADR/DMX channel decoder IC.

SYSTEM CONTROL

The chip-set supports both the L3 and I²C microcontroller

interface protocols. The required protocol is selected during initialization or by a hardware reset. The microcontroller interface requires three signals/pins; a data I/O, a bit clock and mode select. The I²C-bus interface can support data clock rates up to 400 kHz, whilst the microcontroller itself will normally be the limiting factor for the high speed L3 protocol.

The system software control is relatively straightforward, with many of the tasks being handled by the hardware (after initialisation).

CONCLUSION

A new chip-set for ADR signal processing has been described. The ADR specific functions have been implemented in a single channel decoding IC, whilst source decoding is handled by a general purpose MPEG Audio decoder IC. Together, these two ICs offer a very cost-effective (dedicated hardware) solution for receiver manufacturers.