12-1-2005

Reliability Measurement of Mass Storage System for Onboard Instrumentation

Minsu Choi
Missouri University of Science and Technology, choim@mst.edu

Nohpill Park

Vincenzo Piuri

Fabrizio Lombardi

Recommended Citation

M. Choi et al., "Reliability Measurement of Mass Storage System for Onboard Instrumentation," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 6, pp. 2297-2304, Institute of Electrical and Electronics Engineers (IEEE), Dec 2005.
The definitive version is available at https://doi.org/10.1109/TIM.2005.858514

Reliability Measurement of Mass Storage System for Onboard Instrumentation

Minsu Choi, *Member, IEEE*, Nohpill Park, *Member, IEEE*, Vincenzo Piuri, *Fellow, IEEE*, and Fabrizio Lombardi, *Member, IEEE*

***Abstract*—Advances in spaceborne vehicular technology have made possible the long-life duration of the mission in harsh cosmic environments. Reliability and data integrity are the commonly emphasized requirements of spaceborne solid-state mass storage systems, because faults due to the harsh cosmic environments, such as extreme radiation, can be experienced throughout the mission. Acceptable dependability for these instruments has been achieved by using redundancy and repair. Reconfiguration (repair) of memory arrays using spare memory lines is the most common technique for reliability enhancement of memories with faults. Faulty cells in memory arrays are known to show spatial locality. This physical phenomenon is referred to as *fault clustering*. This paper initially investigates a *quadrat-based fault model* for memory arrays under clustered faults to establish a reliable foundation of measurement. Then, lifelong dependability of a fault-tolerant spaceborne memory system with hierarchical active redundancy, which consists of spare columns in each memory module and redundant memory modules, is measured in terms of the reliability (i.e., the conditional probability that the system performs correctly throughout the mission) and mean-time-to-failure (i.e., the expected time that a system will operate before it fails). Finally, minimal column redundancy search technique for the fault-tolerant memory system is proposed and verified through a series of parametric simulations. Thereby, design and fabrication of cost-effective and highly reliable fault-tolerant onboard mass storage system can be realized for dependable instrumentation.**

***Index Terms*—Clustered faults, hierarchical active redundancy, mean-time-to-failure (MTTF), memory reconfiguration (repair), onboard mass storage system, quadrat-based fault model, redundancy minimization, reliability.**

I. Introduction

ADVANCES in spaceborne vehicular technology have made possible the long-life duration of missions in harsh cosmic environments [10]–[12]. Reliability and data integrity are commonly emphasized requirements of spaceborne solid-state mass storage systems, because faults due to the harsh cosmic environments, such as extreme radiation, can be experienced throughout the mission [10]–[12]. Acceptable dependability for these solid-state mass storage instruments has been commonly achieved by using redundancy and repair. Reconfiguration (repair) of memory arrays using spare memory lines is the most common technique for reliability enhancement of memories with faults [1], [2], [4]–[7].

Mainly, three different fault mechanisms can occur in cosmic environment: single event upsets (SEUs), total ionizing dose (TID), and displacement damage (DD) [8], [9]. SEUs cause transition faults (i.e., temporary faults) in random locations. Normally, error detection and correction codes resolve SEU issues. However, TID, mostly due to electrons and protons, can result in device degradation and failure. Also, DD is caused due to cumulative long-term nonionizing damage from protons, electrons and neutrons and can result in lattice defects; the collision between an incoming particle and a lattice atom subsequently displaces the atom from its original lattice position. Interestingly, defects due to DD tend to form clusters [9]. Also, continuous and cumulative TID accelerate this clustering of defects. Thus, random fault models are usually exploited in modeling SEUs, while cluster fault models are more suitable in modeling permanent faults due to TID and DD.

To accurately model the faulty memory arrays, a proper fault model must be introduced. It is well known that defects in VLSI circuits tend to occur in clusters due to defects that span multiple circuit elements [4], [5], [13], [15]. This physical phenomenon is referred to as *defect clustering*. Attempts to deal with defect clustering have focused mainly on the models involving compounded Poisson distributions [4], [5], [15]. In these models, the wafer is divided into multiple regions and the distribution of the defects within each region is assumed to follow the Poisson distribution. Models that use compounded distributions are quadrat-based because they assume different distributions in different regions (quadrats) of the wafer. For quadrat-based models, defects occur s-dependently in the same quadrat, while occurrences of defects in different quadrats are s-independent (i.e., statistically independent) [4]. An alternative approach to modeling defects is the center-satellite approach [13] wherein there are separate distributions describing the locations of cluster centers and the locations of defects within a cluster. While some aspects of the center-satellite approach make it quite well-suited for modeling defect clustering, the resulting models can have more parameters, making the problem of parameter estimation more complex than in quadrat-based models [4]. The quadrat-based fault clustering model makes it possible to accurately measure the reliability of memory arrays with clustered faults without excessive complexity.

Solid-state mass memories for spaceborne applications may experience excessive interference and damage due to harsh cosmic environments [10]–[12]. In [10], error correcting codes are used to cope with particle-induced bit errors—an extended

Manuscript received July 16, 2003; revised May 31, 2005.

M. Choi is with the Department Electrical and Computer Engineering, University of Missouri-Rolla, Rolla, MO 65409 USA (e-mail: choim@umr.edu).

N. Park is with the Department of Computer Science, Oklahoma State University, Stillwater, OK 74078-1053 USA (e-mail: npark@a.cs.okstate.edu).

V. Piuri is with the Department of Information Technologies, University of Milan, 26013 Crema, Italy (e-mail: piuri@dti.unimi.it).

F. Lombardi is with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115 USA (e-mail: lombardi@ece.neu.edu).

Digital Object Identifier 10.1109/TIM.2005.858514

Reed-Solomon code circumvents soft errors while maintaining a low-hardware implementation of coding and checking. The memory system proposed in [11] is also designed for space-borne applications and uses two levels of active redundancy, where faulty columns in a memory module are repaired by spare columns and malfunctioned modules are replaced by module redundancy. Circuits for radiation-hardened memories are also introduced in [12], where an orthogonal shuffle-type of write-read arrays, error correction through weighted bidirectional codes, and associative iterative repair circuits are exploited to harden memories against interference and damage due to excessive radiation.

The objective of this paper is to thoroughly measure the dependability of a fault-tolerant onboard memory system under fault clustering, and achieve more accurate prediction of reliability (i.e., the conditional probability that the system performs correctly throughout a time interval) and mean-time-to-failure (MTTF, i.e., the expected time that a system will operate before it fails). Thereby, the more dependable mission-specific onboard mass storage systems can be realized with respect to reliability and MTTF while maintaining minimal redundancy.

The organization of this paper is as follows. In Section II, review and preliminaries related to this research work will be given. In Section III, a fault-tolerant memory system with two levels of active redundancy proposed in [11] is reviewed. Reliability measurements for nonfault-tolerant and fault-tolerant memory modules with a clustered fault model are discussed in Sections IV and V, respectively. Reliability measurement of a fault-tolerant onboard memory system consisting of such fault-tolerant memory modules is investigated in Section VI. Parametric simulation and its results are given in Section VIII. Discussion and conclusions are in the final section.

II. Review and Preliminaries of Clustered Fault Model

In this Section, the clustered memory fault model proposed by Blough, *et al.* [4], [5], will be briefly reviewed. The following notations are used throughout this work.

- n: number of rows and columns in an array, excluding spares.
- A_n: a $n \times n$ memory array with n rows and n columns.
- s: number of spare columns.
- $a_{i,j}$: an element of A_n.
- m_n: number of rows and columns in a quadrat.
- η: n/m_n.
- $\Pr\{\langle \text{condition} \rangle\}$: conditional probability of the given condition.
- p_1: $\Pr\{\text{a quadrat is FP}\}$ (see below).
- p_2: fault arrival rate (i.e., the conditional probability of becoming a faulty cell in a unit time period) of a memory cell within FP (i.e., fault-prone) quadrat.
- p_3: fault arrival rate of a memory cell within FR (i.e., fault-resistant) quadrat (see below).
- λ: parameter of a Poisson random variable.
- M: number of fault-free memory modules required for the system to be functional.
- N: number of total memory modules including spare modules.
- S: $N - M$ (i.e., number of redundant modules).
- t: time.
- R: reliability, the conditional probability that the system performs correctly throughout Δt.

The following assumptions are made in this work.

1) Quadrats can be one of two types: *fault prone quadrat* (denoted by FP) and *fault resistant quadrat* (denoted by FR). FPs are prone to have faults while FRs resists faults.
2) Within any quadrat, faults occur s-independently.
3) A quadrat is FP with probability p_1, s-independently of other quadrats.
4) Occurrence of faults in FP quadrats is determined by p_2.
5) Occurrence of faults in FR quadrats is determined by p_3.
6) $p_2 \gg p_3$ and $p_3 \approx 0$.
7) $(1 - p_1) \gg p_1$ and $(\eta \cdot p_1) \leq 1$.
8) η is an integer.

For memory arrays, some of the most challenging problems are the achievement of acceptable reliability and the minimization of redundancy area (overhead) [1], [2], [4], [5], [14]. If more redundancy area is provided, a highly reliable memory reconfiguration is possible, but more cost due to the additional redundancy overhead is unavoidable. Thus, an appropriate balance of acceptable reliability and redundancy area is desirable for high-reliability, low-cost manufacturing of memory arrays for space applications.

In this paper, a $n \times n$ memory array, A_n, is partitioned into quadrats containing $m_n \times m_n$ cells. Assumptions given above determine the occurrence patterns of faults within such an array. Assumption (1) defines what it means for a quadrat to be FP or FR: The array is divided into *quadrats with a high density of faulty cells* and *quadrats with a low density of faulty cells*. The *a priori* probability of a cell being faulty is $p_1 \cdot p_2 + \overline{p}_1 \cdot p_3$. However, if some of the neighbors of a cell are known to be faulty, the probability of that cell's being faulty increases toward p_2 since it is more likely that the cell lies in a FP quadrat. Fig. 1 illustrates the effect of the Clustered-Fault model. Fig. 1(a) uses the quadrat-based fault model with $n = 16$, $m_n = 4$, $p_1 = 0.1$, $p_2 = 0.5$ and $p_3 = 0.02$ to generate the faulty memory array. Fig. 1(b) uses a random fault model with $\text{failure} - \text{probability} = 0.068$ which was chosen to make the expected number of faults the same in both illustrations.

A faulty column (row) containing more than one faulty cell is referred to as *connective faulty column (CFC) (CFR)* [2]. The memory array in Fig. 1(a) has eight CFCs and the one in Fig. 1(b) has 14 CFCs. Importance of the fault-clustering is shown in Fig. 2, wherein both of the faulty memory arrays in Fig. 1 are repaired by spare columns. The memory array given in Fig. 2(a) requires eight spare lines while the memory given in Fig. 2(b) needs 14 spare lines.

The average number of faulty cells covered by one spare line is referred to as *covering ratio*. For example, covering ratio of the reconfiguration given in Fig. 2(a) is 2.25 while covering ratio of the other reconfiguration given in Fig. 2(b) is 1.2857. It is quite intuitive that fewer spare lines would be required to repair a given memory array if faulty cells show spatial locality (i.e., fault clustering).

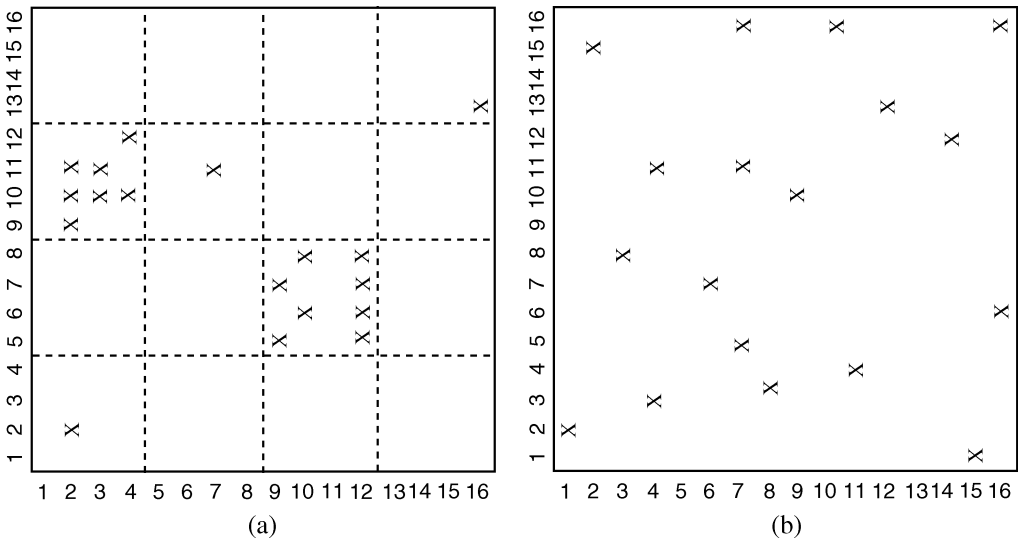

Fig. 1. Fault arrays generated with (a) clustered-fault model and (b) random-fault model [4], [5].

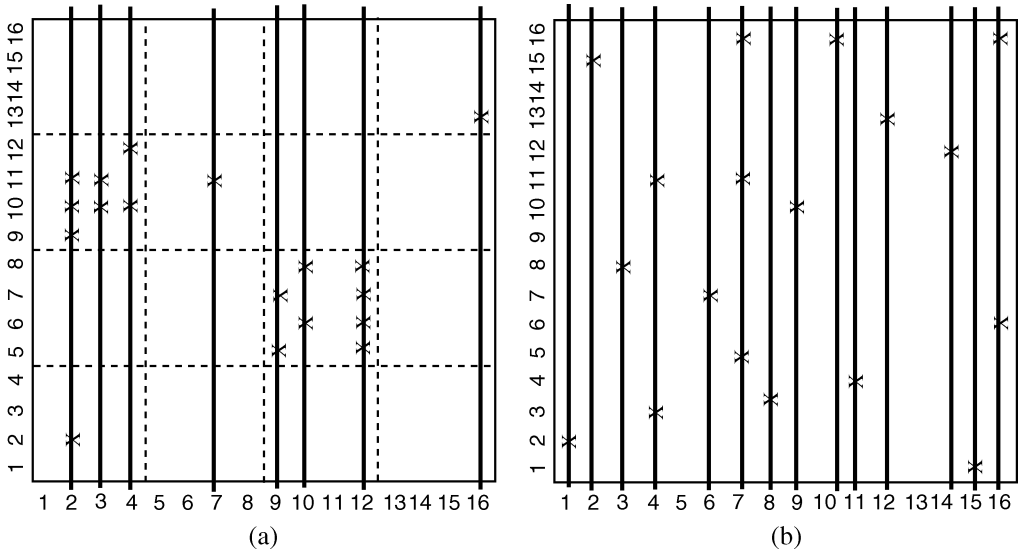

Fig. 2. Repaired fault arrays generated with (a) clustered-fault model and (b) random-fault model.

III. Fault-Tolerant Onboard Memory Architecture

In this section, a fault-tolerant memory system with two levels of active redundancy proposed in [11] is reviewed. A total of $N-M=S$ spare memory modules are provided in the system and each spare module can substitute for any of the M primary memory modules. Consequently, the memory system can tolerate up to S complete memory module failures before the memory system becomes inoperable. Each $n \times n$ module has s spare columns to repair faulty memory columns, if any. If a memory cell fails, then the column containing that cell is eliminated from the system and replaced with a spare column. If the memory module runs out of spare columns, then the entire module is replaced with a spare module. This type of redundancy is often referred to as *two-level redundancy*: The first level being the spare columns and the second level being the spare memory modules. Both forms of reconfiguration are active techniques, and they require that the fault be detected, located, and successfully removed from the system. Fig. 3 shows the architecture of the fault-tolerant memory system for spaceborne applications. A detailed description of the architecture can be found in [11]. In the following sections, the reliability of the given fault-tolerant onboard memory system under fault clustering will be modeled and measured.

IV. Reliability Measurement of Nonfault-Tolerant Memory Module With Clustered Faults Model

The given $n \times n$ memory module A_n has η^2 quadrats. For example, memory module shown in Fig. 1 can be parameterized as $n=16$, $m_n=4$ and $\eta=4$. A quadrat is FP with probability p_1, s-independently of other quadrats. $\Pr\{\text{quadrat is FP}\}=p_1$ and $\Pr\{\text{quadrat is FR}\}=\overline{p}_1$, formally. Fault arrival rate in a FP quadrat is $\lambda_{FP}=p_2\cdot m_n^2$ and fault arrival rate in a FR quadrat is $\lambda_{FR}=p_3\cdot m_n^2$. Then, reliability of a FP is determined by the exponential failure law $R_{FP}(t)=e^{-\lambda_{FP}t}$ and reliability of a FR is $R_{FR}(t)=e^{-\lambda_{FR}t}$. Each column of quadrats in the given memory array is referred to as

quadrat-column where each quadrat-column has η quadrats. Since $\Pr\{\text{quadrat is FP}\} = p_1$ and $\Pr\{\text{quadrat is FR}\} = \overline{p}_1$, the expected number of FP quadrats in a quadrat-column is $p_1 \cdot \eta$ and the expected number of FR quadrats in a quadrat-column is $\overline{p}_1 \cdot \eta$. Therefore, the reliability of a quadrat-column is

$$\begin{aligned} R_{QC}(t) &= (p_1 e^{-\lambda_{FP} t} + \overline{p}_1 e^{-\lambda_{FR} t})^{\eta} \\ &\approx (R_{FP}(t))^{p_1 \cdot \eta} \cdot (R_{FR}(t))^{\overline{p}_1 \cdot \eta}. \end{aligned} \tag{1}$$

Finally, overall reliability of a nonfault-tolerant memory module A_n becomes

$$R_{\mathrm{NFTA}_n}(t) = (R_{QC})^{\eta}. \tag{2}$$

V. Reliability Measurement of Fault-Tolerant Memory Module With Clustered Fault Model

The given memory array A_n consists of approximately $\eta^2 \cdot p_1$ FP quadrats and $\eta^2 \cdot \overline{p}_1$ FR quadrats. For each FP quadrat, $\Pr\{\text{a column in FP quadrat is faulty}\}$ is

$$1 - \Pr\{\text{a column in FP quadrat is fault-free}\} = 1 - (1 - p_2)^{m_n}. \tag{3}$$

Furthermore, the expected number of faulty columns in a FP quadrat becomes

$$m_n \cdot (1 - (1 - p_2)^{m_n}). \tag{4}$$

Since $p_2 \gg p_3$, $\eta \cdot p_1 \leq 1$, and $p_3 \approx 0$, the FR quadrats are essentially fault-free and the FP quadrats primarily dictate the locations of the faulty cells. Hence, the expected number of faulty columns in a quadrat-column is primarily determined by the faulty columns in FP quadrats. Thus, the expected number of faulty columns in a quadrat-column is

$$\lambda_{QC} \approx m_n \cdot (1 - (1 - p_2)^{m_n \cdot \eta \cdot p_1}) \tag{5}$$

and the overall expected number of faulty columns in a memory module A_n becomes

$$\lambda_{A_n} = \lambda_{QC} \cdot \eta. \tag{6}$$

Hence, the failure rate of a single column can be estimated as

$$\lambda_{\mathrm{col}} = \frac{\lambda_{A_n}}{n} \tag{7}$$

and the reliability of a single column can be expressed as

$$R_{\mathrm{col}}(t) = e^{-\lambda_{\mathrm{col}} t}. \tag{8}$$

Each memory module consists of n memory columns and s spare memory columns and a quorum of n out of the total of $n + s$ columns are required to function for the memory module to function. Thus, the reliability of the fault-tolerant memory module with s spare columns can be written as

$$R_{FTA_n}(t) = \sum_{i=0}^{s} \binom{n+s}{i} R_{\mathrm{col}}(t)^{n+s-i} \cdot (1 - R_{\mathrm{col}}(t))^{i} \tag{9}$$

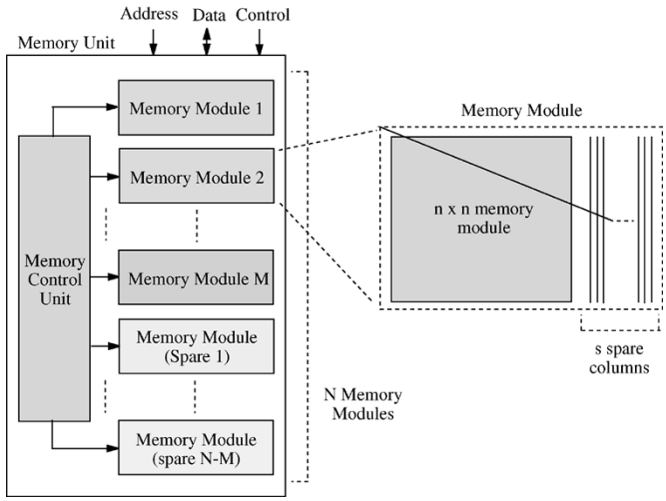

Fig. 3. Architecture of fault-tolerant onboard memory system.

$$\approx e^{-\lambda_{A_n}(n+s)} \cdot \sum_{i=0}^{s} \frac{(\lambda_{A_n}(n+s))^{i}}{i!}. \tag{10}$$

VI. Reliability Measurement of the Fault-Tolerant Onboard Memory System

The fault-tolerant onboard memory system consists of N fault-tolerant memory modules and M of these memory modules must be functional, where column failures of each module are repaired by spare columns and failed modules are replaced by spare modules. The system uses two levels of hierarchical active redundancy. Therefore, reliability of the given fault-tolerant memory system can be expressed as

$$R(t) = \sum_{i=0}^{N-M} \binom{N}{i} R_{FTA_n}(t)^{N-i} \cdot (1.0 - R_{FTA_n}(t))^{i}. \tag{11}$$

In addition to the reliability, the mean time to failure (MTTF) is a useful measurement to specify the quality of a system since the MTTF is the expected time that a system will operate before the first failure occurs. Therefore, it can be used to measure the system operation life without failure. The MTTF is defined in terms of the reliability function as

$$\mathrm{MTTF} = \int_0^{\infty} R(t) dt \tag{12}$$

which is valid for any reliability function that satisfies $R(\infty) = 0$.

VII. Redundancy Optimization of Onboard Memory System Under Fault Clustring

As shown in Fig. 3, the onboard memory system overcomes s column-wise permanent faults and S module-wise permanent faults by exploiting two-level hierarchical active redundancy technique. Embedding balanced amount of redundancy

TABLE I
SUMMARY OF SIMULATION PARAMETERS

Parameter	n	n^2	η	s	M	S	$M \times n^2$	p_1	p_2
Value	128	16K	32	variable	16	variable	256K	5×10^{-4}	5×10^{-3}

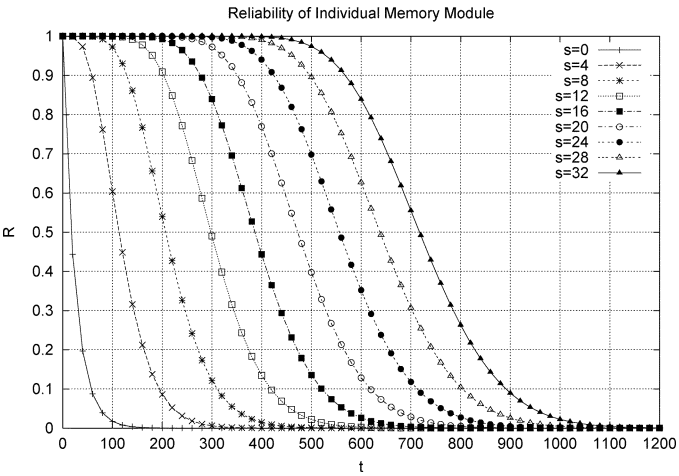

Fig. 4. Reliability of individual memory module.

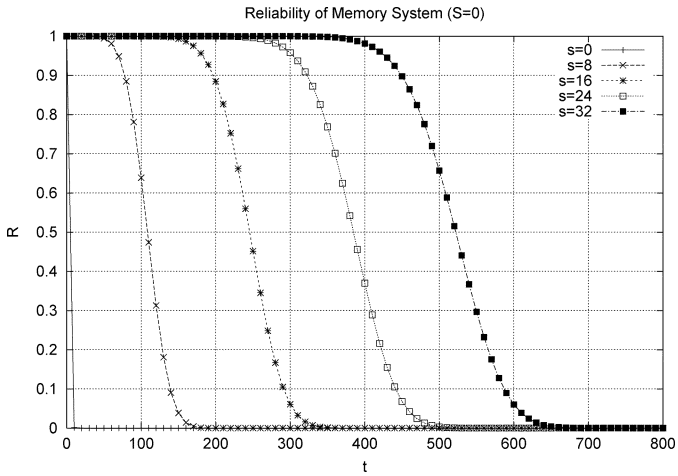

Fig. 5. Reliability of memory system without module redundancy.

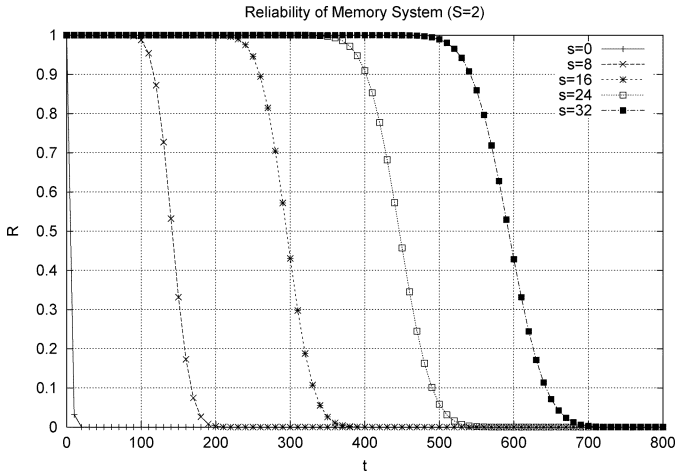

Fig. 6. Reliability of memory system with two redundant modules.

makes possible to achieve acceptable reliability of the memory subsystem while minimizing the cost due to the redundancy. Finding the minimum amount of redundancy which guarantees desired reliability throughout the required system life time is referred to as "*redundancy optimization*." Let t_{system} be the system life time and R_{system} be the minimum reliability which must be guaranteed at the end of the t_{system}; therefore, the following inequality must hold:

$$R(t_{\text{system}}) \geq R_{\text{system}}. \tag{13}$$

Thus, the following equation can be solved with respect to s to find the minimum number of spares required to achieve the given constraints (i.e., t_{system} and R_{system}):

$$R(t_{\text{system}}) - R_{\text{system}} \geq 0. \tag{14}$$

Since s must be an integer value, $s_{\text{minimal}} = \lceil s \rceil$ spares must be embedded.

VIII. PARAMETRIC SIMULATION

The effect of the fault clustering and redundancy on the reliability of the fault-tolerant memory system will be studied through numerical experiments in this section. Parameters used in this simulation are summarized in Table I. The unit time interval is a week.

In Fig. 4, the reliability enhancement ability of spare column redundancy in a memory module is visualized. R of the nonfault-tolerant memory module $(s = 0)$ calculated by the (2) along with R of the fault-tolerant memory module with different numbers of spare columns from 4 to 32 calculated by the (9) are shown. Note that $R_{\text{NFTA}_n}(1) = 0.960\,161\,458\,504\,244$ and $R_{\text{NFTA}_n}(2) = 0.921\,910\,026\,397\,004$, which means that reliability of the nonfault-tolerant memory module becomes less than 0.95 in two weeks. Typical requirements of a long-life application are to have a 0.95, or greater, the probability of being operational at the end of a ten-year period. Thus, the nonfault-tolerant memory module must be hardened to be operational for longer mission time. In the case of $s = 32$ (i.e., 32 spare columns are provided), $R_{FTA_n}(530) = 0.950\,083\,569\,136\,458$ and $R_{FTA_n}(531) = 0.949\,069\,751\,640\,994$ where it successfully endures more than 10 years of mission time while maintaining $R_{FTA_n} > 0.95$ at 25% (i.e., $32/128 = 0.25$) redundancy overhead.

In Figs. 5–8, the reliability enhancement ability of module redundancy in a memory system is investigated. Each figure has five plots varying the number of spare columns from 0 to 32. For example, $S = 6$ and $s = 32$ means that the memory system consists of $16 + 6 = 22$ total modules, including spare modules, and each module has 32 spare columns. For the memory system with no redundancy (i.e., $S = 0$ and $s = 0$), $R(1) = 0.521\,805\,083\,796\,637$, which means it would not maintain $R > 0.95$ for even a week. If 32 spare columns are applied, the memory system will maintain $R > 0.95$

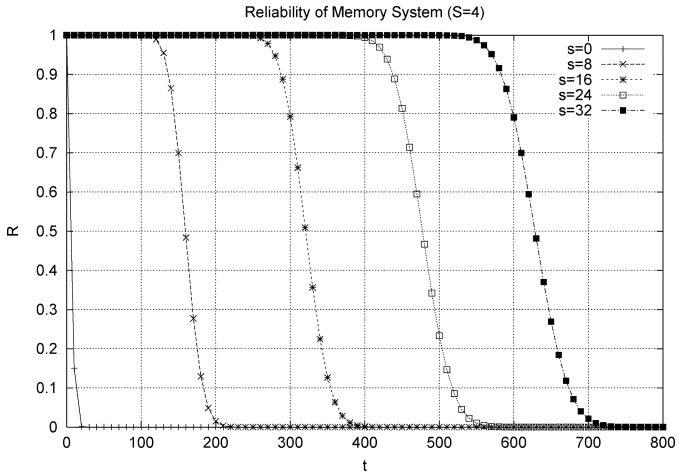

Fig. 7. Reliability of memory system with four redundant modules.

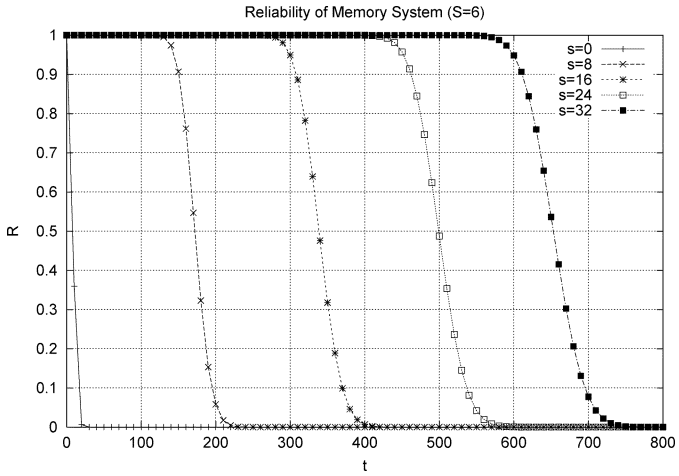

Fig. 8. Reliability of memory system with six redundant modules.

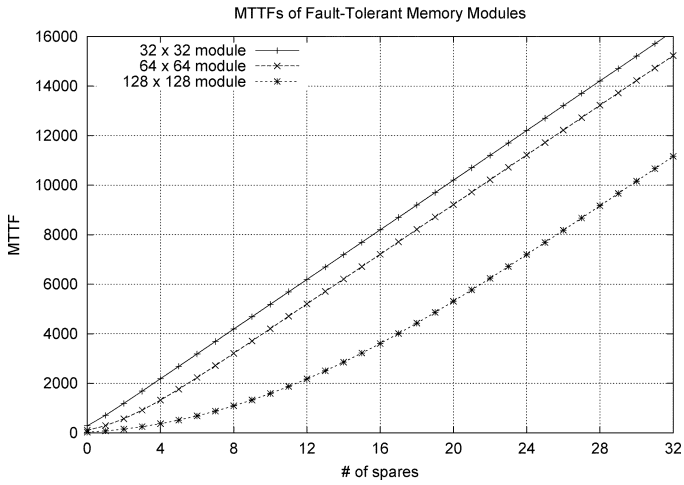

Fig. 9. MTTFs of fault-tolerant memory modules.

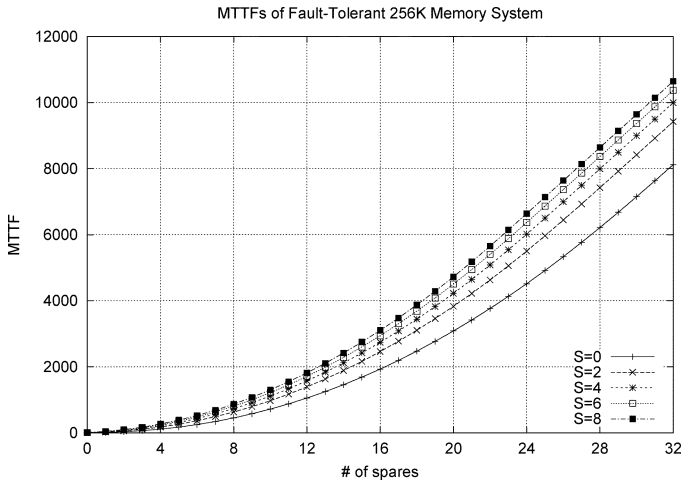

Fig. 10. MTTFs of fault-tolerant 256 K memory system.

for about 9 years since $R(428) = 0.950\,233\,141\,259\,701$ and $R(429) = 0.948\,538\,560\,295\,286$. The reliability of the memory system can be further enhanced by exploiting module redundancy. The memory system with $s = 32$ and $S = 6$ satisfies the requirement of $R > 0.95$ for more than 12 years because $R(599) = 0.951\,682\,181\,131\,270$ and $R(600) = 0.948\,490\,237\,398\,006$. To meet $R > 0.95$ for ten years, the minimal overhead of these systems is with $S = 2$ and $s = 32$.

Another useful measurement of the fault-tolerant onboard memory system quality is mean-time-to-failure (MTTF), which is the expected time that a system will operate before a failure occurs. Fig. 9 shows MTTFs of three different memory module configurations of 32 × 32, 64 × 64, and 128 × 128 with different numbers of spare columns from 0 to 32. For example, $\mathrm{MTTF}_{A_n} = 25.101\,321$ for 32 × 32 memory module without spare columns, which implies that the expected time that the memory module will operate before a failure occurs is only about 25 weeks while the same memory module with 32 spare columns exceeds MTTF≈ 16 000 weeks.

MTTFs of the 256 K nonfault-tolerant (i.e., $s = 0$ and $S = 0$) and fault-tolerant memory systems with various combinations of s and S (i.e., from 1 to 32 for s and from 2 to 8 for S) are given in Fig. 10. MTTF of the nonfault-tolerant memory system, 2.091 197 weeks, can be extended to 10 643.743 596 weeks by use of the two-level active redundancy of $s = 32$ and $S = 6$. Thus, the results shown in Figs. 9 and 10 confirm the fault-tolerant ability of the two-level active redundancy technique.

Finally, the number of spare columns can be optimized by the proposed *redundancy optimization* technique. Optimized redundancy guarantees desired reliability during the required life time of the system at minimal redundancy overhead. In Fig. 11, $R_{\mathrm{system}} = 0.9$ and $S = 0$, 2, 4, 8 and $t_{\mathrm{system}} = 100$, 200, 300, 400, 500, 600, 700 are applied to the (14) to search s_{minimal}s. For example, to maintain reliability more than 0.90 for 700 weeks, s_{minimal} must be 36. Fig. 12 also shows results for $R_{\mathrm{system}} = 0.95$.

As shown in this section, intelligent exploitation of the proposed measurement estimation technique makes possible the design and manufacture of balanced onboard memory systems satisfying reliability and mission duration requirements while maintaining minimal cost due to redundancy overhead.

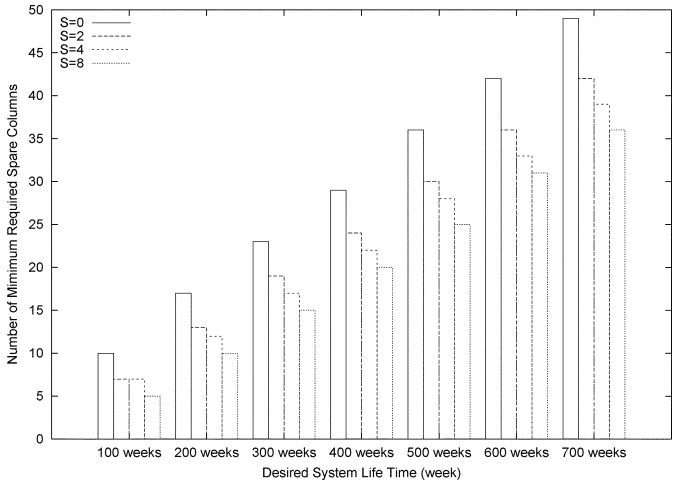

Fig. 11. Redundancy optimization results for $R_{\mathrm{system}} = 0.90$.

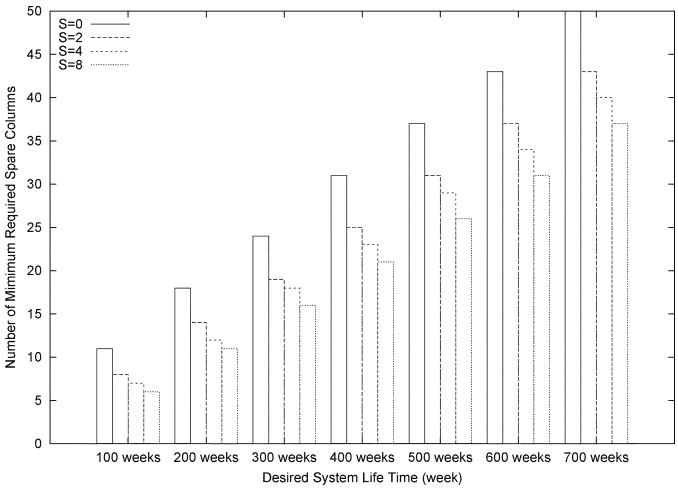

Fig. 12. Redundancy optimization results for $R_{\mathrm{system}} = 0.95$.

IX. Discussion and Conclusion

As advances in spaceborne vehicular technology make possible the long-life duration of missions in harsh cosmic environments, reliability and data integrity become commonly emphasized requirements of spaceborne solid-state mass storage systems, because faults due to the harsh cosmic environments—such as extreme radiation—can be experienced throughout the mission. In addition, it is well known that faults show spatial locality on VLSI circuits. Thus, a reliability measurement and estimation technique for the fault-tolerant onboard memory system under fault clustering has been proposed and validated throughout the parametric simulation in this paper. Thereby, intelligent exploitation of the proposed measurement and estimation technique makes possible the design and manufacture of balanced onboard memory systems satisfying the reliability and mission duration requirements while maintaining minimal redundancy. For example, according to the simulation results given in this paper, the sample 256 K fault-tolerant onboard memory system with 32 spare columns in each memory module and 6 redundant modules has higher probability than 0.95 of being operational after 10 year period and its mean-time-to-failure (MTTF) exceeds 232 years.

References

[1] C. P. Low and H. W. Leong, "A new class of efficient algorithms for reconfiguration of memory arrays," *IEEE Trans. Comput.*, vol. 45, no. 5, pp. 614–618, May 1996.

[2] N. Park and F. Lombardi, "Repair of memory arrays by cutting," in *Proc. Memory Technology, Design and Testing, Proceedings International Workshop*, Aug. 1998, pp. 124–130.

[3] K. Arndt and C. Narayan *et al.*, "Reliability of laser activated metal fuses in DRAMs," in *Proc. 24th IEEE/CPMT Electronics Manufacturing Technology Symp.*, Oct. 1999, pp. 389–394.

[4] D. M. Blough, "Performance evaluation of a reconfiguration-algorithm for memory arrays containing clustered faults," *IEEE Trans. Rel.*, vol. 45, no. 2, pp. 274–284, Jun. 1996.

[5] D. M. Blough and A. Pelc, "A clustered failure model for the memory array reconfiguration problem," *IEEE Trans. Comput.*, vol. 42, no. 5, pp. 518–528, May 1993.

[6] Y. Jeon, Y. Jun, and S. Kim, "Column redundancy scheme for multiple I/O DRAM using mapping table," *Electron. Lett.*, vol. 36, no. 11, May 2000.

[7] R. J. McPartland and D. J. Loeper *et al.*, "SRAM embedded memory with low cost, FLASH EEPROM-switch-controlled redundancy," in *Proc. IEEE Custom Integrated Circuits Conf.*, vol. 36, May 2000, pp. 287–289.

[8] E. J. Daly, A. Hilgers, G. Drolshagen, and H. D. R. Evans, "Environment analysis: experience and trends," presented at the ESA Symp. Environment Modeling for Space-Based Applications, Sep. 1996.

[9] NASA Jet Propulsion Lab., Pasadena, CA. Space Radiation Effects on Microelectronics (Online Document). [Online]. Available: http://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf

[10] T. Fichna, M. Gartner, F. Gliem, and F. Rombeck, "Fault-tolerance of spaceborne semiconductor mass memories," in *Proc. 28th Annu. Int. Symp. Fault-Tolerant Computing*, 1998, pp. 408–413.

[11] K. A. Clark and B. W. Johnson, "A fault-tolerant solid-state memory for spaceborne applications," in *Proc. Government Microelectronics Applications Conf.*, November 1992, pp. 441–444.

[12] T. P. Haraszti, R. P. Mento, N. E. Moyer, and W. M. Grant, "Novel circuits for radiatation hardened memories," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 5, pp. 1341–1351, Oct. 1992.

[13] F. J. Meyer and D. K. Pradhan, "Modeling defect spatial distribution," *IEEE Trans. Comput.*, vol. 38, no. 4, pp. 538–546, Apr. 1989.

[14] S. Y. Kuo and W. K. Fuchs, "Efficient spare allocation in reconfigurable arrays," *IEEE Design and Test*, pp. 24–31, Feb. 1987.

[15] C. H. Stapper, "On yield, fault distributions, and clustering of particles," *IBM J. Res. Develop.*, vol. 30, no. 3, pp. 326–338, May 1986.

Minsu Choi (M'02) received the B.S., M.S., and Ph.D. degrees in computer science from Oklahoma State University, Stillwater, in 1995, 1998, and 2002 respectively.

He is currently with Department of Electrical and Computer Engineering, University of Missouri, Rolla, as an Assistant Professor. His research mainly focuses on computer architecture and VLSI, embedded systems, fault tolerance, testing, quality assurance, reliability modeling and analysis, configurable computing, parallel and distributed systems, dependable instrumentation and measurement, and autonomic computing.

Dr. Choi is a member of Sigma Xi and Golden Key National Honor Society. He was a recipient of the Don and Sheley Fisher Scholarship, in 2000, the Korean Consulate Honor Scholarship in 2001, and the Graduate Research Excellence Award in 2002.

Nohpill Park (M'99) received the B.S. degree and the M.S. degree in computer science from Seoul National University, Seoul, Korea, in 1987 and 1989, respectively, and the Ph.D. degree from the Department of Computer Science, Texas A&M University, College Station, in 1997.

He is currently an Assistant Professor in the Computer Science Department at Oklahoma State University (OSU), Stillwater. His research interests include digital systems design for reliability and reliable digital instrumentation and measurement with emphasis on modeling, analysis, and optimization techniques.

Dr. Park received the OSU Outstanding Young Investigator Award from Sigma Xi in 2003. He has been involved, as a technical program committee member, in many international symposia, conferences, and workshops sponsored by professional organizations, and he has also actively served as a referee for many archival journals.

Vincenzo Piuri (F'01) received the Ph.D. degree in computer engineering from the Politecnico di Milano, Milano, Italy, in 1989.

From 1992 to September 2000, he was an Associate Professor of operating systems at the Politecnico di Milano. Since October 2000, he has been a Full Professor of Computer Engineering at the University of Milano. He was a Visiting Professor with the University of Texas, Austin, from the summers of 1993 to 1999. His research interests include distributed and parallel computing systems, computer arithmetic, application-specific processing architectures, digital signal processing architectures, fault tolerance, neural network architectures, theory and industrial applications of neural techniques for identification, prediction, control, and signal and image processing. His original results have been published in more than 150 papers in book chapters, international journals, and proceedings of international conferences.

Dr. Piuri is a member of the ACM, INNS, and AEI. He is an Associate Editor of the IEEE TRANSACTIONS ON NEURAL NETWORKS and the *Journal of Systems Architecture*. He is Vice President of Publications for the IEEE Instrumentation and Measurement Society, Vice President of Members Activities of the IEEE Neural Networks Society, and Member of the Administrative Committee of both of the IEEE Instrumentation and Measurement Society and the IEEE Neural Network Society.

Fabrizio Lombardi (M'82) received the B.Sc. degree (Hons.) in electronic engineering from the University of Essex, Essex, U.K., in 1977, the M.S. degree in microwaves and modern optics from the Microwave Research Unit, University College London, London, U.K., in 1978, as well as the Diploma in microwave engineering in 1978, and the Ph.D. degree from the University of London in 1982.

He is currently the Chairperson of the Department of Electrical and Computer Engineering and holder of the International Test Conference (ITC) Endowed Professorship at Northeastern University, Boston, MA. He was a faculty member at Texas Technical University, Lubbock, the University of Colorado, Boulder, and Texas A&M University, College Station. He received the Visiting Fellowship at the British Columbia Advanced System Institute, University of Victoria, Victoria, BC, Canada, in 1988, the TEES Research Fellowship from 1991 to 1992 and again from 1997 to 1998, and the Halliburton Professorship in 1995. He has been involved in organizing many international symposia, conferences, and workshops sponsored by organizations such as NATO and the IEEE, as well as Guest Editor in archival journals and magazines. His research interests are fault tolerant computing, testing and design of digital systems, configurable computing, defect tolerance, and CAD VLSI. He has extensively published in these area and has edited six books.

Dr. Lombardi received the International Research Award from the Ministry of Science and Education of Japan for the period from 1993 to 1999, the 1985/1986 Research Initiation Award from the IEEE/Engineering Foundation, a Silver Quill Award from Motorola in 1996, and a Distinguished Visitor of the IEEE Computer Society for the period from 1990 to 1993. He was an Associate Editor of the IEEE TRANSACTIONS ON COMPUTERS from 1996 to 2000 and currently, he is the Associate Editor-in-Chief of the IEEE TRANSACTIONS ON COMPUTERS.