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Quality Enhancement of Reconfigurable Multichip Module Systems by Redundancy Utilization

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***Abstract*—This paper evaluates the quality effectiveness of redundancy utilization in reconfigurable multichip mode (RMCM) systems. Due to reconfigurability, the RMCM system can implement a device with different redundancy levels. A redundancy level is determined by the requirement of fault tolerance (FT) of the device under implementation which can be realized through reconfiguration. No previous work has adequately investigated the effect of utilization of redundancy on the quality-level (QL) of RMCM. In this paper, the tolerance to escape from testing is also introduced to provide more extensive and comprehensive analysis and is referred to as escape tolerance (ET). This can be achieved by utilizing an appropriate amount of redundancy and is exploited for evaluating its effect on the QL of RMCM with different utilizations of redundancy. It is shown through theoretical analysis that the coverage of testing [i.e., fault coverage (FC)] can be improved by reconfiguration. Thus, we derive the QL by relating the QL to the yield enhancement by reconfiguration, the effect of interconnection yield and ET on the QL, and the improvement in FC by reconfiguration. In the proposed approaches, appropriate combinatorial models are formulated to take into account the parameters related to the redundancy and reconfiguration process in RMCM systems. From the extensive parametric simulation results, it is shown that there exists a bound in the effectiveness of redundancy utilization (i.e., the amount of redundancy) depending on the RMCM yield and FC. Using the proposed approach, the redundancy utilization in RMCM systems can be appropriately used to enhance the QL.**

***Index Terms*—Escape-tolerance (ET), fault-tolerance (FT), field-programmable system (FPS), interconnection yield, multichip-module, quality assurance, reconfiguration, utilization.**

I. Introduction

FIELD programming systems (FPS) using field programmable gate array (FPGA) and field programmable logic device (FPLD) technologies are recently emerging as a quick-turnaround alternative to mask-programmed gate arrays of up to a few-thousand gates. The basic idea is replacing the metal interconnect which determines the functionality of the gate array with static random access memory (SRAM) based pass-gates that could be programmed for customization in the field instead of at the manufacturing site [5]. FPLDs have gained much attention because they can be cheaply mass-produced and yet customized to a particular application. They allow one FPLD to be configured to implement many circuits and the same circuit can be implemented on many different FPLDs; thu, in such a way, advances in manufacturing technology and applications can occur concurrently and independently [5]. Although significant gains have been made in FPLD architecture and in the process used to manufacture FPGA, the fact that FPLD is customizable for multipurpose use requires the existence of a few resources on the FPLD that are underutilized in many applications, resulting in it being less dense and slower than its compatible application specific integrated circuit (ASIC). The FPLD providers will always be challenged to find ways to justify the benefit of FPLDs [5].

A new way to reduce risk and time in system-level development while, retaining a high level of logic integration, lies in the use of FPGAs during all the stages of system development [14]. Especially during the prototyping stage, FPGA provides a capacity of rapid hardware emulation without the cost and delay of wire-wrapped standard device technology. However, FPSs combining a large number of FPGAs are often bulky, expensive, and slow because the inherently low integration density of FPGAs results in a large system interconnect area to be carried in the upper levels of the packaging hierarchy, such as printed circuit boards (PCBs) and back-planes, rather than in a more space effective circuit integration [6].

Multichip module (MCM) technology provides a potential to revolutionize computing [6], [13] as it can reduce the cost, increase the utility of FPS, and dramatically increase the capability of FPLD and FPS in such a way that it can cost effectively deliver four to eight times the capacity of the largest FPLDs and provide even larger reduction in the area of PCB-based FPSs [5]. The design and special advantages of the field programmable MCM (FPMCM) have been presented in [5]. A new field programmable architecture for prototyping large designs using multiple FPGAs, which offers excellent performance and cost effectiveness while retaining the immediate turnaround of FPGAs at the system level, has been proposed in [9]. MCMs have been chosen as a packaging technology not only because they offer large pin count per chip necessary for high chip utilization in a partitioned design, but also because the off-chip delays are smaller than with PCBs. In [9], due to the technological complexities of providing configurability at MCM level, a fixed, statistically-determined wiring pattern on the MCM has been chosen.

Although the standard advantages of MCM technology (smaller size, decreased power consumption, increased performance, and lower cost) can benefit FPLD, another compelling reason for moving to MCM technology is that flip-chip allows many more I/Os to be placed on a single die, removing the partitioning overhead and allowing seamless integration of

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hybrid chips of silicon separately manufactured and verified [5]. Breaking a large FPS into optimally sized chunks can greatly enhance its efficiency and cost/performance.

Due to the inherent nature of MCMs, the achievement of an acceptable assembly yield and the requirement of product quality of the reconfigurable MCM (RMCM) should also be assured [4]. There have been a few works on assuring the quality level (QL) of MCMs under various features such as uneven fault-coverage and imperfect diagnosis [4], repair process [3], and uneven known good yield [1]. Also, fault coverage enhancements in digital circuits, in particular relation to manufacturing yield (based on Williams' earlier contribution to this regard on defect level analysis), using simple but rigorous mathematical tools, such as sequential statistical analysis and stochastic analysis have been considered in [2], [10], [12].

However, different implementations of a device on RMCM may experience a wide range of QL, which cannot be readily and effectively evaluated by using the previous approaches [1], [3], [4]. Hence, a new approach should be considered to assure the QL of RMCM to take into account the effect of reconfiguration by utilizing redundancy on the QL.

Given the results of testing (i.e., the numbers of good, bad and escaped chips [4]), the QL of RMCM is determined by whether escaped chips are activated (i.e., participating in the configuration of the device under implementation) or not. Hence, the escaped chips for the device under implementation should be taken into account in evaluating the QL. Reconfiguration is conducted so the RMCM runs under different implementations, the RMCM can be reconfigured to tolerate faults on chips by utilizing redundant chips, or the RMCM can work in the hybrid way of both. A device can be implemented by utilizing a different number of chips, i.e., utilizing a different number of redundant chips on the RMCM. Thus, the redundancy utilization must be determined by trading-off the effective performance and the QL of the system as it can relate the effect of reconfiguration through redundancy on the QL.

The objective of this paper is to evaluate the quality-effectiveness of the utilization of redundancy in RMCM systems by developing a QL model which takes into account the effect of fault tolerance and reconfiguration processes on the QL and thereby ultimately achieving RMCM testing and utilization strategies for its quality enhancement.

This paper is organized as follows. In the next section, previous work on the RMCM is reviewed and basic principles and assumptions of the proposed approach are introduced. Section III describes the basic concepts of the redundancy utilization of RMCM. The proposed approach is analytically studied in Section IV. In Section V, the proposed approaches are simulated and evaluated parametrically. Final discussions and conclusions are presented in Section VI.

II. Review and Preliminaries

The application of MCM technology in FPS has been proposed in [6], where several challenges for future RMCM architectures such as parametric yield, interconnect density, thermal dissipation, and second level packaging have been discussed. In [5], the feasibility of silicon-on-silicon for 40 K-gate prototype has been demonstrated, and several advantages offered by combining MCM and FPLD technologies have been shown. The upper capacity limits for RMCM have been shown to be determined mainly by the cost and defect density of the substrate, and as the CMOS process moves into the deep-submicron range, RMCM has been shown to have even faster and denser substrates in [5].

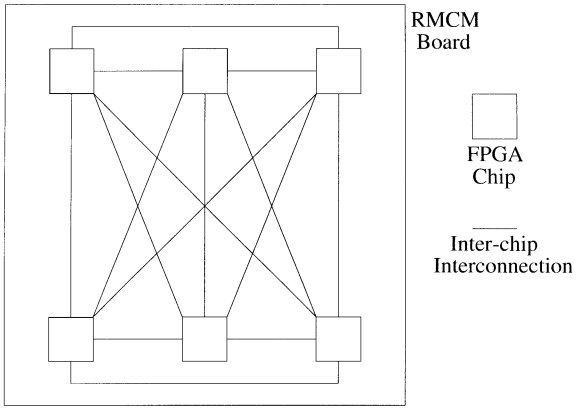

Fig. 1. Example of a fully connected structure of a RMCM.

However, commercially available FPGAs have such drawbacks to be used in RMCMs as underutilization of the FPGAs, degraded performance, severe routing constraints, and degraded routing delays [9]. Such FPGAs do not provide the high pin-to-gate ratio required when partitioning a design among multiple FPGAs; thus, as a result, the FPGAs are typically underutilized [9]. Since the I/O buffers of these chips are designed for general purpose use with PCBs, they may not achieve a better performance than MCMs [9]. The fixed MCM wiring pattern assumed in [9] imposes severe routing constraints which can be resolved by routing signals through the FPGAs themselves. Since the routing architectures of commercial FPGAs are optimized for local interconnects, the delays incurred during routing signals from one pin to another through the entire chip are too large [9]. Placing specialized switching chips on the MCM would partially avoid this problem by providing flexibility in partitioning, placement, and routing, while such centralization would increase average wire length [9]. Modified FPGAs [9] also have been proposed to support quick connections from one pin to another, thereby uniformly distributing routing resources across the chips on the MCM by surrounding the FPGA logic core with an interconnection frame which supports fast intra-chip, as well as inter-chip, connections focusing on the configuration and design of the interconnection frame in CMOS technology.

For MCMs, the effects of uneven fault-coverage and imperfect diagnosis on the QL have been shown in [4], and the repair process has been considered in evaluating the QL of MCMs in [3]. In [1], an uneven known-good-yield has been addressed and a novel stratified testing approach has been proposed for improving the QL of the MCM. However, the effect of reconfigurability on the QL has not been adequately considered and no consideration has been given on the effect of redundancy utilization of the chips and reconfiguration strategies on the QL.

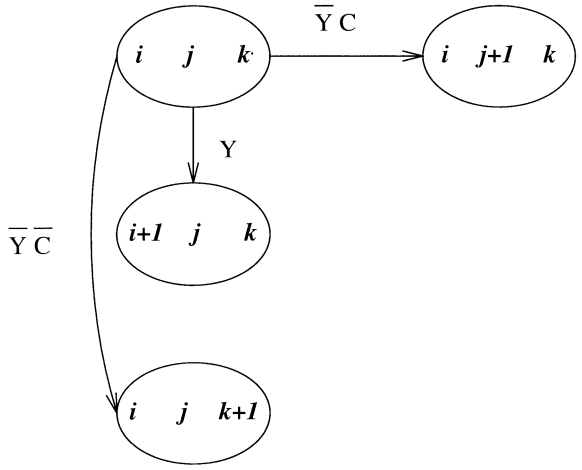

Fig. 2. States and transitions under imperfect fault-coverage.

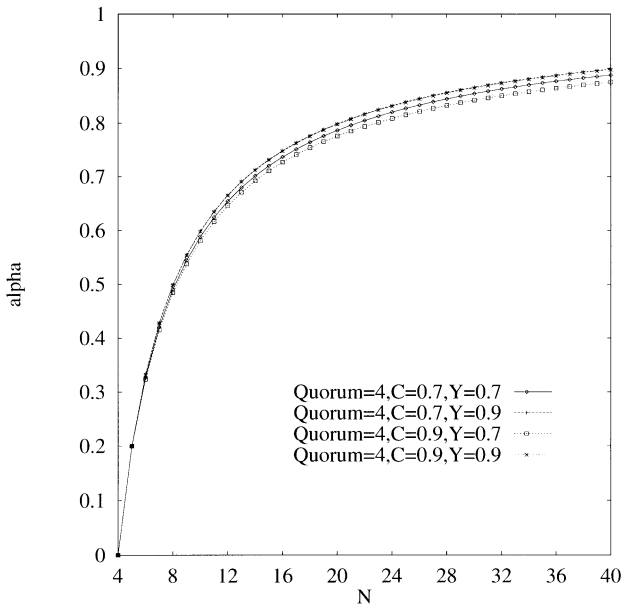

Fig. 3. Values of α at different C and Y.

An example of the RMCM is shown in Fig. 1 and the assumptions in this paper are as follows.

1) The RMCM is composed of multiple (N) identical FPGAs, whose known-good-yields and fault-coverages are even (identical).
2) Full interconnection structure is assumed as a criterion for the maximum overhead in interconnection testing.
3) The yield of each inter-chip interconnection is equal.
4) The testing is performed during the assembly phase [4].
5) Failure independence is assumed for the chips.
6) The selection of the chips for reconfiguration is random.
7) No loss in yield due to the reconfiguration process is assumed.

The notations to be used throughout the paper are given as follows.

- N: the number of chips on RMCM.
- Q: the number of quorum chips.
- (i, j, k): the state in which there are i good chips, j bad chips and k escaped chips ($i + j + k \leq N$) during testing.

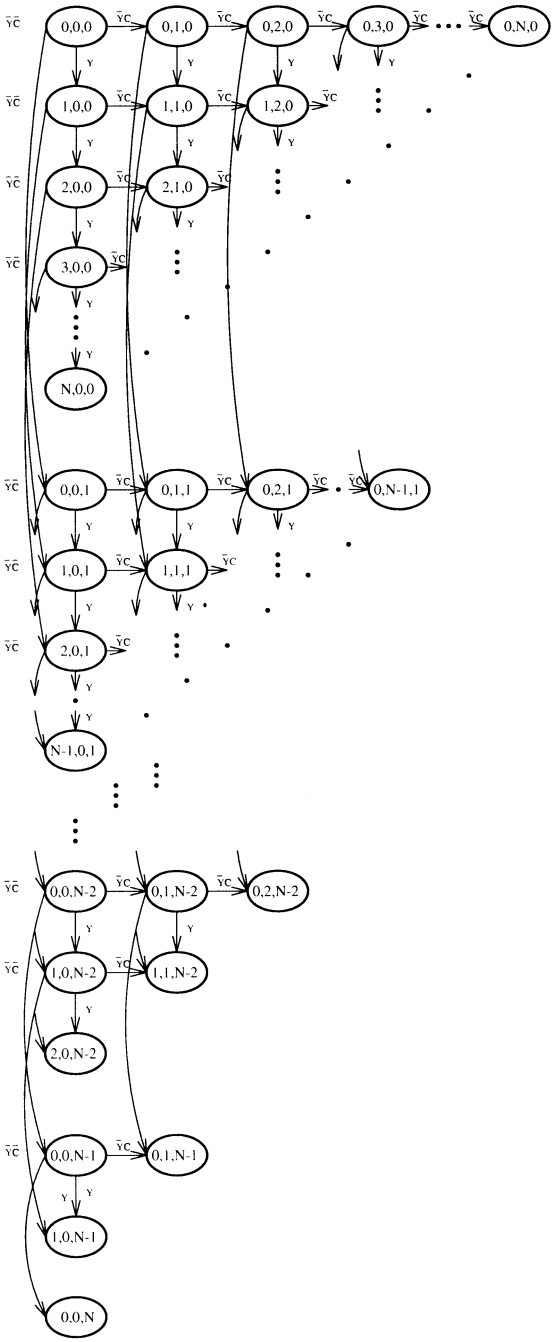

Fig. 4. CQL model.

- (G, B, E): the state in which G good chips, B bad chips and E escaped chips ($G + B + E = N$) after a testing completed and before a reconfiguration applied.
- (g, b, e): the state in which g good chips, b bad chips and e escaped chips ($g \leq G, b \leq B$ and $e \leq E$) after a testing and a reconfiguration completed.
- Y_M: the yield of the RMCM which takes into account both chips and interconnections.
- Y_m: the yield of the RMCM which takes into account only chips without reconfiguration.
- Y_r: the yield of the RMCM which takes into account only chips with reconfiguration.
- Y: the yield of an individual chip.

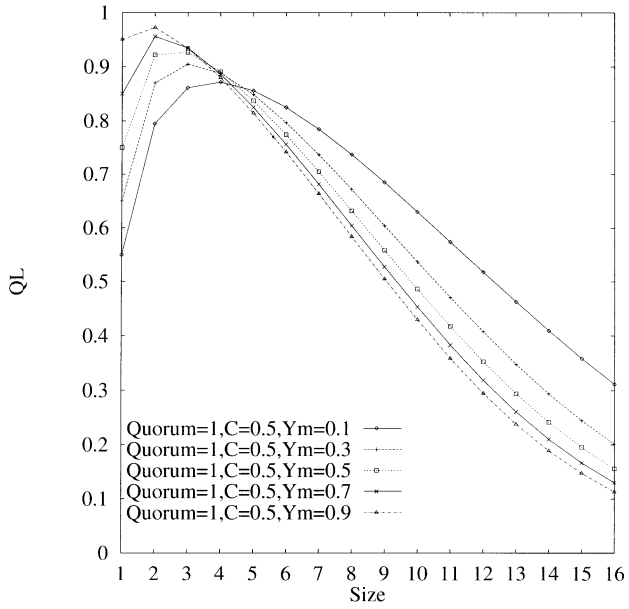

Fig. 5. QL of $Q = 1$ RMCM at $C = 0.5$ and $Y_{int} = 0.9$.

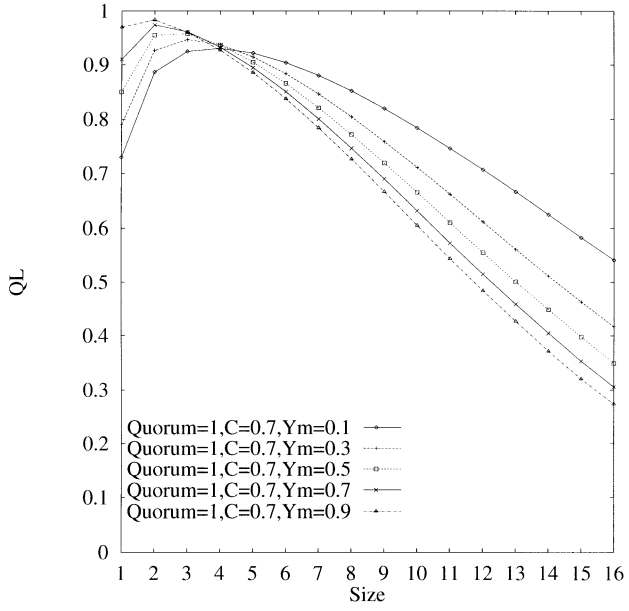

Fig. 6. QL of $Q = 1$ RMCM at $C = 0.7$ and $Y_{int} = 0.9$.

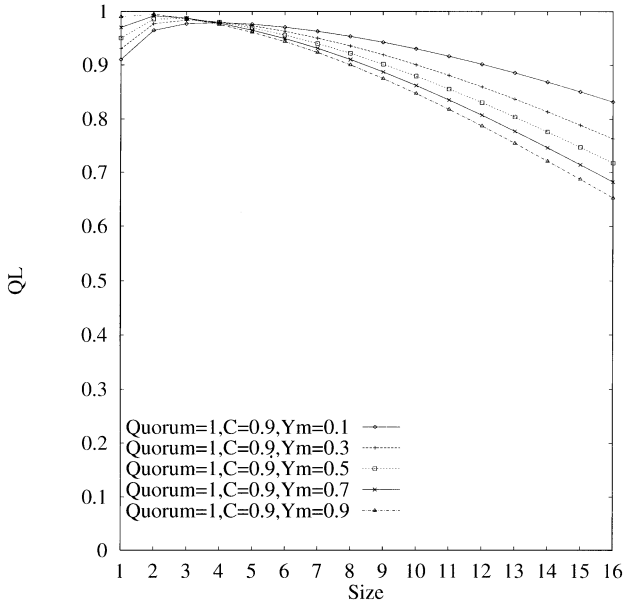

Fig. 7. QL of $Q = 1$ RMCM at $C = 0.9$ and $Y_{int} = 0.9$.

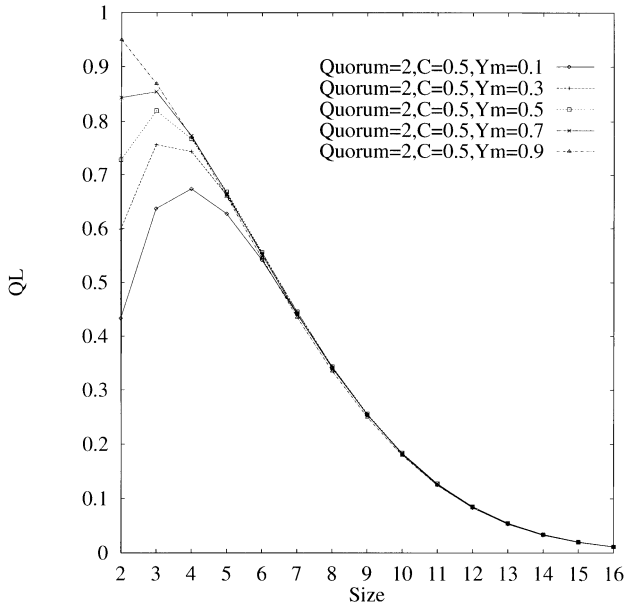

Fig. 8. QL of $Q = 2$ RMCM at $C = 0.5$ and $Y_{int} = 0.9$.

- C: the FC of an individual chip.
- Y_{int}: the overall yield of interconnections.
- y_{int}: the yield of each interconnection between each pair of chips.
- $CQL(N)$: the QL of the RMCM with N chips without reconfiguration.
- $FRP(g, b, e)$ (*Field-Reconfiguration-Probability*): the probability to be reconfigured in the field with g chips out of G good chips, b chips out of B bad chips and e chips out of E escaped chips.
- $FET(G, B, E)$ (*Field-Escape-Tolerability*): the probability for a state (G, B, E) to be escape-free (i.e., no escaped chip) in the field after a reconfiguration.
- $FQL(N, Q)$: the probability for the RMCM (with Q chips of quorum out of N chips) to be escape-free.
- T_c: the FC without reconfiguration.
- T_f: the FC with reconfiguration.
- α: the enhancement rate of FC due to reconfiguration.

III. Redundancy Utilization for Quality Enhancement

Reconfiguration with redundant FPGAs can be employed in conventional reconfigurable systems for the purpose of FT. RMCM systems perform reconfiguration to tolerate faulty FPGAs by utilizing redundant FPGAs, and the effect of FT on the overall yield depends on the amount of redundancy, as well as the reconfiguration strategies. The yield enhancement through FT in reconfigurable gate arrays has been reported in a few works [15], [16] and can be effectively extended to multiple FPGA systems.

However, the QL (i.e., the yield of the system relating to confidence level of testing process or FC) of reconfigurable systems utilizing redundancy has not been reported. During the reconfiguration process, not only can bad chips be tolerated, but escaped chips can also be tolerated. Supposing there are g good, b bad, and e escaped chips after testing the RMCM, ET can be achieved by configuring the system of quorum Q only with good and bad chips, excluding all the escaped chips if $Q \leq g + b$. Hence, assuming random reconfiguration of the system, the probability to configure the system satisfying this condition affects the QL of the system. Note that FT is achieved by configuring the system of quorum Q only with good and escaped chips, excluding all the bad chips if $Q \leq g + e$. Thus, the overall QL can be formulated as a function of the effect of the reconfiguration on FT, FC, and ET, which is dependent on the utilization because the QL is a function of yield (which is related to FT) and FC (which is related to ET) [8].

Traditionally, DL is defined [11] by

$$DL = 1 - Y_m^{1-C} = 1 - QL \tag{1}$$

where Y_m does not assume any reconfiguration process (i.e., $Y_m = Y^N$).

The yield of RMCM with reconfiguration process (i.e., Y_r) can be formulated as follows [7] by using binomial distribution

$$Y_r = \sum_{i=Q}^{N} \binom{N}{i} Y^i (1-Y)^{N-i}. \tag{2}$$

Since (1) does not assume the reconfiguration process, Y_m cannot be readily substituted with Y_r in (2). The QL model proposed in [4] has been shown to be equivalent (in full agreement) to the traditional model and furthermore to relate the QL effectively to various parameters such as uneven FC and imperfect diagnosability by taking into account the stochastic feature of the testing process in MCM systems. However, this model cannot readily relate the QL to the yield enhancement due to FT because failure independence between chips has been assumed and, thus, Y_m in this model is derived by Y^N. To fully evaluate the yield of RMCM, its interconnection yield must be taken into account. Assuming the fully connected structure of FPGAs in the RMCM as the worst case as shown in Fig. 1, the Y_{int} can be formulated by

$$Y_{int} = \sum_{i=1}^{N} y_{int}^{i(i-1)/2}. \tag{3}$$

Hence, Y_M of RMCM to take into account both chips and interconnection can be derived by

$$Y_M = Y_r \times Y_{int}. \tag{4}$$

IV. Analysis

As the testing and mounting process of each chip can be characterized stochastically as shown in [3], [4], then it is possible to define a state of the system in which there are i tested-mounted-as-good chips (believed to be fault free), j tested-mounted-as-bad chips, and k tested-mounted-as-escaped chips (passed the test process as good, while indeed bad) by vertex (i, j, k). At each state of this Markov model, there is only one untested chip for $N > i + j + k$, where N is the number of chips to be mounted on the substrate of the MCM. The quality level of MCMs is affected by the probability of the states in which $i + j + k = N$ and $k > 0$. The value of k is obviously a function of the fault-coverage and the diagnosability.

State transitions take place every time a chip is tested to be mounted. It is assumed that chips are selected for testing and mounted in an arbitrary order and the tests are independent (as in random testing). The state transition rates for every state under imperfect fault-coverage and perfect-diagnosis are shown in Fig. 2. Fig. 4 shows the state transition diagram of RMCM under imperfect fault-coverage and perfect diagnosis prior to reconfiguration, which is referred to as $CQL(N)$ where N is

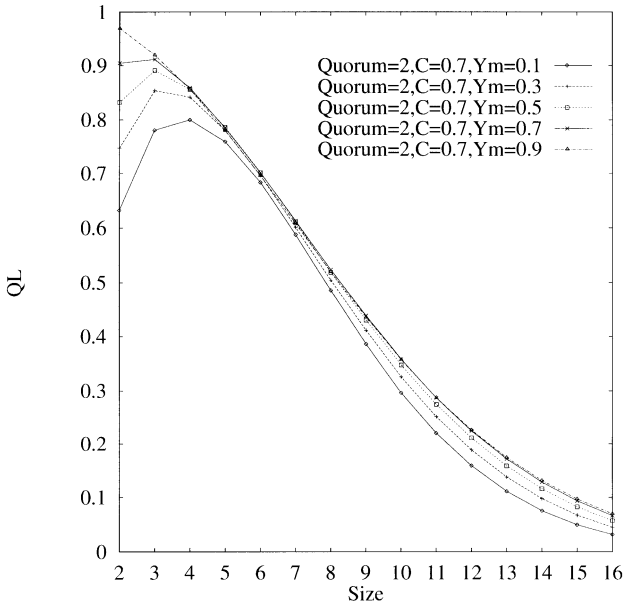

Fig. 9. QL of $Q = 2$ RMCM at $C = 0.7$ and $Y_{int} = 0.9$.

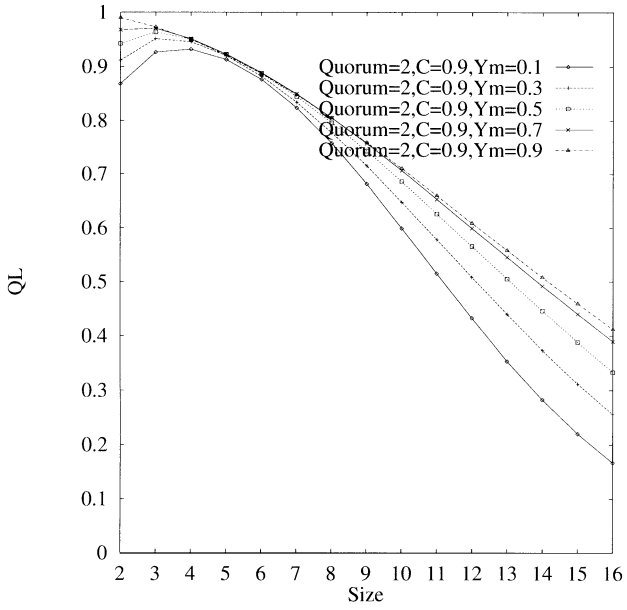

Fig. 10. QL of $Q = 2$ RMCM at $C = 0.9$ and $Y_{int} = 0.9$.

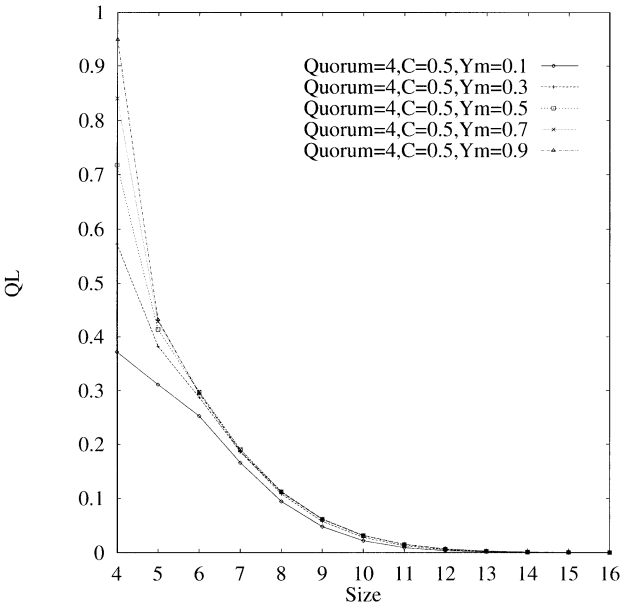

Fig. 11. QL of $Q = 4$ RMCM at $C = 0.5$ and $Y_{int} = 0.9$.

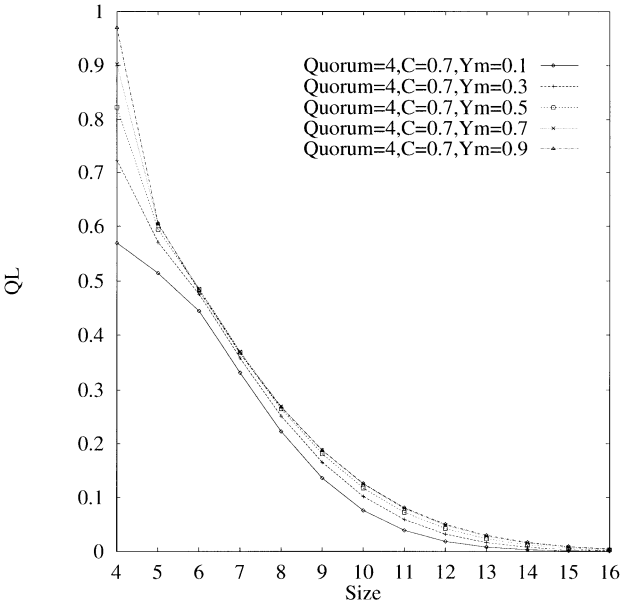

Fig. 12. QL of $Q = 4$ RMCM at $C = 0.7$ and $Y_{int} = 0.9$.

the total number of FPGAs on the RMCM. From each state (i, j, k), $(N > i + j + k)$, three cases can occur [note that as no intermediate test and rework processes are assumed, there is no transition to $(i-1, j+1, k)$, $(i+1, j-1, k)$, $(i+1, j, k-1)$, $(i, j+1, k-1)$].

1) A just-mounted chip is tested, mounted, and diagnosed as good, thus driving the system into state $(i + 1, j, k)$ with probability Y.
2) A just-mounted chip is tested and diagnosed as bad, thus driving the system into state $(i, j + 1, k)$ with probability $\overline{Y}C$. The implication of this transition probability is that a chip is correctly tested as bad only if the testing process detects all faults with a fault-coverage given by C.
3) A faulty chip is tested, mounted, and diagnosed as good, thus driving the system into state $(i, j, k + 1)$ with probability $\overline{Y}\ \overline{C}$. This implies that a chip can be faulty with probability $\overline{Y}$ and the testing process fails in detecting all faults with probability $\overline{C}$.

All the state probabilities $P(i, j, k)$ for every state (i, j, k) can be calculated from (6)–(13) in Appendix A; thus, the overall $CQL(N)$ of the RMCM can be derived as a function of the known-good-yield (Y) and the FC as

$$CQL(N) = \sum_{i+j=N} P(i, j, 0) - P(0, N, 0) \tag{5}$$

where the term $\sum_{i+j=N} P(i, j, 0) - P(0, N, 0)$ corresponds to the sum of the probabilities of the states in which there is no chip in an escape state after all the N chips have been tested and mounted [note that $P(0, N, 0)$ is the probability of a state in which all the N chips have been tested and mounted as bad, i.e., no good and escaped chips].

At each state (G, B, E) in Fig. 4, where $G + B + E = N$, N = *total number of FPGAs on the system*, the FPGAs are supposed to undergo reconfiguration with a given Q (note that $Q = g + b + e$). $FRP(g, b, e)$ is as follows.

$$FRP(g, b, e) = \frac{\binom{G}{g}\binom{B}{b}\binom{E}{e}}{\binom{N}{Q}}. \tag{6}$$

Then, $FET(G, B, E)$ can be derived as follows:

$$FET(G, B, E) = \sum_{e=0} FRP(g, b, e),$$
$$0 \le g \le G,\ 0 \le b \le B, g + b = Q. \tag{7}$$

Hence, $FQL(N, Q)$ can be derived as follows.

$$FQL(N, Q) = \sum FET(G, B, E),$$
$$0 \le G \le N, 0 \le B \le N,$$
$$0 \le E \le N, \text{ and } G + B + E = N. \tag{8}$$

However, as mentioned in the previous section, $FQL(N, Q)$ cannot readily relate the yield enhancement due to FT and the effect of reconfiguration on the FC; thus, the following steps are proposed.

The $CQL(N)$ follows the conventional QL model [8] as follows.

$$CQL(N) = Y_m^{1-T_c}. \tag{9}$$

which holds because neither $CQL(N)$ nor T_c is related to the reconfiguration process.

Thus

$$T_c = 1 - \log_{Y_m} CQL(N). \tag{10}$$

The effect of reconfiguration on FC considered in this paper shows that more faults can be covered in reconfigurable systems than in the compatible nonreconfigurable systems equipped with the same logic and interconnection components.

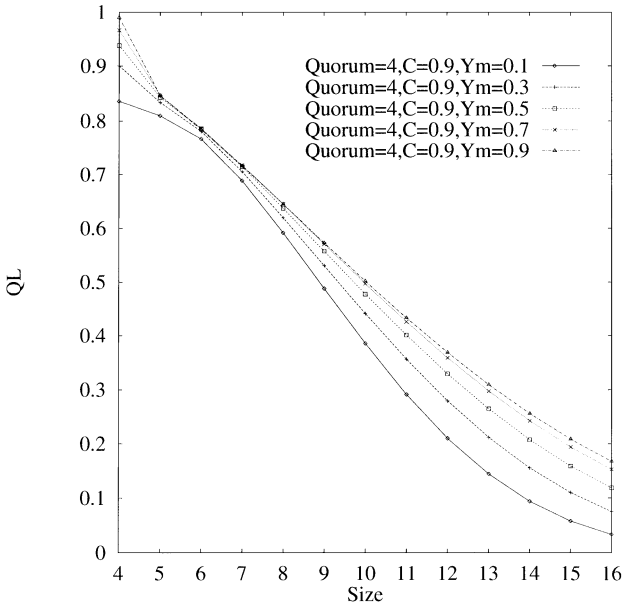

Fig. 13. QL of $Q = 4$ RMCM at $C = 0.9$ and $Y_{int} = 0.9$.

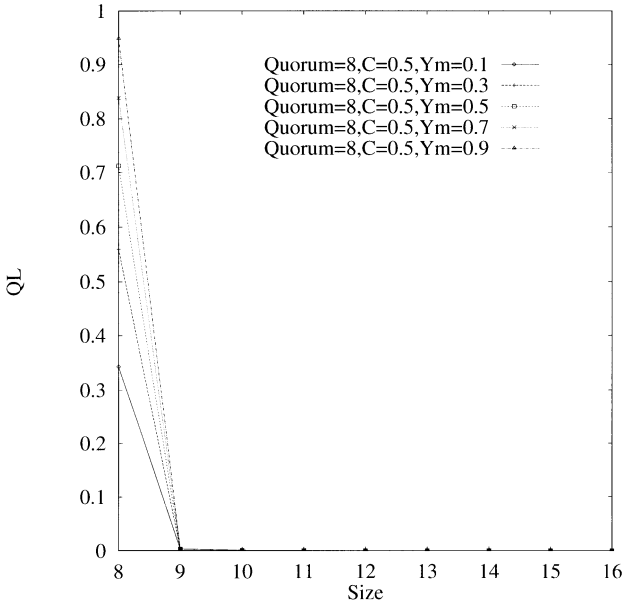

Fig. 14. QL of $Q = 8$ RMCM at $C = 0.5$ and $Y_{int} = 0.9$.

This observation is shown through theoretical analysis in the following.

By employing the reconfiguration process in the RMCM, the overall FC (T_f) can be formulated as

$$T_f = T_c + (1 - T_c)\alpha. \tag{11}$$

Now, the $FQL(N, Q)$ can be related to Y_m and T_f by the following convention as

$$FQL(N, Q) = Y_m^{1-T_f} \tag{12}$$

which holds because $FQL(N, Q)$ is not related to yield enhancement by FT (i.e., not related to Y_r). Thus, the enhanced FC for the raw yield (i.e., Y_m) can be obtained from (12) and the value of α can be derived as follows by substituting T_f with $T_c + (1 - T_c)\alpha$ and T_c with $1 - \log_{Y_m} CQL(N)$.

$$\alpha = 1 - \frac{\log FQL(N, Q)}{\log CQL(N)}. \tag{13}$$

It is shown in Fig. 3 that, by using (13), α increases as the amount of redundancy increases; thus, the reconfiguration process improves the coverage of testing (i.e., FC). Note that the increase of α as more redundancy is employed is a theoretical observation of the enhancement of fault coverage associated with the increase of the redundancy and reconfiguration process.

Now, by following the conventional QL model [8], the resultant QL incorporating the effect of the yield enhancement due to FT and the FC enhancement due to reconfiguration can be derived as follows.

$$QL = Y_M^{1-T_f} \tag{14}$$

which holds because every term in the equation is related to reconfiguration features. In Appendix B, the analysis of the proposed approach is summarized.

Therefore, the proposed QL model can effectively take into account the overall yield enhancement due to FT, the effect of reconfiguration on the overall FC;, and the effect of ET on the overall QL.

V. Parametric Analysis

The effect of redundancy utilization on the QL in RMCM systems will be studied through numerical experiments in this section. Five kinds of theoretical RMCM systems with $Q = 1$, $Q = 2$, $Q = 4$, $Q = 8$, and $Q = 16$, as shown in Table I, will be investigated with $N = 16$ and $y_{int} = 0.9$ for each configuration. For the configuration 1, redundancy is given by 0 to 15 FPGA and 0 to 14, 0 to 12, and 0 to 8 for each configuration 2, 3, and 4, respectively; thus $N = 1$ to 16, 2 to 16, 4 to 16, and 8 to 16, respectively. The QL of the configuration with $Q = 16$ is shown in Fig. 17 for the purpose of comparison.

The effect of redundancy utilization on QL will be shown under various sets of fault-coverage (C) on each FPGA, known-good-yield (Y_m) of the quorum of RMCM (i.e., $C = 0.1$ and 0.5 to 0.9 increased by 0.2 and $Y_m = 0.1$ and 0.5 to 0.9 increased by 0.2) and size N (note that redundancy is $N - Q$) for a given value of Q.

The known-good-yield of each FPGA is calculated by ${Y_m}^{1/Q}$ and then the addition of $N - Q$ ($N > Q$) FPGAs will reduce the overall known-good-yield (i.e., Y_m) of the RMCM by $(Y_Q - Y_N)/Y_Q$ (where Y_Q is Y_m and Y_N is $Y^{N/Q}$).

The values of QL for the given values of C are drawn in Figs. 5–16. For $Q = 1$, RMCMs with given C, the QL at different Y_m are plotted in Figs. 5–7. Also, in Figs. 8–10, 11–13, and 14–16, the QLs at different Y_m are plotted for $Q = 2$, $Q = 4$, and $Q = 8$ RMCM, respectively.

By comparing the results in Figs. 5–7, the following can be observed.

- The QL increases as the value of C increases at a given value of Y_m.

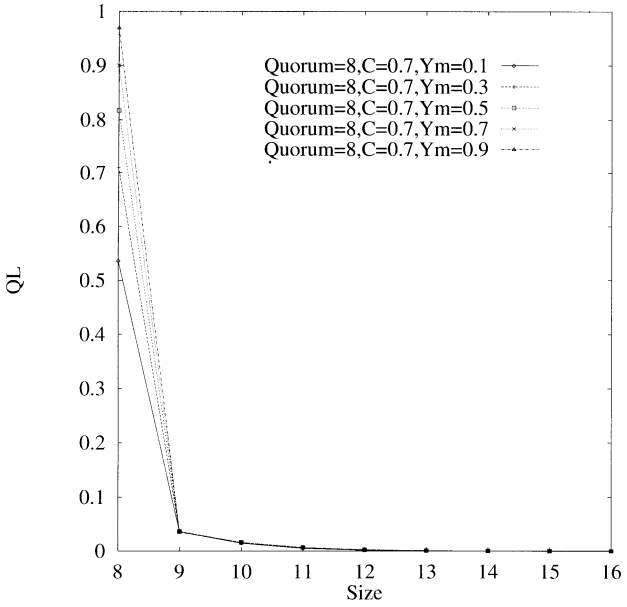

Fig. 15. QL of $Q = 8$ RMCM at $C = 0.7$ and $Y_{int} = 0.9$.

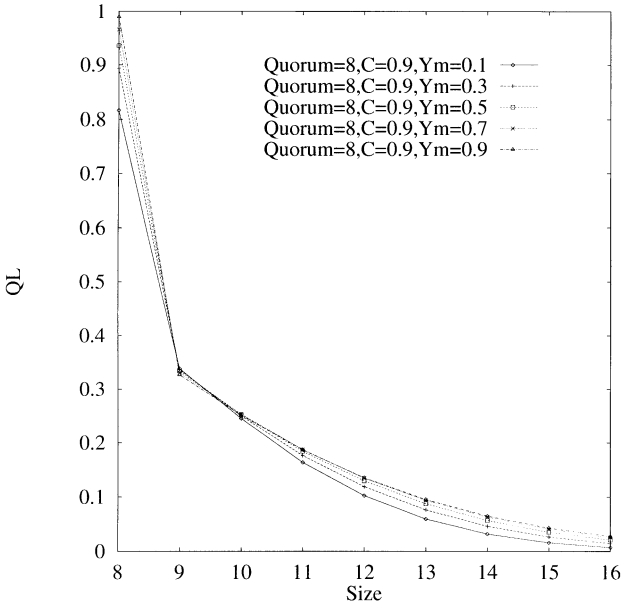

Fig. 16. QL of $Q = 8$ RMCM at $C = 0.9$ and $Y_{int} = 0.9$.

- The QL increases up to a certain value of N but decreases after this value as Y_m increases with a given value of C. This value is formed at the smaller value of N as C increases.
- The increase in the QL is bounded at a certain value of N with given values of C and Y_m. This value is formed at the larger value of N as Y_m decreases.

Also, by comparing the results in Figs. 5–7 and 8–16, the following can be observed.

- Given the value of N, the QL decreases as the value of Q increases.
- The value of N at which the increase of the QL is bounded is smaller as the value of Q increases and the further the QL decreases as the value of N increases beyond a certain value of Y_m and Q.

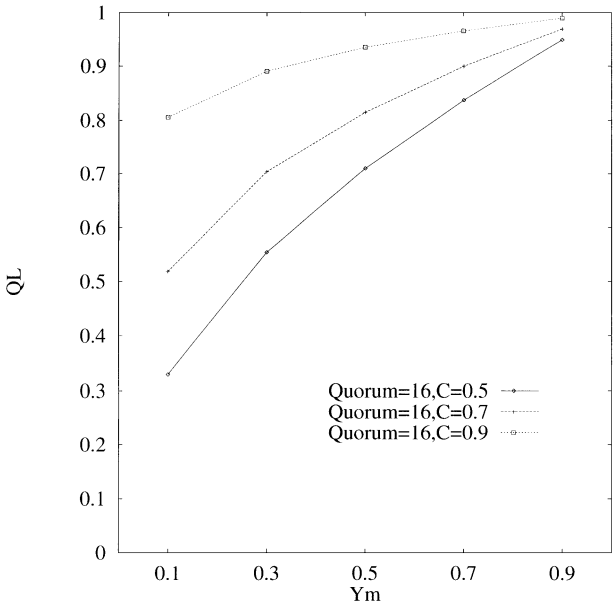

Fig. 17. QL of $Q = 16$ RMCM at $C = 0.5, 0.7, 0.9$ and $Y_{int} = 0.9$.

TABLE I
RMCM CONFIGURATIONS UNDER INVESTIGATION IN THIS PAPER

RMCM	N	Q
Configuration 1	16	1
Configuration 2	16	2
Configuration 3	16	4
Configuration 4	16	8
Configuration 5	16	16

Hence, from the above observations, the following conclusions can be drawn.

1) Given the values of Y_m, N, and Q, redundancy utilization enhances the QL better at high values of C.
2) Up to a certain amount of redundancy (or a certain value of N with a given Q), redundancy utilization enhances the QL better for high-yield systems than for low-yield systems, but beyond that redundancy level, the redundancy utilization is more in favor of the low-yield systems in terms of QL.
3) Low-yield systems can use more redundancy to enhance the QL than high-yield systems with a given value of C.

VI. DISCUSSION AND CONCLUSION

This paper has presented an evaluation technique for the quality-effectiveness of redundancy utilization of RMCM systems. Unlike the previous methods [1], [3], [4], [7], and [8], we have derived a QL by relating the QL to the yield enhancement by reconfiguration, the effect of ET, and the improvement in FC by reconfiguration. In the proposed approach, combinatorial models are proposed to take into account the parameters related to the redundancy and reconfiguration processes in RMCM systems based on the quality model proposed in [4].

From the extensive parametric results, it is shown that given the values of Y_m, N, and Q, redundancy utilization enhances the QL better. Up to a certain amount of redundancy (or a certain value of N with a given Q), redundancy utilization enhances the QL more effectively for high-yield systems than for low-

yield systems; beyond that redundancy level, low-yield systems can utilize more redundancy to enhance the QL than high-yield systems with any given value of C.

Therefore, by using the proposed approach, a quality-effective redundancy utilization of RMCM systems can be realized, and effective testing strategies and design-for-quality for RMCM systems can be ultimately achieved.

APPENDIX A

After the $(i+j+k)$'th chip is tested (and mounted) with an imperfect fault-coverage, the difference equations for the state diagram of Fig. 4 are as follows:

$$P(i,0,0) = P(i-1,0,0)Y, \text{ for } j=0, k=0 \text{ and } i \geq 1 \quad (15)$$

$$P(0,j,0) = P(i,j-1,0)\overline{Y}C, \text{ for } i=0, k=0 \text{ and } j \geq 1 \quad (16)$$

$$P(i,j,0) = P(i-1,j,0)Y + P(i-1,j,0)\overline{Y}C, \text{ for } k=0 \text{ and } i,j \geq 1 \quad (17)$$

$$P(0,0,k) = P(i,j,k-1)\overline{YC}, \text{ for } i=0, j=0 \text{ and } 0 < k < N \quad (18)$$

$$P(i,0,k) = P(i-1,0,k)Y + P(i,0,k-1)\overline{YC}, \text{ for } j=0, 0 < k < N \text{ and } i \geq 1 \quad (19)$$

$$P(0,j,k) = P(0,j-1,k)\overline{Y}C + P(0,j,k-1)\overline{YC}, \text{ for } i=0, 0 < k < N \text{ and } j \geq 1 \quad (20)$$

$$P(i,j,k) = P(i-1,j,k)Y + P(i,j-1,k)\overline{Y}C + P(i,j,k-1)\overline{YC}, \text{ for } 0 < k < N \text{ and } i,j \geq 1 \quad (21)$$

$$P(0,0,N) = P(0,0,k-1)\overline{YC}, \text{ for } i=0, j=0 \text{ and } k=N \quad (22)$$

where $P(i,j,k)$ represents the state probability of having i, j, and k chips tested (and mounted) as good, bad, and escaped, respectively. Y and C represent the known good yield and the fault-coverage, respectively.

APPENDIX B

The following is the summary of the analysis steps of the proposed approach (refer to the notations provided in Section II).

1) Calculate Y_M.
2) Derive the probability of each state (G,B,E) using Appendix A in Fig. 4, where $G+B+E=N$.
3) Calculate each $FRP(g,b,e)$ by using (6).
4) Calculate $FET(G,B,E)$ by using (7).
5) Calculate α from the value of $FQL(Q,N)$ and by using (10)–(12).
6) Calculate T_f by using the value of α from step 5).
7) Derive the value of QL by using the values of Y_M from step 1) and T_f from step 6) as (14).
8) End of analysis.

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