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FDTD Modeling Incorporating a Two-Port Network for I/O Line EMI Filtering Design

Xiaoning Ye, *Member, IEEE*, and James L. Drewniak, *Senior Member, IEEE*

***Abstract*—Electromagnetic interference (EMI) filters are often utilized on I/O lines to reduce high-frequency noise from being conducted off the printed circuit board (PCB) and causing EMI problems. The filtering performance is often compromised at high frequencies due to parasitics associated with the filter itself, or the PCB layout and interconnects. Finite difference time domain (FDTD) modeling can be used to quantify the effect of PCB layout and interconnects, as well as filter type, on the EMI performance of I/O line filtering. FDTD modeling of a T-type and π-type filter consisting of surface-mount ferrites and capacitors is considered herein. The FDTD method is applied to model PCB layout and interconnect features, as well as the lumped element components, including the nonlinear characteristics of ferrite surface-mount parts. The EMI filters with ferrites are included in the modeling by incorporating the time-domain Y-parameters of the two-port network into the FDTD time-marching equations. Good agreement between the FDTD modeling and S-parameter measurements supports the new FDTD algorithm for incorporating two-port networks.**

***Index Terms*—Finite difference time domain (FDTD) method, generalized pencil-of-function (GPOF), I/O filter, two-port network.**

I. Introduction

ELECTRONIC devices are operating at increasingly faster speeds and consuming more power, which significantly increases electromagnetic interference (EMI) concerns at high frequencies, and makes it more challenging to meet radiated emissions requirements. One important radiation mechanism is high-frequency noise on I/O lines that is conducted onto the attached cables, and results in EMI problems [1]. Many lines that come off a high-speed digital design to peripherals are nominally low-speed. However, as the clock speeds and edge rates of device technologies continue to increase, increasingly higher frequency noise is unintentionally coupled to the low-speed I/O lines [2]. EMI filters are often inserted on the I/O lines to suppress the high-frequency noise.

The relevant design features that affect the EMI performance of I/O line filtering found on a typical electronic product are illustrated in Fig. 1. Shunt capacitors are often used to "divert" the high-frequency noise back to its source. However, due to the inherent equivalent series inductance (ESL) and equivalent series resistance (ESR) of the surface-mount technology (SMT) capacitor, the EMI filtering performance is compromised at frequencies higher than the series resonance of the capacitance and the ESL. Furthermore, when the EMI filter is mounted on the printed circuit board (PCB) in practical design, layout parasitics, such as connecting traces and vias, introduce additional inductance in the shunt filtering branch. The filtering performance is further compromised, and far from ideal. The open literature on the design and application of EMI filters is extensive [3]–[6]. Other EMI coupling paths that result in high-frequency common-mode current on low-speed cables can be characterized by a noise voltage between a shielding enclosure and the I/O line, as shown Fig. 1. The connection between the PCB reference plane and the conducting shielding enclosure or chassis at the connector can also profoundly impact the EMI performance of any filtering at the connector. The PCB/chassis connection has some nonzero impedance that is schematically represented with an inductor symbol in Fig. 1.

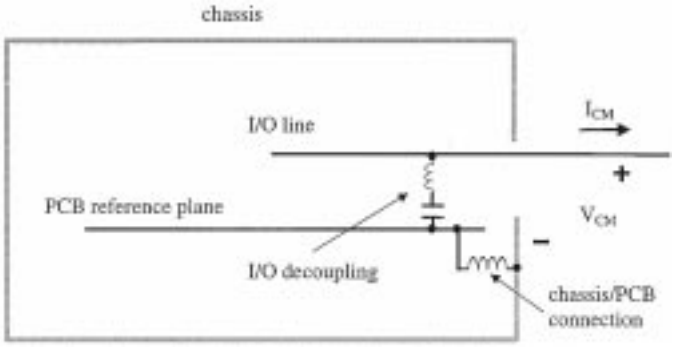

Fig. 1. Schematic representation showing the I/O filtering and chasis/PCB connection parasitics.

Numerical modeling in electromagnetic compatibility (EMC) design is beneficial for better understanding of the physics, and can aid in developing design guidelines. For the geometry shown in Fig. 1, full-wave modeling can be applied. The finite difference time domain (FDTD) method is a good candidate because it is capable of analyzing multiple frequencies with a single time-domain simulation, and it is well suited for rectilinear geometries. The method has been successfully applied in modeling shielding enclosures [7], and FDTD modeling of lossy, multiconductor transmission lines terminated in arbitrary loads has also been reported [8]. However, incorporating EMI filters into the FDTD modeling is challenging because the ESL, ESR, and other parasitics of the filter are strongly dependent on package size, PCB layout, and interconnection of the components. Characterization of the parasitics usually relies on measurements.

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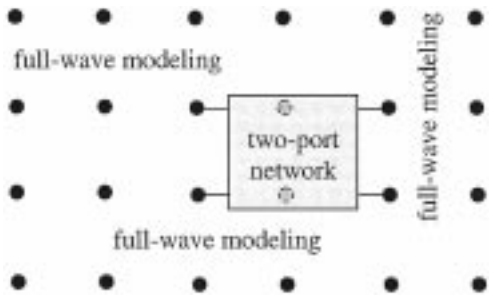

Fig. 2. Schematic representation of the FDTD grid with an embedded two-port network. Each black dot represents an FDTD node.

In this study, an algorithm for including passive networks characterized as two-ports into the FDTD method is presented in Section II. The time-domain Y-parameters of a two-port network are obtained from the inverse Fourier transform (IFT) of the frequency-domain measurements, and integrated into the FDTD updating equation through a time-domain convolution. The method can readily include the nonlinear behavior of lumped ferrite into the two-port network. In Section III, the approach is shown with T- and π-filters, and demonstrated with measurements. In Section IV, the utility of the FDTD modeling is further demonstrated by modeling the board layout effects on the filtering performance, and the modeling is supported by $|S_{21}|$ measurements.

II. FDTD Modeling of I/O Lines With an EMI Filter Using a Two-Port Algorithm

The parasitics that compromise the performance of an EMI filter are strongly dependent on package size, PCB layout, and interconnection of the components, as stated previously. These parasitics are usually obtained from measurable parameters such as impedance and resonance frequencies. There are different approaches to incorporate a filter with parasitics into the FDTD modeling. A straightforward approach to account for the parasitics is to extract an equivalent circuit model from measurements, and then include the equivalent lumped elements in the modeling using the algorithms developed in [9] and [10]. This approach is most suitable when an *RLC* model of the filter with frequency-independent element values is available. In practical design, SMT ferrite beads are often inserted at I/O lines because ferrite beads have a small impedance at low frequencies but a large impedance at high frequencies. The low-frequency signals are then passed, while high-frequency noise is blocked. Although an equivalent circuit model was proposed in [11], which characterized the ferrite using a frequency-dependent *RLC* circuit, these *RLC* values cannot be incorporated into the FDTD modeling using the algorithms in [9] and [10]. Recent work on modeling the lumped ferrite converted the impedance of the ferrite into the time-domain, and incorporated this into the FDTD updating equations [12]. A modeling approach which incorporates a two-port network into the FDTD modeling was proposed in [13], where the time-domain Y-parameters of a two-port network were obtained from the IFT of the frequency-domain measurements (e.g., S-parameters), and integrated into the FDTD updating equation through a time-domain convolution. There have been other approaches to include two-port networks to FDTD [14], [15]. In the study, the two-port algorithm described in [13] is applied.

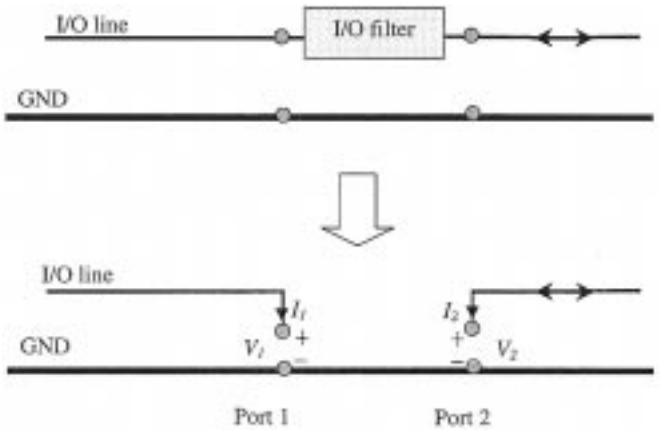

Fig. 3. I/O filter modeling with an FDTD two-port subcellular algorithm.

The traditional FDTD algorithm discretizes the computational domain into rectangular cells and uses a leapfrog time-stepping process to update the electric-field and magnetic-field components at each node [16]–[18]. A two-dimensional representation of the FDTD grid with an embedded two-port network is shown in Fig. 2. The network may span a few cells to account for the physical distance between the two ports. Special treatment is required for updating the fields at the nodes where the network ports are connected, while the normal full-wave modeling, *viz*., the Yee-algorithm is applied elsewhere, including the FDTD nodes between the ports. The two-port network is incorporated in the FDTD modeling, as shown in Fig. 3, for I/O filtering. The electric field time-stepping equation at network ports is modified by adding an impressed current to account for the currents directed into the ports [10], and the Ampere's Law Maxwell equation becomes

$$\nabla \times \vec{H} = \sigma \vec{E} + \frac{\partial \vec{D}}{\partial t} + \vec{J}_{\text{net}} \tag{1}$$

where $\vec{J}_{\text{net}}$ is the impressed current density into the network. Let the network be oriented along the z direction of the FDTD mesh. Then, the current density is related to the node current as

$$J_{\text{net}} = \frac{I_{\text{net}}}{\Delta x \cdot \Delta y}. \tag{2}$$

The current is related to the voltage in the frequency-domain by Y-parameters as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{3}$$

Then, in the time-domain, the current density at Port 1 is

$$\begin{aligned} J_{\text{net1}} &= \frac{I_{\text{net1}}}{\Delta x \cdot \Delta y} = \frac{V_{\text{net1}} * Y_{11}(t) + V_{\text{net2}} * Y_{12}(t)}{\Delta x \cdot \Delta y} \\ &= \Delta z \cdot \frac{E_{\text{net1}} * Y_{11}(t) + E_{\text{net2}} * Y_{12}(t)}{\Delta x \cdot \Delta y} \end{aligned} \tag{4}$$

where the $*$ symbol indicates convolution.

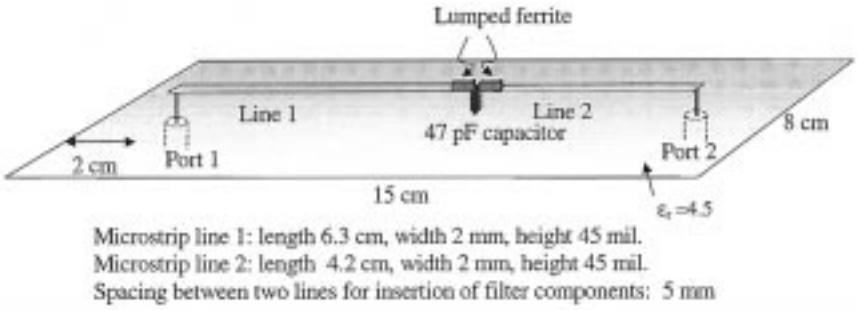

Fig. 4. Schematic of a PCB with a T-type EMI filter—Board A.

The time-stepping equation can then be readily developed from (1) and (4). The two-port network can be characterized by S-, Y-, or Z-parameters; however, the Y-parameters are used in the FDTD algorithm, and other parameter sets can be readily converted to the Y-parameters. An IFFT is performed to translate the frequency-domain Y-parameters into the time-domain. The frequency-domain Y-parameter sequence is further extended to $2 \times N$ by conjugating the first N values before application of the IFFT in order to get a real sequence in the time-domain. The presence of the convolution in (4) requires storing the complete E-field and Y-parameter time histories, which increases memory usage. The generalized pencil-of-function (GPOF) technique is employed here, which uses a finite sum of complex exponentials to describe the time response sequences of the Y-parameters [$Y_{11}(n)$, $Y_{12}(n)$, $Y_{21}(n)$, and $Y_{22}(n)$], as [19]

$$Y_{ij}(n) = \sum_{k=1}^{m} \alpha_{ij}(k)[\beta_{ij}(k)]^n \tag{5}$$

where $\alpha_{ij}(k)$ and $\beta_{ij}(k)$ are the terms obtained by the GPOF method, and generally are complex numbers. For simplicity in the present development, the network is assumed to be located in free space, and the time-marching equation for the z-component of the electric field at Port i ($i = 1$ or 2) is shown in (6) at the bottom of the page. Substituting (5) into (6) results in a recursive convolution for the time-marching equation, where

$$\sum_{l=0}^{n} Y_{ij}(l) \cdot E_{z,\,\mathrm{Port}\,j}(n-l) = \sum_{k=1}^{m} \alpha_{ij}(k) \cdot E_{z,\,\mathrm{Port}\,j}(n) + \sum_{k=1}^{m} \Phi_{ij}(n,\,k) \tag{7}$$

and

$$\Phi_{ij}(n,\,k) = \alpha_{ij}(k) \cdot \beta_{ij}(k) \cdot E_{z,\,\mathrm{Port}\,j}(n-1) + \beta_{ij}(k) \cdot \Phi_{ij}(n-1,\,k). \tag{8}$$

Application of the GPOF algorithm to generate the Y-parameters as an exponential series allows for recursive convolution in the FDTD updating equations, where only the intermediate parameters $\Phi_{ij}(n,\,k)$ are stored for the current time step. These intermediate parameters are then overwritten at each following time step, without the need of storing the complete time history for the convolution. This treatment significantly minimizes the computer memory usage. The constants $\alpha_{ij}(k)$ and $\beta_{ij}(k)$, which characterize the two-port network, are used as the input circuit description of the network for the FDTD simulation.

III. Experimental and Numerical Results

A simple microstrip circuit shown in Fig. 4, denoted as Board A, was studied to demonstrate the FDTD procedure. Two sections of microstrip lines were connected by a low-pass T-type filter, which was constructed using two SMT lumped-element ferrites and one SMT capacitor. The PCB dimensions were 8×15 cm^2, and the dielectric was a 45-mil thick FR-4 material. The width of the microstrip was 2 mm, and the length of each section of microstrip line was 6.3 cm and 4.2 cm for Line 1 and Line 2, respectively. The characteristic impedance of the microstrip line was 52 Ω, which was calculated using empirical equations [20]. The 0805 SMT capacitor had a capacitance of 47 pF, which was verified by measurement using an HP 4291 impedance analyzer. One end of the capacitor was soldered to the ground plane directly by cutting a hole in the dielectric substrate, and "burying" the capacitor vertically into the dielectric substrate. The other end of the capacitor was soldered to the end of both SMT ferrites. The layout parasitics were then minimized. SMA jacks were located at Port 1 and Port 2 to provide connection for S-parameter measurements.

A. Experimental Results

The $|S_{21}|$ was then measured using an HP 8753D Network Analyzer. The solid line in Fig. 5 shows the measured $|S_{21}|$ for Board A. Although the layout parasitics were minimized, the effectiveness of the shunt capacitor was limited by the parasitic inductance of the current path through the component itself. The equivalent circuit for the filtering capacitor is an inductor in series with an ideal capacitor, and an ESR. Beyond the series resonance of the equivalent circuit (approximately 940 MHz in this

$$E_{z,\,\mathrm{Port\,i}}^{n+1} = E_{z,\,\mathrm{Port\,i}}^{n} + \frac{\Delta t}{\varepsilon_0}[\nabla \times H^{n+1/2}]_z - \frac{\Delta t \cdot \Delta z \cdot \left[\sum_{l=0}^{n} Y_{i1}(l) \cdot E_{z,\,\mathrm{Port\,1}}(n-l) + \sum_{l=0}^{n} Y_{i2}(l) \cdot E_{z,\,\mathrm{Port\,2}}(n-l)\right]}{\varepsilon_0 \cdot \Delta x \cdot \Delta y} \tag{6}$$

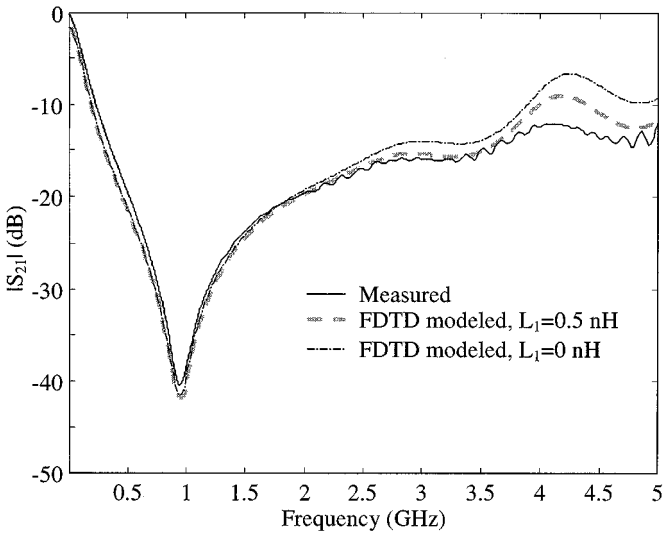

Fig. 5. Measured and FDTD modeled $|S_{21}|$ for Board A.

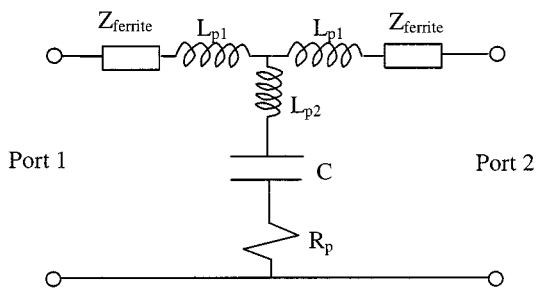

Fig. 6. Simple equivalent circuit model of the local lumped element T-network with $L_{p2} = 0.58$ nH, $C = 47$ pF, and $R_p = 0.4\ \Omega$.

example), the shunt capacitor branch begins to look inductive; consequently, the impedance between the microstrip line and the reference plane increases with frequency, resulting in an increase in $|S_{21}|$.

B. Numerical Results

The FDTD method was applied to model Board A. In order to use the two-port FDTD algorithm, which incorporates the time-domain Y-parameters of the two-port lumped-element network into the FDTD algorithm, the two-port lumped element network needed to be characterized. A simple equivalent circuit of the network is shown in Fig. 6. The parasitics are included in the circuit, where R_p is the ESR of the capacitor, L_{p2} is the ESL of the capacitor, and L_{p1} is the parasitic inductance associated with the discontinuity in the transmission line at the SMT ferrite part. Although the ESL and ESR of the capacitor can be measured using the impedance analyzer, the actual parasitics of a component mounted on the PCB board may differ from the measurement of an individual component. An alternative approach was employed herein to determine the parasitics. The two ferrites shown in Fig. 4 were removed, and the transmission line made continuous with two short sections of copper tape with the same width of 2 mm. Therefore, the I/O line was continuous and the filter consisted of only a shunt capacitor. The $|S_{21}|$ was then measured using an HP 8753D Network Analyzer.

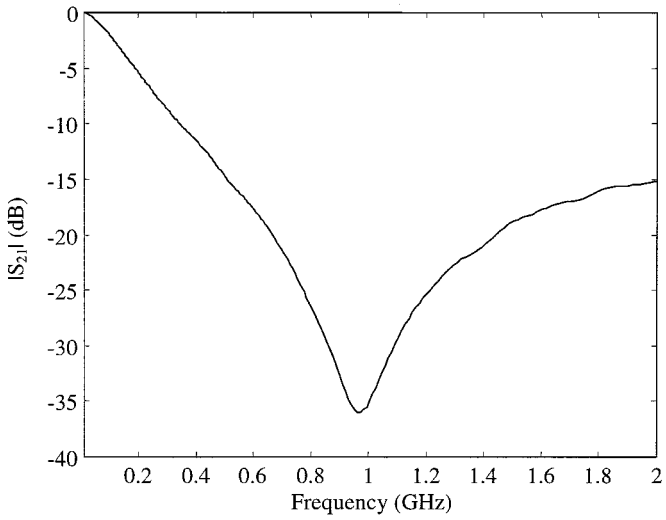

Fig. 7. Measured $|S_{21}|$ for the Board A without ferrites for the filter.

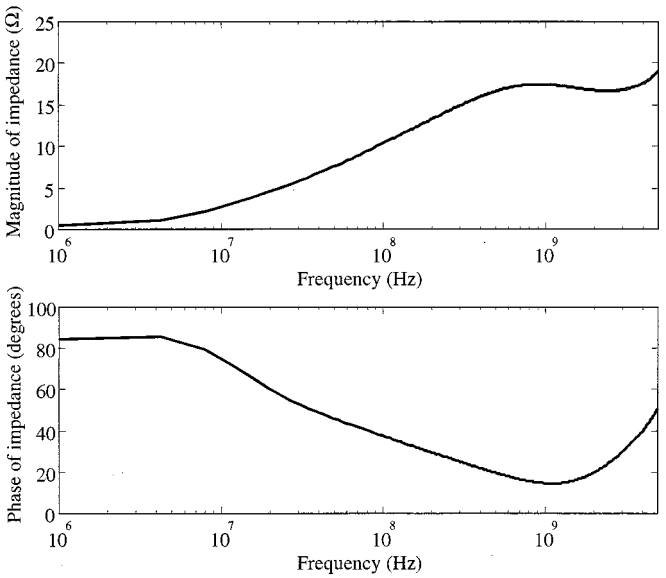

Fig. 8. Measured impedance of an 0805 package size SMT ferrite.

The measured result shown in Fig. 7 has a resonance at approximately 960 MHz. The minimum of the measured $|S_{21}|$ results from the series resonance of C and L_{p2}, and L_{p2} is then readily determined to be 0.58 nH. At the resonance, the impedance of the capacitor is purely resistive, and the ESR can be easily calculated from the $|S_{21}|$ at the minimum, which is approximately $0.4\ \Omega$. The impedance of one individual 0805 package size SMT ferrite was measured using the HP 8753D Network Analyzer, and the result is shown in Fig. 8. Determination of the L_{p1} is difficult since it is related to the redistribution of the current when it flows from the transmission line through the ferrite, and can only be characterized by measurement. Once the Y-parameters are determined, the two-port network can be incorporated into the modeling using the algorithm presented in Section II.

The FDTD cell size for the modeling was $0.5 \times 0.5 \times 0.381$ mm^3. The smallest dimension was used for the board thickness. A sinusoidally modulated Gaussian pulse was applied at Port 1, and Port 2 was terminated with a 50 Ω

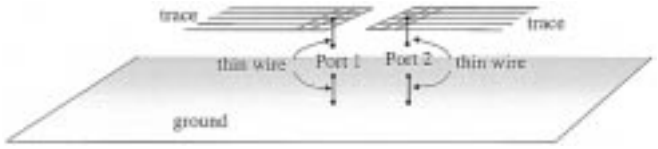

Fig. 9. Schematic of the local subcell modeling for the two-port network.

resistive load. The feeding probe at Port 1 and Port 2 were modeled using a thin-wire algorithm [17]. Eight perfectly matched layers (PMLs) were placed at each boundary plane of the computational domain [21], and seven white space layers were placed between the PML and the test board. The dielectric loss of the FR-4 material was included in the FDTD modeling using a Debye model to approximate the dispersive nature of the material. There are a few algorithms (Z-transform-based, auxiliary differential equation-based, or recursive-based) to incorporate Debye material in the modeling [22]–[24]. This work utilizes the same modeling approach as described in [25], which is a recursive-based approach. Y-parameters were calculated for the filter model shown in Fig. 6, and incorporated into the FDTD modeling. However, in this particular case, the three cells were used to model the thickness of the dielectric and the network port spanned only one cell, as shown in Fig. 9. A connection was made to the trace and ground plane by adding two wires to span the other two cells of the board thickness to ensure current continuity. The connecting wires were modeled with a thin-wire algorithm. This approximation introduced additional parasitics in the modeling, since current had to neck down from the relatively wide trace to the thin wire. The parasitics can also be represented by an inductance that is similar to L_{p1}. However, these additional parasitics only affected the results at very high frequencies, in part because of the substantial series impedance of the ferrites, as shown by the comparison of the measured and modeled result in Fig. 5. Good agreement was achieved between the measurement and the modeled result for $L_{p1} = 0.5$ nH. The modeled results with $L_{p1} = 0$ nH are also shown in the same figure. The results indicate that including the small value of L_{p1} improves the modeling accuracy.

C. Results of a π-Type Filter

Measurement and modeling of a π-type filter were also conducted. The filter consists of one SMT ferrite and two shunt capacitors. The individual component values were the same as those used in the T-type filter, and the circuit layout shown in Fig. 4 was used again. Both shunt capacitors were "buried" in the dielectric as well. The same FDTD modeling approach was used to model the entire board, with the same parasitics L_{p1} for the ferrite, and L_{p2} for the capacitor components. The measured and modeled $|S_{21}|$ is shown in Fig. 10. Good agreement is achieved again between measured and modeled results. The discrepancies at the resonance were due in part to the variance of the lumped element parasitics as well as measurement errors.

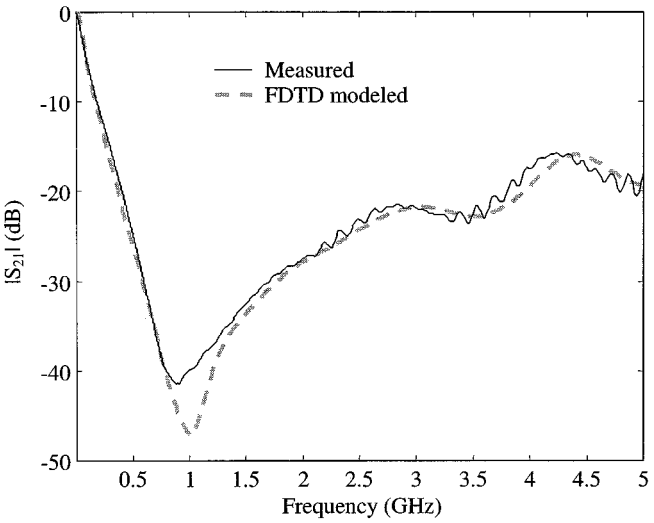

Fig. 10. Measured and FDTD modeled $|S_{21}|$ of a π-type I/O filter.

IV. Including Layout Parasitics in I/O Filtering

The minimum layout parasitics of Board A are usually impractical in actual circuit design. It is hard to "bury" the SMT capacitor in the substrates, and layout and manufacturing constraints typically limit how close the capacitor can be connected to the signal line or the reference plane. This physical interconnect length results in a parasitic inductance, which may have a significant impact on the filtering performance at high frequencies. A second PCB (denoted as Board B) was constructed to demonstrate the modeling approach for investigating the impact of layout parasitics. The schematic of the board is shown in Fig. 11. The layout and components of Board B were the same as that of Board A except that a 1.8-cm long, 2-mm wide trace was introduced between the SMT capacitor and the I/O line. The length of the trace was chosen exceptionally long to demonstrate the effects of layout parasitics, as well as show the utility of the two-port FDTD algorithm for conducting engineering studies. The measured $|S_{21}|$ is shown in Fig. 12, and compared to the measured result of Board A. Board B has a better filtering performance from 100 MHz to 400 MHz due to the resonance shift. However, for higher frequencies, the layout parasitics dominate the effectiveness of the 47 pF SMT capacitor, and the filtering performance of Board B is considerably worse than that of Board A. The results indicate that layout parasitics can significantly impact the performance of the EMI filter.

FDTD modeling of Board B was also conducted. The 1.8-cm long trace was included in the two-port network by considering the impedance looking into the capacitor from the T-junction of the trace as an equivalent lumped impedance, and then the same two-port network modeling approach as that for Board A was used. The 1.8-cm long trace was approximated as an ideal lossless transmission line with characteristic impedance of 52 Ω, and the equivalent lumped impedance was readily calculated from transmission-line theory [20]. Other FDTD modeling details were the same as those for Board A. The modeled result is

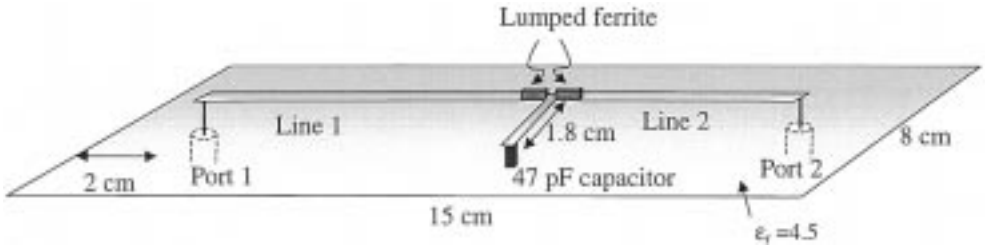

Fig. 11. Schematic of a PCB with a T-type EMI filter—Board B.

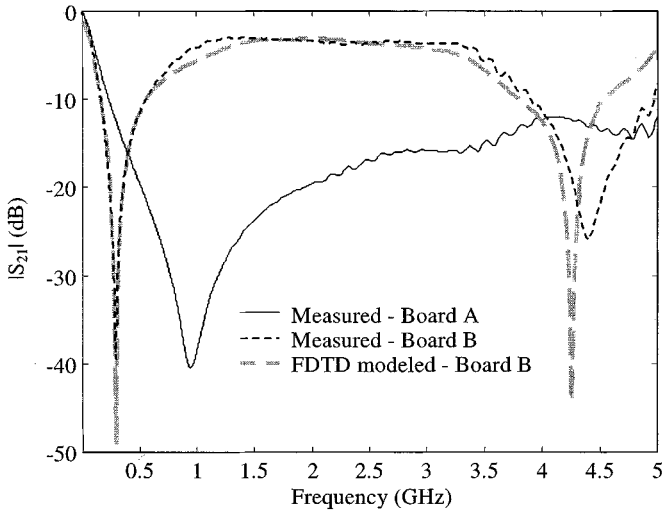

Fig. 12. Measured $|S_{21}|$ of Board A and Board B, and FDTD modeled $|S_{21}|$ of Board B.

also shown in Fig. 12, and good agreement was achieved again between the modeled and measured results over most of the frequency range. The $|S_{21}|$ is nearly flat between 1 GHz and 3.5 GHz because over this frequency range, the impedance of the 1.8-cm transmission line terminated with the 47 pF capacitor is relatively large, and the 50 Ω load resistance at Port 2 works as a voltage divider with the two series SMT lumped ferrites. There is some discrepancy above 4 GHz, which results in part from neglecting the dispersion and loss of the FR-4 in the length of the trace connecting the SMT capacitor. This discrepancy also illustrates the importance of including dispersion and loss for the signal propagation in the FR-4.

V. Conclusion

An algorithm for including passive networks characterized as two-ports into the FDTD method was presented in this work. Of particular interest was the application to EMI filtering of low-speed I/O lines. The method can also include the nonlinear behavior of ferrite components. The two-port filtering networks were included in the modeling by incorporating the time-domain Y-parameters into the FDTD algorithm. The approach was shown with T- and π-filters, and demonstrated with measurements. The method also works using any network parameters that can be converted to Y-parameters, and at least theoretically, for any number of ports.

References

[1] W. Cui, M. Li, X. Luo, and J. L. Drewniak, "Anticipating EMI from coupling between high-speed digital and I/O lines," in *IEEE Int. Symp. Electromagn. Compat.*, Aug. 1999, pp. 189–194.

[2] N. Oka, C. Miyazaki, and S. Nitta, "Radiation from a PCB with coupling between a low-frequency and a digital signal traces," in *IEEE Int. Symp. Electromagn. Compat.*, Aug. 1998, pp. 635–640.

[3] R. L. Ozenbaugh, *EMI Filter Design*. New York: Marcel Dekker, 1996.

[4] S. Wakamatsu, F. Tilley, and G. Hubers, "To reinforce immunities around GHz frequencies by EMI-noise suppression filters," in *IEEE Int. Symp. Electromagn. Compat.*, Aug. 1996, pp. 511–514.

[5] K. Takei, O. Ishii, and M. Senda, "Application of magnetic metal thin films to EMI noise filter," in *IEEE Int. Symp. Electromagn. Compat.*, Aug. 1996, pp. 508–510.

[6] R. G. Munoz, "Simulation of response of modeled EMI filters to measured or simulated time-domain waveforms," in *IEEE Int. Symp. Electromagn. Compat.*, Aug. 1995, pp. 272–275.

[7] M. Li, J. Nuebel, J. L. Drewniak, R. E. DuBroff, T. H. Hubing, and T. P. Van Doren, "EMI from cavity modes of shielding enclosures—FDTD modeling and measurements," *IEEE Trans. Electromagn. Compat.*, vol. 42, pp. 29–38, Feb. 2000.

[8] A. Orlandi and C. R. Paul, "FDTD analysis of lossy, multiconductor transmission lines terminated in arbitrary loads," *IEEE Trans. Electromagn. Compat.*, vol. 38, pp. 388–399, Aug. 1996.

[9] M. Piket-May, A. Taflove, and J. Baron, "FDTD modeling of digital signal propagation in 3-D circuits with passive and active loads," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1514–1523, Aug. 1994.

[10] Y. Tsuei, A. C. Cangellaris, and J. L. Prince, "Rigorous electromagnetic modeling of chip-to-package (first-level) interconnections," *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 16, pp. 876–882, Dec. 1993.

[11] K. Naishadham, "A rigorous experimental characterization of ferrite inductors for RF noise suppression," in *Proc. Radio and Wireless Conf.*, 1999, pp. 271–274.

[12] M. Li, X. Luo, and J. L. Drewniak, "FDTD modeling of lumped ferrites," *IEEE Trans. Electromagn. Compat.*, vol. 42, pp. 142–151, May 2000.

[13] X. Ye and J. L. Drewniak, "Incorporating two-port networks with S-parameters into FDTD," *IEEE Microwave Wireless Comp. Lett.*, vol. 11, pp. 77–79, Feb. 2001.

[14] C. Emili, F. Alimenti, P. Mezranotte, L. Roselli, and R. Sorrentino, "Rigorous modeling of packaged Schottky diodes by the nonlinear lumped network (NL/sup 2/N)-FDTD approach," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 2277–2282, Dec. 2000.

[15] M. Celuch-Marcysiak and W. K. Gwarek, "Implicit incorporation of nonlinear elements for unconditionally stable FDTD analysis at coarse time-steps," in *Proc. IEEE Int. Symp. MTT*, vol. 3, 1996, pp. 1381–1384.

[16] K. S. Yee, "Numerical solution of initial boundary value problems involving Maxwell equations in isotropic media," *IEEE Trans. Antennas Propagat.*, vol. 14, pp. 302–307, 1966.

[17] A. Taflove, *Computational Electrodynamics: The Finite-Difference Time-Domain Method*. Norwood, MA: Artech House, 1995.

[18] K. Kunz and R. Luebbers, *The Finite Difference Time Domain Method for Electromagnetics*. Boca Raton, FL: CRC, 1995.

[19] T. K. Sarkar and O. Pereira, "Using the matrix pencil method to estimate the parameters of a sum of complex exponentials," *IEEE Trans. Antennas Propagat. Mag.*, vol. 37, pp. 48–54, Feb. 1995.

[20] D. M. Pozar, *Microwave Engineering*. New York: Wiley, 1998.

[21] J. P. Berenger, "Perfectly matched layer for the absorption of electromagnetic waves," *J. Comput. Phys.*, vol. 114, pp. 185–200, Oct. 1994.

[22] W. H. Weedon and C. M. Rappaport, "A general method for FDTD modeling of wave propagation in arbitrary frequency-dispersive media," *IEEE Trans. Antennas Propagat.*, vol. 45, pp. 401–410, Mar. 1997.

[23] O. P. Gandhi, B.-Q. Gao, and J.-Y. Chen, "A frequency-dependent finite difference time-domain formulation for general dispersive media," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 658–665, Apr. 1993.
[24] R. Luebbers, F. P. Hunsberger, K. S. Kunz, R. B. Standler, and M. Schneider, "A frequency-dependent finite difference time-domain formulation for dispersive materials," *IEEE Trans. Electromagn. Compat.*, vol. 32, pp. 222–227, Aug. 1990.
[25] X. Ye, "Advances and applications of the finite difference time domain (FDTD) method and scattering parameter measurement techniques for electromagnetic compatibility in high-speed digital design," Ph.D. dissertation, Univ. of Missouri, Rolla, 2000.

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