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Designing Power Bus Decoupling for CMOS Devices

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Abstract: *The adequacy of the DC power bus decoupling for CMOS devices can be determined if the effective board decoupling capacitance, the CMOS load capacitance, the CMOS power dissipation capacitance, the switching time, and the allowable bus noise voltage are known. A simple method is presented for estimating the effective decoupling capacitance. The load and power dissipation capacitance values are shown analytically and experimentally to be closely related to the transient current. The transient current and switching time are used to estimate the transient noise voltage on the power bus.*

I. INTRODUCTION

The decoupling of a printed circuit board (PCB) has become more difficult as a result of continously increasing clock frequencies and edge rates in high-speed digital systems. Ineffective decoupling may lead to excessive power bus noise. As a consequence, conducted EMI and significant common-mode radiation can result. The evaluation of the decoupling network on a PCB proves to be a key issue from an EMC perspective [1], [2].

The simultaneous switching of multiple outputs is one of the main causes of transient noise voltages on the power bus [3]. This noise can be estimated if the effective decoupling capacitance and the transient switching current waveshape are known. For CMOS devices, the switching current can be related to the load capacitance, the power dissipation capacitance, and the switching time. In the analysis below, the following assumptions have been made:

❒ Only CMOS devices are considered for which a power dissipation capacitance C_{PD} is known.
❒ At least one pair of power and ground (return) planes exist on the PCB. This assumption is not necessary, but it does simplify the calculation of trace and via inductances.
❒ The maximum frequency is limited to a value below which power plane transmission line resonances occur.
❒ Only capacitor values smaller than 200 nF are considered. The larger "bulk" capacitors are not usually effective above 10 MHz.
❒ All of the lumped decoupling capacitors are assumed to be connected to the power and ground (return) planes, rather than directly to the power pins of an integrated circuit package. This is not a necessary assumption, but it does simplify the estimation of the total effective capacitance.

Each lumped decoupling capacitor is connected to the power planes through a series inductance formed by the solder pads, traces, vias, and closest plane (power or ground). A reasonable estimate for this inductance can be made by using microstrip formulas for the traces and pads over a plane and experimental measurements for via inductance. Each lumped capacitor then has an impedance magnitude:

$$|Z| = \left|\omega L - \frac{1}{\omega C}\right| = \frac{1}{\omega C_{eff}}$$

where:

$$C_{eff}(\omega) = \left|\frac{C}{1 - \omega^2 LC}\right|$$

In these expressions C_{eff} is the effective value of the decoupling capacitance and L is the self inductance of the loop connecting the capacitor to the planes. The effective decoupling capacitance for each lumped capacitor is arbitrarily limited to a maximum value of 2C. The total effective capacitance for each power bus is the sum of the interplane capacitance and the effective capacitance of each lumped capacitor.

From an EMC point of view it is important to know the high frequency noise on each DC power bus due to the switching of the digital circuits. If the transient current drawn by each IC can

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be estimated, then the noise voltage can be calculated using the simple equation: $i(t) = C_{eff}\, dv/dt$. In order to find the optimum value of the total decoupling C_{eff}, an "allowable" value of dv is needed. From a functional point of view this value can be determined, but usually it is too large for the radiated or conducted EMI. From an EMC point of view the value of an acceptable dv cannot be derived without knowing the antenna and the coupling path, both very specific to each particular design.

II. ESTIMATING THE TRANSIENT CURRENT

The total current drawn by an IC is the sum of the quiescent current, the current associated with the inputs, the internal current, and the output currents. The quiescent current is less than 150 µA. For data inputs, a typical current is less than 1.5 mA/input at 3.4V, and for a control input, less than 3 mA/input at 3.4V. The design must take into account the particular type of the CMOS logic device (MG, HC, FACT, LVC, LVX, ASICs), but for high-speed CMOS circuits, the quiescent and input current values are an order of magnitude lower than the internal and the output currents, and can be neglected. The internal current are mainly the "through" current when both transistors in the output stage are active, and the load currents are due to the capacitance of the driven circuits.

For thermal calculations involving CMOS circuits, the data books give information about the power dissipation associated with the internal currents by giving the value of an equivalent "power dissipation capacitance C_{PD}". C_{PD} acts like an increase of the load capacitance to account for the supplementary internal current. Typical values are in the range of 15 - 40 pF/output. Other catalogs give the value of the "dynamic power supply current I_{CCD}", with typical values in the range 300 - 800 µA/MHz/bit.

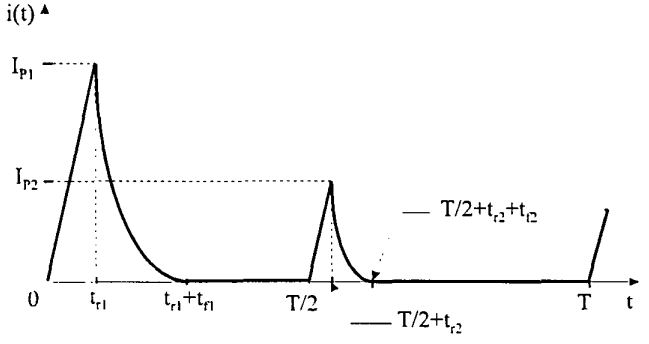

Figure 1. The wave shape of the transient current drawn by each IC, in the loaded case.

From experiments and data found in the literature [3], the transient current can be well approximated as a triangular shaped waveform associated with each edge of the clock, or only with one edge of the clock for flip-flop like circuits. As shown in Figure 1, the rising edge was considered linear, and the falling edge exponential, to take into account the effect of the load.

For the unloaded case, at each commutation of the output stage a transient current will be drawn from the power bus. In the absence of load, the HI-LO, and the LO-HI transition will draw equal currents. So, $I_{P1} = I_{P2}$, and $\Delta t_1 = \Delta t_2$,, where $\Delta t_1 = t_{r1} + t_{f1}$, and $\Delta t_2 = t_{r2} + t_{f2}$. The peak transient current is given by:

$$I_{p1} = I_{p2} = \frac{C_{PD} V_{CC}}{\Delta t} = \frac{I_{CCD}}{\Delta t}$$

where: I_{P1} [mA], V_{CC} [V], Δt [ns], C_{PD} [pF], $I_{CC}(D)$ [µA/MHZ]. If the switching frequency is f_o, the spectrum of the transient current will have stronger harmonics of $2f_o$, and the odd harmonics of f_o will appear mainly as a result of the slight differences in amplitude and shape of the current pulses.

The effect of a capacitive load can be easily taken into account:

$$I_{p1} = \frac{(C_{PD} + C_L) V_{CC}}{\Delta t} = \left| \frac{C_{PD} + C_L}{C} \right| \frac{I_{CCD}}{\Delta t}$$

In this case $I_{P1} >> I_{P2}$, because the load is important only for one of the switching edges. Each transient current must be calculated using the appropriate switching time and capacitance. If $C_L >> C_{PD}$, the asymmetry between I_{P1} and I_{P2} will be important. The harmonics of f_o will have much more energy than in the unloaded case, and the odd and even harmonics will have almost equal amplitude.

This approach was experimentally verified, and the agreement between the estimation of the peak current based on C_{PD} and the measured value is good.

For ASICs the estimation is more difficult, but typically CMOS technology is used. Most ASICs have an internal "core" and a ring of output stages, similar to buffers. The ring of output stages run at lower frequencies, but usually switch higher currents and may have significant capacitive loads, up to 50 pF. Therefore, the necessary decoupling may be estimated based on the transient output currents typical for buffers.

III. THE POWER BUS NOISE

From Figure 1, using the same methodology and notations as in [6], the amplitude of each harmonic of the Fourier series for

the transient current drawn from the power bus is:

$$a_n = -\frac{I_{p1}T}{n^2\pi^2}\left[\frac{\sin^2(\pi f_n t_{r1})}{t_{r1}} - \frac{\sin(\beta_{n1})\sin(\omega_n t_{r1} + \beta_{n1})}{t_{F1}}\right] + \frac{I_{p2}T}{n^2\pi^2}\left[\frac{\sin^2(\pi f_n t_{r2})}{t_{r2}} - \frac{\sin(\beta_{n2})\sin(\omega_n t_{r2} + \beta_{n2})}{t_{F2}}\right](-1)^n$$

$$b_n = \frac{I_{p1}T}{n^2\pi^2}\left[\frac{\sin(\pi f_n t_{r1})\cos(\pi f_n t_{r1})}{t_{r1}} - \frac{\sin(\beta_{n1})\cos(\omega_n t_{r1} + \beta_{n1})}{t_{F1}}\right] + \frac{I_{p2}T}{n^2\pi^2}\left[\frac{\sin(\pi f_n t_{r2})\cos(\pi f_n t_{r2})}{t_{r2}} - \frac{\sin(\beta_{n2})\cos(\omega_n t_{r2} + \beta_{n2})}{t_{F2}}\right](-1)^n$$

where: $f_n = nf = nf_0 = n/T$, and $\omega_n = 2\pi f_n$. The following notations were used:

$$t_{F1} = \frac{t_{f1}}{e}$$

$$t_{F2} = \frac{t_{f2}}{e}$$

$$\beta_{n1} = \arctan(\pi f_n t_{F1})$$

$$\beta_{n2} = \arctan(\pi f_n t_{F2})$$

$$\sin(\beta_{n1}) = \frac{\pi f_n t_{F1}}{\sqrt{1 + (\pi f_n t_{F1})^2}}$$

$$\sin(\beta_{n2}) = \frac{\pi f_n t_{F2}}{\sqrt{1 + (\pi f_n t_{F2})^2}}$$

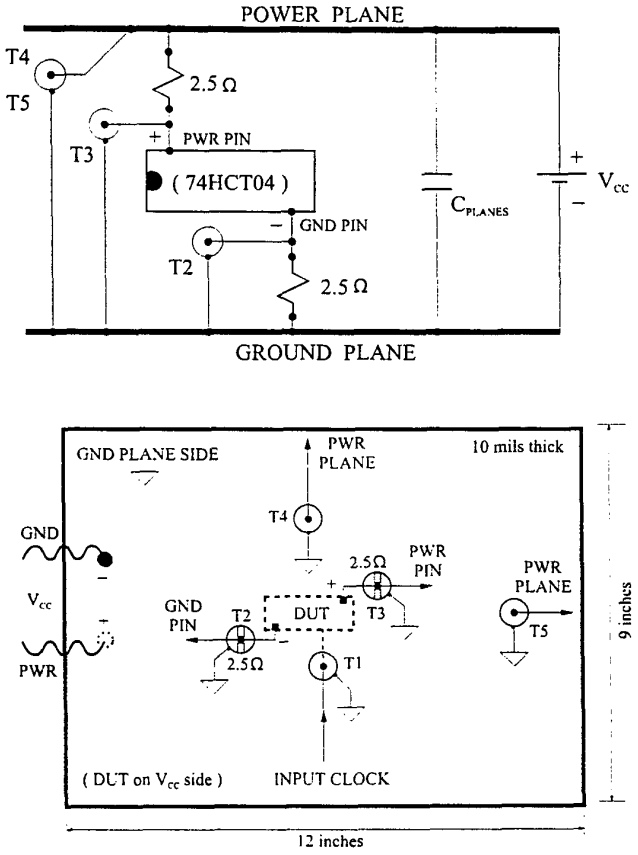

Figure 2. The schematic diagram and the layout of the experimental setup.

$$\cos(\beta_{n1}) = \frac{1}{\sqrt{1 + (\pi f_n t_{F1})^2}}$$

$$\cos(\beta_{n2}) = \frac{1}{\sqrt{1 + (\pi f_n t_{F2})^2}}$$

Knowing the spectrum of the transient current, the magnitude of each harmonic of the power bus noise $V(nf_0)$, can be calculated:

$$|V(nf_0)| = \frac{|I_n|}{2\pi n f_0 C_{eff}(nf_0)}$$

where: $|I_n| = \sqrt{a_n^2 + b_n^2}$

IV. EXPERIMENTAL MEASUREMENTS

In order to verify the transient current estimation and the link with the generated power bus noise voltage, a series of experiments were defined. The experimental setup is presented in Figure 2. A two sided 10 mils thick circuit board was used to achieve a large interplane capacitance. The dimensions of the board were 9 x 12 inches. SMA connectors were used for all of the test points. The 2.5 Ω current sensing resistors were obtained by placing four 10 Ω surface mounted resistors in parallel.

All of the SMA connectors were mounted on the ground plane side. The DUT and the current sensing resistors were mounted on the opposite side (V_{cc}). The T1 point is the clock input for the circuit, T2 is the test point for the voltage across the resistor in the ground lead, T3 for the voltage across the resistor in the power lead, T4 and T5 for the voltage between power and ground planes at two different locations. Several types of CMOS devices were used in the experiments, and in Figures 3-6 sample results with 74HCT04 (C_{PD}=22pF per inverter) are presented [4].

In Figure 3 only one inverter was clocked and the results at the test points T2 (voltage across ground lead resistor) and T4 (voltage between power planes) are presented. Even with efforts to keep test fixture parasitics under control, some oscillation after the falling edge is still present. However, for peak current and switching time estimation, the rising edge is enough. The voltage at the test point T2 is directly proportional to I_{GND}, from the figure it results that $I_P \cong 18$ mA. Using the C_{PD} value from the data sheets and the experimentally estimated switching time ($\Delta t \cong 6$ ns), the same value for the peak current can be obtained. In Figure 4 the same experiment is repeated with all six inverters simultaneously switched. The voltage at the test point T3 is directly proportional with I_{PWR} (= I_{CC}), and again the agreement is very good. The measured value for the peak current is $I_P \cong 80$ mA, and the estimation based on C_{PD} is $I_P \cong 82$ mA. In Figure 5 the power bus voltage in two different locations (T4 and T5) is shown, for the Low - High output transition. In this experiment all the six outputs were loaded with 47 pF each (surface mounted), and were switched simultaneously.

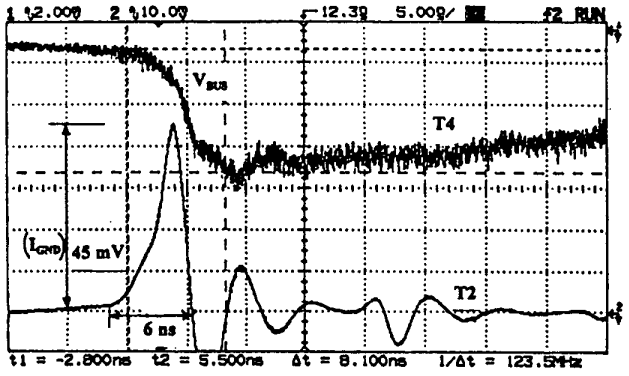

Figure 3. Transient current through the GND pin, and bus voltage for 74HCT04 (1 input clocked, no load).

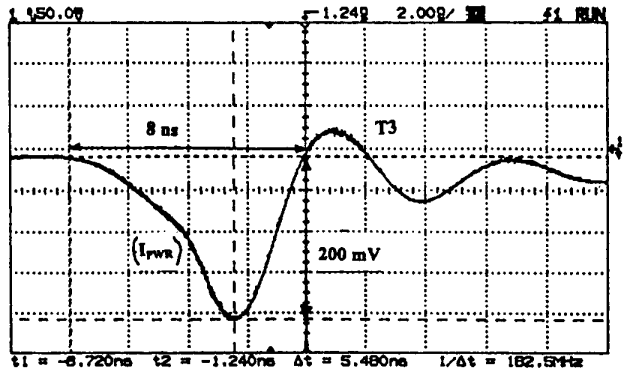

Figure 4. Transient current through the PWR pin for 74HCT04 (6 inputs clocked, no load).

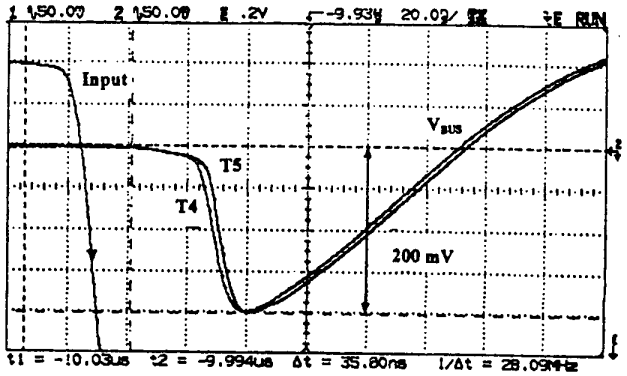

Figure 5. Transient bus voltage at two different locations for output going High (74HCT04, 6 inputs clocked, each output loaded with C_L = 47 pF).

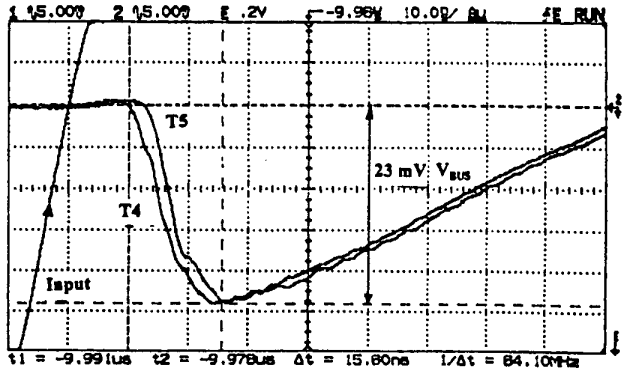

Figure 6. Transient bus voltage at two different locations for output going Low (74HCT04, 6 inputs clocked, each output loaded with C_L = 47 pF).

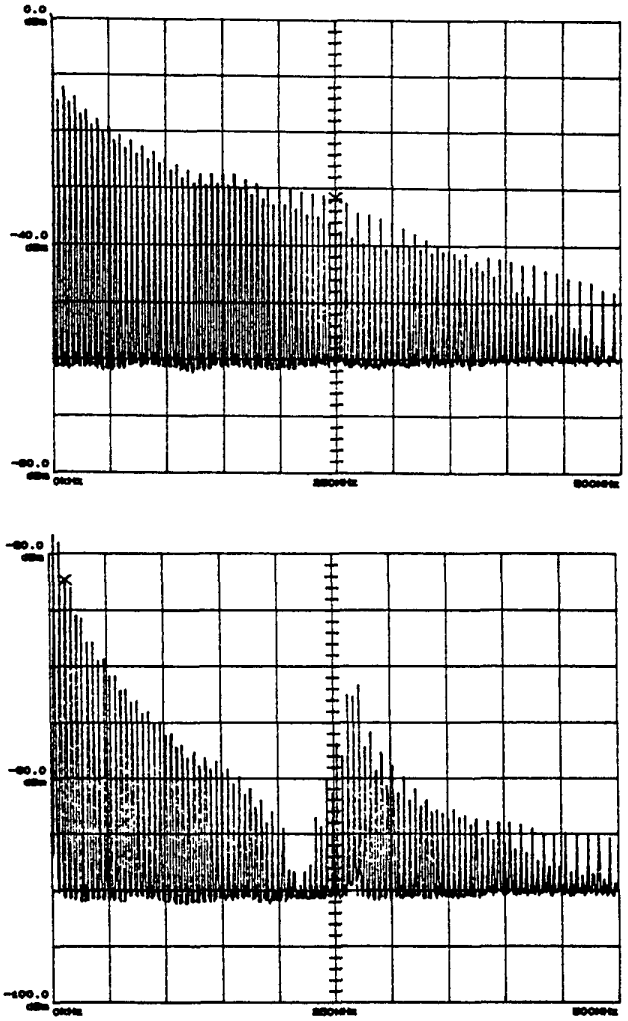

Figure 7. The frequency spectrum of the a) current through the ground pin T2 (REF 0 dBm, 10 dB/div, 50 MHz/div), and b) voltage between power planes T5 (REF-20 dBm, 10 dB/div, 50 MHz/div) , experimentally measured (loaded).

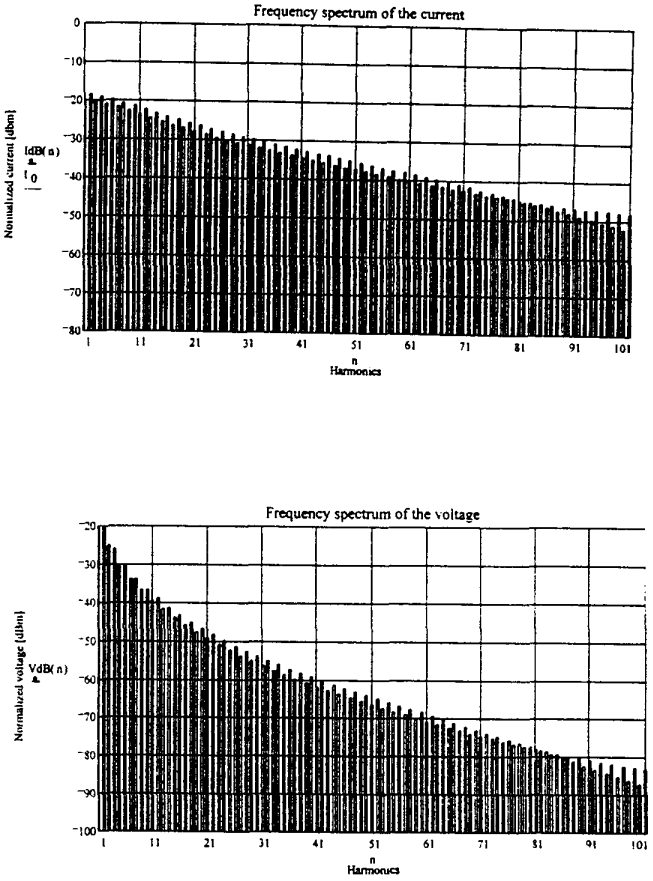

Figure 8. The frequency spectrum of the a) current through the ground pin T2 (REF 0 dBm, 10 dB/div, 50 MHz/div), and b) voltage between power planes T5 (REF -20 dBm, 10 dB/div, 50 MHz/div), calculated (loaded).

differences between the experimental and the calculated result, the agreement is good. The envelope is almost at the same level in both cases. For EMI problems the highest peaks are the real concern, and the calculations presented give a acceptable prediction of the peaks. Note that for the unloaded case, Figures 9 and 10, the dominate harmonics occur at twice the fundamental switching.

In Figures 7 - 10 the switching frequency is 5 MHz. In all these figures the frequency range is 500 MHz (0 - 500 MHz), but in Figures 8 and 10 the order of the harmonics is indicated. In all graphics, on the horizontal axis, the grid is at 50 MHz/div. On the vertical axis the grid is always at 10 dB/div.

V. SUMMARY AND CONCLUSIONS

The data presented above show that by using only typical switching time and C_{PD} or I_{CCD} catalog data for a CMOS IC, the waveshape of the transient current drawn by the circuit can be estimated with good accuracy. This information can be used to estimate the frequency spectrum of the noise voltage on the power bus. This voltage can be the source of conducted and/or radiated EMI.

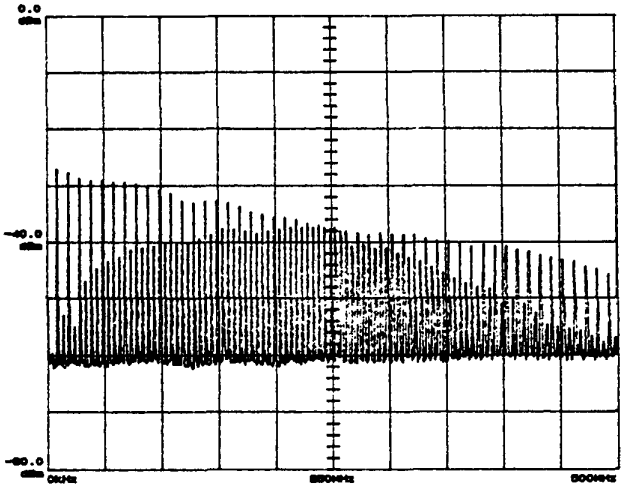

Figure 9. The frequency spectrum of the current through the ground pin T2 (REF 0 dBm, 10 dB/div, 50 MHz/div), experimentally measured (unloaded).

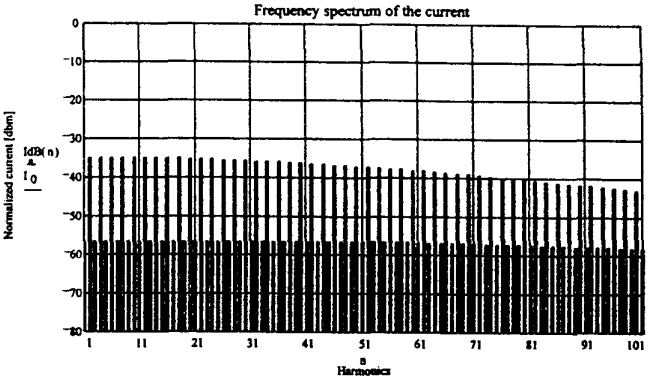

Figure 10. The frequency spectrum of the current through the ground pin T2 (REF 0 dBm, 10 dB/div, 50 MHz/div) calculated (unloaded).

This research is part of the effort to find an optimum solution for the "Power Bus Decoupling Algorithm", which is part of the "EMI Expert System" [5]. This software tool is under development by "The University of Missouri-Rolla EMI Expert System Consortium".

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