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Analysis of a Novel Four-Level DC/DC Boost Converter

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Abstract - In this paper, novel two-quadrant buck/boost and one-quadrant boost four-level DC/DC converters are introduced. The primary application for these converters is that of interfacing a low voltage DC source, such as a fuel cell or battery, to a high-voltage four-level inverter. One important feature of the four-level DC/DC converters proposed herein is the ability to perform the power conversion and balance the inverter capacitor voltages simultaneously. With the capacitor voltage balancing, it is possible to obtain the full voltage from the inverter. For the boost converter, the steady-state and Non-Linear Average-Value (NLAM) models are developed. The NLAM is verified against a detailed simulation of a four-level converter/inverter drive system.

Keywords: Multi-level converters, four-level converters, DC/DC converters, average-value modeling, triangle modulation, current-regulated control.

I. INTRODUCTION

The general trend in power electronics devices has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. However, the increase in switching frequency increases the switching losses which become especially significant at high power levels. Several methods for decreasing switching losses have been proposed including constructing resonant inverters and multi-level inverters [1].

Resonant inverters avoid switching losses by adding an LC resonant circuit to the hard switched inverter topology. The inverter transistors can be switched when their voltage or current is zero, thus mitigating switching losses. Examples of this type of inverter include the resonant DC link [2], and the Auxiliary Resonant Commutated Pole inverter (ARCP) [3,4]. One disadvantage of resonant inverters is that the added resonant circuit will increase the complexity and cost of the inverter control. Furthermore, high IGBT switching edge rates can create switch level control problems.

Multi-level inverters offer another approach to reducing switching losses. In particular, these converters offer a high number of switching states so that the inverter output voltage can be "stepped" in smaller increments [5-11]. This allows mitigation of harmonics at a low switching frequencies thereby reducing switching losses. In addition, EMC concerns are reduced through the lower common mode current facilitated by lower dv/dt's produced by the smaller voltage steps. One disadvantages of these techniques are that they require a high number of switching devices. The primary disadvantage of multi-level inverters is that they must be supplied from isolated DC voltage sources or a bank of series capacitors with balanced voltages. In systems where isolated DC sources are not practical, capacitor voltage balancing becomes the principal limitation for multi-level inverters.

One of the most popular industrial multi-level inverters is the diode clamped three-level inverter [5,7,8,10]. It has been well established that the DC capacitor voltages can be readily balanced through the use of straightforward selection of redundant inverter switching states [10]. However, for inverters with a higher number of levels, the voltage balancing through redundant state selection limits the output voltage to 50% of the maximum [12,13]. For this reason, some systems incorporate auxiliary DC/DC converters for capacitor voltage balancing [14-17]. Some interesting three-level boost DC/DC converters have been proposed for systems that are powered from a low-voltage source such as a battery, fuel cell, or Superconducting Magnetic Energy Storage (SMES) [18-20]. In this paper, a novel four-level DC/DC converter is presented. The standard steady-state and average-value modeling techniques are applied to this new converter. Detailed and average-value model simulation demonstrates the converter performance.

II. PROPOSED FOUR-LEVEL DC/DC CONVERTER

A. Converter Description

Figure 1 shows the novel four-level two-quadrant converter proposed herein. This converter can operate as a boost or buck converter depending on whether the DC source v_{dc} is supplying or absorbing power respectively. For many applications, bi-directional power flow is not necessary and the semiconductor parts count can be reduced to the topology shown in Figure 2. In a standard boost converter, one transistor and one diode are used for the boost process [21,22]. In this new topology, two additional transistors are added in order to provide additional switching states that can be used to balance the capacitor voltages. It should be pointed out that although there are three times as many transistors as with a standard boost converter, the switches are rated at 1/3 of the DC voltage and thus the overall semiconductor cost is roughly the same. Figure 3 shows the possible switching states of the four-level DC DC converter. States 0 and 4 are the two states typically used for DC/DC boost conversion. Due to the nature of the motor impedance load and the switching of the four-level inverter transistors, the voltage of the center capacitor v_{c2} tends to discharge to zero in this system.

Figure 1. Proposed 4-level two-quadrant DC/DC converter.
Figure 2. Proposed 4-level one-quadrant boost converter.

For this reason, state 1 is inserted in the switching sequence order to increase the charge on the center capacitor. A secondary goal of this converter is to balance the voltages on the upper and lower capacitors. Although this is typically not difficult in four-level inverters, states 2 and 3 can be added to ensure this balance.

B. Switching Sequence

One advantage of multi-level DC/DC power conversion is a reduction in the inductor current ripple when compared to a standard DC/DC converter. For the three-level DC/DC converter, a reduction in current ripple can be accomplished by defining the switching sequence as a function of the input and output voltages [18-20]. In the case of the four-level converter, it is not possible to reduce the current ripple for all operating conditions and simultaneously balance the capacitor voltages. Therefore, one sequence has been chosen with the objective of balancing the capacitor voltages. The overall switching state sequence suggested for this converter is 0 - 1 - (2 or 3) - 4 - (2 or 3) - 1 - 0. The state diagram for this sequence is shown in Figure 4.

Note that this sequence is similar to that of a standard DC/DC converter with two additional switching states. Two additional duty cycles are defined in the sequence timing for control of the additional states. The timing sequence is defined by

$$\text{state} = \begin{cases} 0, & 0 \leq t < d_1 T \\ 1, & d_1 T \leq t < (d_1 + d_2) T \\ 2/3, & (d_1 + d_2) T \leq t < (d_1 + d_2 + d_3) T \\ 4, & (d_1 + d_2 + d_3) T \leq t < T \end{cases}$$

where $d_1$, $d_2$, and $d_3$ are the controller duty cycles and $T$ is the total time spent in the switching states. The remainder of the sequence is to reverse the order spending the same amount of time in each state as before. Therefore, the total time of the switching controller is $T_w = 2T$.

The amount of time spent at the particular switching state can be controlled depending on the desired output voltage and the capacitor voltage imbalance. For example, the time spent at switching state 1 can be increased in order to increase the voltage across the center capacitor. The time spent at states 2 and 3 can be controlled to maintain the voltage balance between the upper and lower capacitors. The choice as to which state to switch to during the sequence (2 or 3) is made depending on which of the two capacitor voltages $v_{cl}$ or $v_{cl}$ is underbalanced with respect to the other.

C. Steady-State Modeling

As with other types of DC/DC converters, it is instructive to perform a steady-state analysis of the converter driving a resistive load [18-21]. In the case of the four-level boost converter, the circuit topology is that of Figure 5. Since the goal of this converter is to equalize the capacitor voltages, it will be assumed that the controller duty cycles have been set so that the capacitor voltages are equal, or
Figure 5. Four-level converter with resistive load.

\[ v_{c1} = v_{c2} = v_{c3} = \frac{v_c}{3}. \]  

(2)

It will also be assumed that \( R_1 > R_2 \) so that switching state 3 is used during the time when there is a choice between states 2 and 3. The resulting inductor current waveform is shown in Figure 6. For steady-state periodic operation, it is necessary that the average inductor voltage be zero. From this requirement, the output to input voltage ratio can be determined as

\[ \frac{v_c}{v_{dc}} = \frac{1}{1 - d_1 - \frac{2}{3} d_2 - \frac{1}{3} d_3}. \]  

(3)

Assuming that the converter losses are negligible, the average inductor current can be found from the output power and input voltage as

\[ I_{avg} = \frac{v_c^2}{9v_{dc}} \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right). \]  

(4)

From the load equations and the fact that the average capacitor currents must be zero, it can be shown that the steady-state currents, defined in Figure 6, are

\[ I_1 = I_{avg} + \frac{d_3 T_{sw}}{6L} (2v_c - 3v_{dc}) + \ldots \]

\[ \frac{T_{sw}}{2L} (1 - d_1 - d_2 - d_3)(v_c - v_{dc}) + \ldots \]

\[ d_2 I_{avg} + \frac{d_3 T_{sw}}{6L} (v_c - 3v_{dc}) \]

(5)

\[ I_2 = I_{avg} + \frac{d_3 T_{sw}}{6L} (2v_c - 3v_{dc}) + \ldots \]

\[ \frac{T_{sw}}{2L} (1 - d_1 - d_2 - d_3)(v_c - v_{dc}) \]

\[ d_2 I_{avg} + \frac{d_3 T_{sw}}{6L} (v_c - 3v_{dc}) \]

(6)

\[ I_3 = I_{avg} + \frac{d_3 T_{sw}}{6L} (2v_c - 3v_{dc}) + \ldots \]

\[ \frac{T_{sw}}{2L} (1 - d_1 - d_2 - d_3)(v_c - v_{dc}) \]

By waveform symmetry,

\[ I_4 = 2I_{avg} - I_3 \]  

(8)

\[ I_5 = 2I_{avg} - I_2 \]  

(9)

\[ I_6 = 2I_{avg} - I_1. \]  

(10)

For design purposes, it is often desirable to calculate the inductor current ripple \( \Delta \). From (5-10), it can be seen that

\[ \Delta I_L = 2(\max(I_1, I_2, I_3) - I_{avg}). \]  

(11)

Note that the maximum current \((I_1, I_2, \text{ or } I_3)\) depends on the shape of the inductor current and thus depends on the DC input and capacitor voltages. Regardless of which current is the maximum, it can be seen that the inductor current ripple decreases with increasing switching frequency, inductance, and load resistance as is typical of DC/DC converters.

It may be desirable to calculate the required duty cycles for a given set of load resistances. In this case, setting the average capacitor currents to zero yields three equations which can be solved for duty cycles resulting in

\[ d_1 = 1 - \frac{3v_{dc}}{R_2v_c \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)} \]  

(12)

\[ d_2 = \frac{3v_{dc}}{v_c \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)} \]  

(13)

\[ d_3 = \frac{v_{dc}}{v_c \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)} \]  

(14)

The steady-state model equations presented herein have been verified through the use of detailed computer simulation. Although the steady-state model is useful for design calculations, a dynamic model is needed for evaluating system transient performance.

(7) D. Non-Linear Average-Value Modeling

The general concept of Non-Linear Average-Value Models (NLAM's) is that the high-frequency switching of the power
determining the dependant source equations are shown in Figure 8 with the assumption that \( v_{cl} \) and state 3 is not used. If the inductor current ripple is neglected, the average-value equations are

\[
\dot{v}_{sw} = \dot{v}_{c2} (1 - d_1) + \dot{v}_{c1} (1 - d_1 - d_2) + \cdots \\
\dot{v}_{c3} (1 - d_1 - d_2 - d_3)
\]

(15)

\[
i_{L1} = -i_{dc} d_2
\]

(16)

\[
i_{L2} = i_{dc} (d_2 + d_3)
\]

(17)

\[
i_{L3} = i_L (1 - d_1 - d_2 - d_3)
\]

(18)

If \( v_{c2} > v_{c3} \), then the average-value equations become

\[
\dot{v}_{sw} = \dot{v}_{c2} (1 - d_1) + \dot{v}_{c3} (1 - d_1 - d_2) + \cdots \\
\dot{v}_{c1} (1 - d_1 - d_2 - d_3)
\]

(19)

\[
i_{L1} = -i_{dc} (d_2 + d_3)
\]

(20)

\[
i_{L2} = i_{dc} d_2
\]

(21)

\[
i_{L3} = i_L (1 - d_1 - d_2)
\]

(22)

For four-level inverter loads, the unbalance of capacitor voltages \( v_{c2} \) and \( v_{c3} \) is not severe and the controller will select state 2 over state 3 about one-half of the time. In this case, the two sets of equations can be averaged to yield one model. For example, an equation for \( v_{sw} \) can be obtained by averaging (15) and (19).

The NLAM can be used to evaluate the dynamic and steady-state performance of the converter including the high-frequency switching of the controller. If a resistive load is connected to the NLAM, equations (3) and (12-14) can readily be derived. Alternatively, an NLAM of a four-level inverter can be connected to the converter NLAM for dynamic modeling of the system depicted in Figure 2.

### III. FOUR-LEVEL INVERTER

Figure 9 illustrates a four-level diode clamped inverter [6, 8, 12, 13]. The general theory of this inverter is that each phase (a, b, or c) can be electrically connected to the junctions \( d_a, d_b, d_c \), and \( d_d \) by appropriate switching of the inverter transistors. Assuming that the IGBT’s operate as ideal switched, the \( \alpha \)-phase switching can be modeled by an ideal positional switch as shown in Figure 10. The \( b \) - and \( c \)-phase circuits can be modeled by similar switches connecting to the same capacitor junctions. By pulse-width modulation of the positional switch, the inverter line-to-ground voltages \( v_{ag}, v_{bg} \), and \( v_{cg} \) can be directly controlled. The motor line-to-neutral voltages can be calculated from the line-to-ground voltages by [23].

\[
v_{as} = \frac{2}{3} v_{ag} - \frac{1}{3} v_{bg} - \frac{1}{3} v_{cg}
\]

(23)

\[
v_{bs} = \frac{2}{3} v_{bg} - \frac{1}{3} v_{ag} - \frac{1}{3} v_{cg}
\]

(24)

\[
v_{cs} = \frac{2}{3} v_{cg} - \frac{1}{3} v_{ag} - \frac{1}{3} v_{bg}
\]

(25)

In most motor control systems, the commanded phase currents are determined from the desired torque. A regulating control then generates commanded motor phase voltages based on the commanded currents. In general, these commanded voltages can be expresses as

\[
v_{as}^* = \sqrt{2} v_s^* \cos(\theta_a)
\]

(26)

\[
v_{bs}^* = \sqrt{2} v_s^* \cos(\theta_b - \frac{2 \pi}{3})
\]

(27)
By comparing (33-35) to (26-28), it can be seen that the desired voltage magnitude and phase angle can be set by selecting $m$ and $0$, in (29-31). Typically, (29-31) are normalized to the DC voltage $v_\text{dc}$. This yields duty cycles defined by

$$d_a = \frac{1}{2} \left[ 1 + m \cos(\theta_c) - \frac{m}{6} \cos(3\theta_c) \right]$$

$$d_b = \frac{1}{2} \left[ 1 + m \cos(\theta_c - \frac{2\pi}{3}) - \frac{m}{6} \cos(3\theta_c) \right]$$

$$d_c = \frac{1}{2} \left[ 1 + m \cos(\theta_c + \frac{2\pi}{3}) - \frac{m}{6} \cos(3\theta_c) \right]$$

The duty cycles can then be integerized to determine the switching states for the PWM control. For example, if the $a$-phase duty cycle is integerized by

$$l_a = \text{INT}(3d_a)$$

then the PWM switching will be between levels $s_2=l_a$ and $s_1=l_a+1$. If the clock frequency of the PWM controller is $T_c$, then the $a$-phase switching states for one cycle are

$$s_a = \begin{cases} l_a + 1, & 0 \leq t < (3d_a-l_a)T_c \\ l_a, & (3d_a-l_a)T_c \leq t \leq T_c \end{cases}$$

For the purposes of system model comparison, an average-value model of the four-level inverter has been developed. The structure of the $a$-phase of the average-value model is shown in Figure 11. Figure 12 shows the first step in the derivation of the average-value model dependant source equations. Therein, the modulation duty-cycle is plotted versus the controller electrical angle. The functions $s_1$, $s_2$, and $s_3$ represent the percent of time that the $a$-phase is switched to junctions $d_2$, $d_3$, and $d_1$, respectively. These switching functions are related to the $a$-phase duty cycle as shown in Figure 12. Using these switching functions, the currents drawn from the diode junctions are defined by
Table I. Induction motor parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( r_2 )</td>
<td>0.4 ( \Omega )</td>
</tr>
<tr>
<td>( P )</td>
<td>4</td>
</tr>
<tr>
<td>( r_2' )</td>
<td>0.227 ( \Omega )</td>
</tr>
<tr>
<td>( L_a )</td>
<td>5.7 mH</td>
</tr>
<tr>
<td>( L_{as} )</td>
<td>64.4 mH</td>
</tr>
<tr>
<td>( L_{as}' )</td>
<td>4.6 mH</td>
</tr>
</tbody>
</table>

The induction motor is operating at a constant speed of 183.3 rad/sec and a constant electrical frequency of 60 Hz ensured by setting

\[ \theta_c = 2\pi f t \]  \hspace{1cm} (45)

Figures 11 and 12 illustrate the average-value model of the four-level inverter and the A-phase duty cycle and switching functions, respectively.

Four-Level System Simulations

Detailed and NLAM based simulations were performed on the converter / inverter system shown in Figure 2. The induction motor used in these studies is a 3.7kW machine with the parameters listed in Table I [23].

Use of this control was justified by examining the sensitivity of the system outputs (capacitor voltages) to the changing inputs (duty cycles). Using the NLAM, it was observed that the capacitor voltage \( v_{c3} \) was more sensitive to changes in \( d_2 \) than \( v_{c1} \) or \( v_{c2} \). Furthermore, \( v_{c1} \) and \( v_{c3} \) were more sensitive to changes in \( d_1 \) than \( v_{c2} \). This sensitivity somewhat decouples the control and allows for the following approximate control to be used.

\[ d_1 = K_{p1} e_1 + K_{i1} \int e_1 dt \]  \hspace{1cm} (46)
\[ d_2 = K_{p2} e_2 + K_{i2} \int e_2 dt \]  \hspace{1cm} (47)

where the errors \( e_1 \) and \( e_2 \) are defined by

\[ e_1 = v_{c1} - v_c \]  \hspace{1cm} (48)
\[ e_2 = v_{c2} - v_{c2} \]  \hspace{1cm} (49)

The commanded converter output voltage \( v_{c1}^* \) was set to a constant value of 318 V. The commanded voltage on the center capacitor was set to

\[ v_{c2}^* = \frac{1}{3} v_c \]  \hspace{1cm} (50)

The third duty cycle was set to a constant value of \( d_3 = 0.05 \). For this study, the PI controller gains were set to the values listed in Table II.

Table II. Converter PI controller gains

<table>
<thead>
<tr>
<th>Gain</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( K_{p1} )</td>
<td>0.001</td>
</tr>
<tr>
<td>( K_{i1} )</td>
<td>0.2</td>
</tr>
<tr>
<td>( K_{p2} )</td>
<td>0.01</td>
</tr>
<tr>
<td>( K_{i2} )</td>
<td>0.5</td>
</tr>
</tbody>
</table>
The DC input voltage was $v_{dc} = 150$ V and the controller switching period was $T_{sw} = 0.1$ ms. The converter inductance value was $L = 10$ mH. The capacitor values were unevenly distributed so that the voltage ripple of all capacitors would be roughly the same in the detailed model. The values used were $C_1 = C_2 = 9900 \mu F$ and $C_3 = 3300 \mu F$.

![Figure 13. Detailed model prediction of system performance during a step change in modulation index.](image1)

![Figure 14. NLAM model prediction of system performance during a step change in modulation index.](image2)

Figures 13 and 14 show the simulation results for the detailed and NLAM models respectively. As can be seen, the capacitor voltages drop when the inverter modulation index is increased. The regulating control on the DC/DC converter then controls the duty cycles so that the capacitor voltages return to their desired values. The inductor current increases as the power to the motor...
increases. Notice from the detailed model that there are two components to the inductor current ripple. One component is due to the converter switching and the other is due to the capacitor voltage ripple. Figures 13 and 14 also display the controller duty cycles. Note that for \( m = 0.6 \), the duty cycle \( d_1 \) is very low. This suggests an alternate switching sequence for \( m = 0.6 \) where the switching state \( 0 \) is eliminated and the inductor current ripple is reduced as compared to a standard boost converter.

V. CONCLUSION

A novel four-level DC/DC converter has been introduced. The main objective of this converter is to supply a four-level diode-clamped inverter and provide capacitor voltage balancing as well as perform a boost operation. With the capacitor balancing controlled by the converter, the inverter can be operated up to its full output voltage (as compared to 50% of full output voltage when balancing the capacitors with the inverter switching). Steady-state and average-value modeling of the proposed converter is presented. A simulation study on the converter/inverter system demonstrates that the average-value model prediction compares favorably to a detailed simulation.

REFERENCES


Keith A. Corzine received the BSEE, MSE, and Ph.D. degrees from the University of Missouri - Rolla in 1992 and 1994, and 1997 respectively. In the Fall of 1997 he joined the University of Wisconsin - Milwaukee as an assistant professor. His research interest include the design and modeling of electric machinery and electric drive systems. Contact: kcor@ece.wisc.edu.

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