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Chen Wang

Jun Fan Missouri University of Science and Technology, jfan@mst.edu

James L. Knighten

Norman W. Smith

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1295

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The Effects of Via Transitions on Differential Signals

Chen Wang, Jun Fan*, James L. Knighten*, Norman W. Smith*, Ray Alexander*, James L. Drewniak

Electromagnetic Compatibility Laboratory University of Missouri-Rolla, Rolla, MO 65409 Tel: (573) 341-4969 Fax: (573) 341-4532 cwang@umr.edu, drewniak@ece.umr.edu

*NCR Corporation 17095 Via del Campo, San Diego, CA 92127 Tel: (858) 485-3167 Fax: (858) 485-3788 jun.fan@ncr.com

Abstract

Vias in differential transmission lines have been modeled using the finite-difference time-domain (FDTD) method. The velocity that the differential signal propagated through the vias was estimated. Differential S-parameters were calculated up to 50 GHz. Below 10 GHz, the differential signal can propagate through vias without much reflection and distortion. However, as frequency increases, the reflection from the vias and the loss of differential power become significant.

Introduction

The effect of signal transmission through vias can be significant as operating frequencies on printed circuit board (PCB) increase into GHz range. Differential signaling is often employed in the high frequency range. However, use of vias in differential lines may lead to degradation of the differential signal due to reflection from the vias and excitation of power bus noise, etc. FDTD has been successfully applied to via investigations [1-4]. Most studies considered vias in single-ended signaling configurations. Via holes in differential line were modeled in [5] as a cascade of capacitances and inductances using a boundary integral equation technique to calculate the capacitance. In this work, the FDTD method was applied to investigate the behavior of vias in differential signaling.

Numerical Approach

The FDTD method was employed to model vias in differential transmission line. Figure 1 shows a 4-layer board geometry. Layers 2 and 3 are reference planes, and layers 1 and 4 are signal planes. A pair of microstrip lines was routed on layers 1 and 4. Each microstrip line was 12 mils wide and was 7 mils above its reference plane. The dielectric constant of the substrate was 4.3. Dielectric losses were not considered. The spacing between the two lines from edge to edge was 12 mils. The odd and even mode characteristic impedances calculated using Ansoft XFX were $Z_{\infty} = 49 \Omega$ and $Z_{\infty} = 54 \Omega$, respectively. The lines on layer 1 were excited by two sinusoidally modulated Gaussian voltage sources, V_{s1} and V_{s2} . V_{s1} and V_{s2} were equal in magnitude but out of phase, such that the pair of microstrip lines was excited in the differential mode. A 50 Ω resistance was incorporated in each voltage source in order to match the approximately 100Ω differential impedance. The differential lines were routed 960 mils on layer 1, then, they were transited to layer 4 by two vias. In a real board, vias are usually round, however, vias were approximated as square for FDTD modeling convenience. Each via pad had a dimension of 24 mils × 24 mils and each via hole 12 mils × 12 mils. The via pads on the reference planes were also considered in the modeling. After the via transition, the differential lines were routed another 960 mils on layer 4, then were terminated by a π network. The π -network load was designed to match both differential- and common-mode impedances. Voltages and currents were recorded at locations 0, 1 and 2, as shown in Figure 1. Uniform rectangular cells with size $\Delta x = 3$ mils, $\Delta y = 3$ mils and $\Delta z = 1.75$ mils were applied in the FDTD modeling.

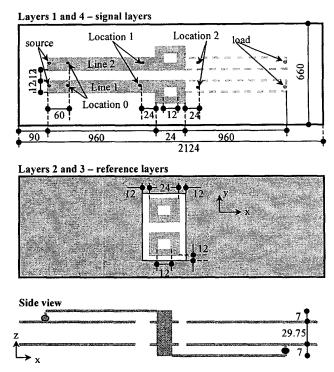


Figure 1. Modeling geometry. Unit: mils

Modeling Results

Figure 2 shows the differential waveforms at locations 0, 1 and 2. The differential voltage is defined as $v_{im}(x) \equiv v_1(x) - v_2(x)$,

where $v_1(x)$ and $v_2(x)$ are the voltages on lines 1 and 2 respectively. The distance between location 0 and location 1 is $d_{01} = 876$ mils. It took approximately 129.7 ps for the dip at location 0 to propagate to location 1. Therefore, the wave propagation speed is approximately $v_{line} = 1.716 \times 10^8$ m/s. The straight distance between locations 1 and 2 is 72 mils and the vertical length of the vias is 43.75 mils. Therefore, the total length that the differential signal propagated from location 1 to 2 is 115.75 mils. From Figure 2, the corresponding time is approximately 20.5 ps. Thus, the velocity that the wave propagating through the vias area is approximately $v_{via} = 1.43 \times 10^8$ m/s. Comparing v_{line} and v_{via} indicates that waves propagate slower in the via area than in the microstrip traces. In other words, extra delay was introduced by vias in this configuration. The possible explanation for the delay is the fact that the vias were embedded in the dielectric medium while the traces were not. The velocity for a transmission line in the substrate is $v_p = 1/\sqrt{\mu_0 \varepsilon_0 \varepsilon_r} = 1.45 \times 10^8 \, m/s$. The calculated v_{via} is close to v_p , therefore, the delay introduced by the vias may be modeled as a lossless transmission line which is embedded in the dielectric. The estimation of velocities presented here neglects the dispersion of microstrip lines. Further, wave shapes may vary a bit due to transmission and reflections, so using the voltage dips, shown in Figure 2, as reference points may introduce errors. Nevertheless, the simple estimation demonstrates that a long via may impose unexpected time delay to signal transmission that may have adverse impact to time critical circuit designs.

Differential S-parameters are calculated in order to investigate the frequency response of the differential vias. The line length in the model was designed sufficiently long that a pure right-going-wave (RGW)

could be recorded in early time history at location 0 before the wave was reflected back. Then, the differential impedance Z_{dm} is the ratio of the RGW differential voltage and current.

$$Z_{dm} = \frac{v_{dm}^{RGW}(x)}{i_{dm}^{RGW}(x)}\bigg|_{x=location0},$$

where $v_{dm}^{RGW}(x) = v_1(x) - v_2(x)$, $i_{dm}^{RGW}(x) = \frac{1}{2}[i_1(x) - i_2(x)]$ and $v_1(x)$, $v_2(x)$, $i_1(x)$ and $i_2(x)$

are the voltages and currents on lines 1 and 2. The differential normalized waves at location 1 become [6]

$$a_{dm1} \equiv \frac{1}{2\sqrt{\text{Re}(Z_{dm})}} [v_{dm}(x) + i_{dm}(x)Z_{dm}] \Big|_{x = loaction1}$$

$$b_{dm1} \equiv \frac{1}{2\sqrt{\text{Re}(Z_{dm})}} [v_{dm}(x) - i_{dm}(x)Z^*_{dm}] \Big|_{x = location1}.$$

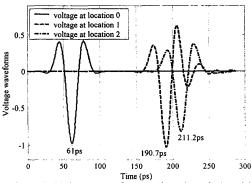


Figure 2. Voltage waveforms at locations 0, 1 and 2.

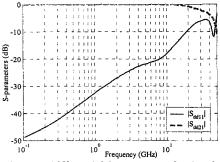


Figure 3. Differential S-parameters for the vias.

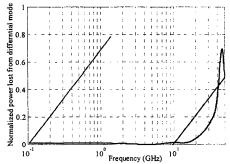


Figure 4. The power lost from differential-mode.

An analogous definition is applied at location 2. The differential S-parameters, S_{dd11} and S_{dd21} can be calculated by

$$S_{dd11} = \frac{b_{dm1}}{a_{dm1}} \bigg|_{a_{dm}, =0, a_{cm1}=0, a_{cm}, =0}$$

$$S_{dd21} = \frac{b_{dm2}}{a_{dm1}} \bigg|_{a_{dm2} = 0, a_{cm1} = 0, a_{cm2} = 0},$$

where a_{cm1} and a_{cm2} are the incident common-mode waves. Figure 3 shows the differential S-parameters with the solid line as $|S_{ddI}|$ and the dashed line as $|S_{ddI}|$. As frequency increases, the reflection from the vias increases and the transmission decreases. Therefore, in general, as frequency increases, the impact of the viás also increases. However, at frequencies below 10 GHz, $|S_{ddII}|$ is below -20~dB and $|S_{dd2I}|$ is almost zero, indicating the differential signals below 10 GHz can propagate through the vias without much distortion and reflection. However, when the critical harmonics of a digital signal have frequencies higher than 10 GHz, the rise time, or eye, will be degraded through the vias, and bit-error-rate (BER) of the link could be affected. If the fundamental frequency of a digital signal exceeds 10 GHz, the magnitude of the signal will decrease due to the transmission loss of the vias, which could become a signal integrity issue.

The total lost differential power can be calculated by

$$P_{dmlost} = 1 - \left| S_{dd11} \right|^2 - \left| S_{dd21} \right|^2.$$

 $P_{dmlost} = 1 - \left|S_{dd11}\right|^2 - \left|S_{dd21}\right|^2.$ Figure 4 shows the total lost differential power as a function of frequency. In general, with the increase of frequency, the lost differential power also increases. However, in the frequency range below 10 GHz, the power lost is very small, again indicating that most differential energy can propagate through the vias smoothly.

Conclusion

FDTD was used to analyze the effect of vias on differential signaling. The velocity of the signal propagating through the via area was estimated. It was lower than the velocity of the signal propagating on the differential microstrip lines, indicating the vias introduces additional delay to the signal propagation. Differential S-parameters were calculated in frequency range up to 50 GHz and the differential power lost due to via transition was also calculated as a function of frequency. In general, the vias degrade the signal integrity as frequency increases. At frequencies below 10 GHz, the impact of the vias is not significant for this particular differential signaling geometry. When frequencies exceed 10 GHz, signal integrity becomes an issue.

References

- [1] S. Maeda, T. Kashiwa and I. Fukai, "Full wave analysis of propagation characteristics of a throughhole using the finite-difference time-domain method", IEEE Transactions on Microwave Theory and Techniques, vol. 39, No. 12, December 1991.
- [2] W. Becker, P. Harms and R. Mittra, "Time-domain electromagnetic analysis of interconnects in a computer ship package", IEEE Transactions on Microwave Theory and Techniques, vol. 40, No. 12, December 1992.
- [3] E. Pillai and W. Wiesbeck, "Derivation of equivalent circuits for multiplayer printed circuit board discontinuities using full wave models", IEEE Transactions on Microwave Theory and Techniques, vol. 42, No. 9, September 1994.
- [4] P. C. Cherry and M. F. Iskander, "FDTD analysis of high frequency electronic interconnection effects", IEEE Transactions on Microwave Theory and Techniques, vol. 43, No. 10, October 1995.
- [5] E. Laermans, and J. De Geest et al, "Modeling differential via holes", IEEE Conference on Electrical Performance of Electronic Packaging, 2000.
- [6] D. E. Bockelman and W. R. Eisenstadt, "Combined differential and common-mode scattering parameters: theory and simulation", IEEE Transaction on Microwave Theory and Techniques, vol. 43, No. 7, July 1995.