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Dynamic Average-Value Modeling of a Four-Level Drive System

Keith Corzine, *Member, IEEE*, Xiaomin Kou, *Student Member, IEEE*, and James R. Baker

Abstract—Multilevel power converters have gained much attention in recent years due to their high power quality, low switching losses, and high-voltage capability. These advantages make the multilevel converter a candidate for the next generation of Naval ship propulsion systems. Evaluation of these systems is typically assisted with a dynamic average-value models in order to rapidly predict system performance under several operating scenarios. In this paper, an average-value model is developed for the four-level diode-clamped converter which takes into account the active capacitor voltage balancing control. This model performance prediction is compared to a detailed model and laboratory measurements on an 18 kW rectifier/inverter test system.

Index Terms—Average-value modeling, four-level converters, multilevel converters.

I. INTRODUCTION

THE general trend in power electronics has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. However, the increase in switching frequency increases the switching losses which become significant at high power levels. Several methods for decreasing switching losses, and the same time improving power quality, have been proposed including constructing resonant converters and multilevel converters [1].

Resonant converters avoid switching losses by adding an LC resonant circuit to the hard switched inverter topology. The inverter transistors can be switched when their voltage or current is zero, thus mitigating switching losses. Examples of this type of converter include the resonant dc link [2], and the auxiliary resonant commutated pole inverter (ARCP) [3], [4]. One disadvantage of resonant inverters is that the added resonant circuitry will increase the complexity and cost of the converter control. Furthermore, high IGBT switching edge rates can create switch level control problems.

Multilevel converters offer another approach to providing high power quality. In particular, these converters offer a high number of switching states so that the output voltage can be “stepped” in smaller increments [5]–[11]. This allows mitigation of harmonics at a low switching frequencies thereby reducing switching losses. In addition, EMC concerns are

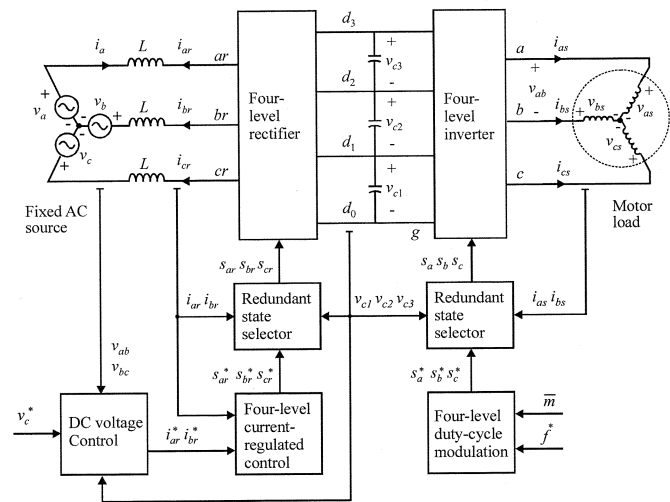


Fig. 1. Four-level rectifier/inverter system and associated control.

reduced through the lower common mode current facilitated by lower dv/dt 's produced by the smaller voltage steps. One disadvantage of these techniques is that they require a high number of switching devices. Although the devices are rated at a lower voltage, gate drive and control circuitry must still be provided. The primary disadvantage of multilevel inverters is that they must be supplied from isolated dc voltage sources or a bank of series capacitors with balanced voltages. In systems where isolated dc sources are not practical, capacitor voltage balancing becomes the principal limitation for multilevel converters.

In this paper, an average-value model is developed for the four-level converter. The challenge in developing the model is the inclusion of redundant switching state selection; a method of switching used to assist in capacitor voltage balancing. This model is then used to analyze a four-level rectifier/inverter system. Detailed model and laboratory comparison are included.

II. FOUR-LEVEL DRIVE SYSTEM DESCRIPTION

Fig. 1 shows the four-level rectifier/inverter system described herein. The fixed frequency ac source may represent a utility grid or a synchronous generator on a Naval ship power system. The four-level rectifier and associated control ensures that the capacitor dc voltages v_{c1} , v_{c2} , and v_{c3} are identical. With these voltages balanced, the four-level inverter and associated control can properly supply the induction motor with high power quality waveforms. The induction motor is a standard NEMA type B industrial design having a well-established model [12].

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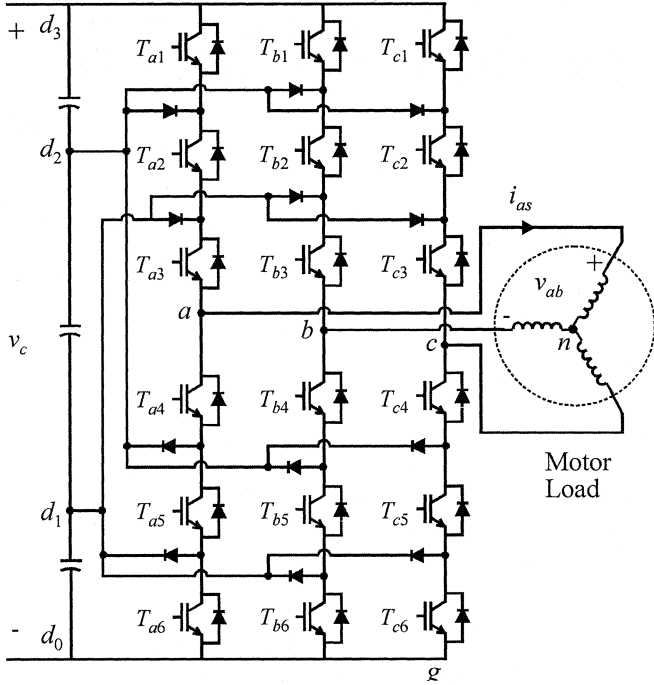


Fig. 2. Four-level inverter topology.

A. Four-Level Converter

Herein, the term converter will be used to describe any power electronic conversion device. Specific terms such as rectifier or inverter are used to specify a particular converter. Fig. 2 shows the topological detail of the four-level inverter. Despite the high number of switching devices, the power converter operation is fairly straightforward. Each phase of the inverter or rectifier can be connected to the points d_0 , d_1 , d_2 , or d_3 through suitable switching of the converter transistors [5]–[11]. The resulting operation is similar to that of a positional switch as shown in Fig. 3 for the inverter a -phase. The inverter line-to-ground voltage for a particular phase is determined from the switching state and capacitor voltages by

$$v_{xg} = \sum_{i=0}^{s_x} v_{ci} \quad (1)$$

where x represents phase and may be a , b , or c . The switching state s_x in (1) is determined by the pulse width modulation (PWM) control and has the values 0, 1, 2, or 3 for the four-level inverter. Since the induction motor is wye connected, it can be shown that the motor voltages are related to the inverter line-to-ground voltages by [12]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \quad (2)$$

The four-level rectifier structure is identical to that of the four-level inverter. As with the inverter, the phases ar , br , and cr , may be connected to any of the capacitor junctions d_0 , d_1 , d_2 , or d_3 resulting in similar phase-to-ground voltages of

$$v_{xrg} = \sum_{i=0}^{s_{xr}} v_{ci} \quad (3)$$

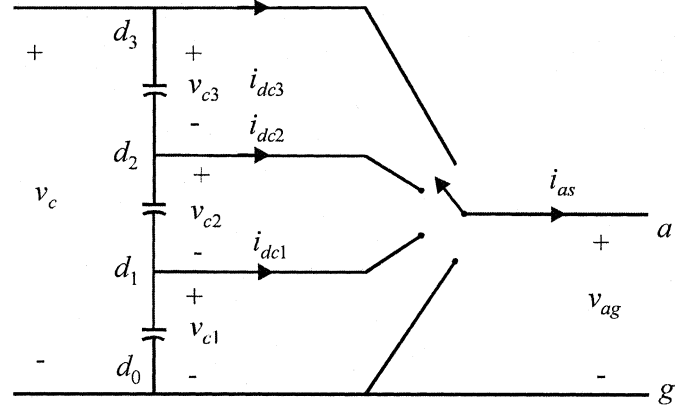


Fig. 3. Four-level inverter a-phase equivalent switching.

where s_{xr} represents the rectifier phase x switching state. The ac supply voltages are then calculated from

$$\begin{bmatrix} v_{ar} \\ v_{br} \\ v_{cr} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{arg} \\ v_{brg} \\ v_{crg} \end{bmatrix}. \quad (4)$$

Voltages in (4) are defined from the rectifier phases to the neutral connection of the source.

B. Duty-Cycle Modulation

The goal of duty-cycle modulation is to regulate the inverter switching states s_x so that the desired motor voltages v_{as} , v_{bs} , and v_{cs} are obtained. The desired motor phase voltages may be expressed as

$$v_{as}^* = \sqrt{2}v_s^* \cos(\theta_c) \quad (5)$$

$$v_{bs}^* = \sqrt{2}v_s^* \cos\left(\theta_c - \frac{2\pi}{3}\right) \quad (6)$$

$$v_{cs}^* = \sqrt{2}v_s^* \cos\left(\theta_c + \frac{2\pi}{3}\right) \quad (7)$$

where v_s^* is the desired RMS voltage magnitude and θ_c is the desired electrical angle including phase shift which may be expressed

$$\theta_c = \theta_c + \phi_v. \quad (8)$$

The electrical angle can be related to a desired electrical frequency f^* by

$$\theta_e = 2\pi \int_0^t f^* d\tau. \quad (9)$$

After considering the third harmonic injection, the PWM switching is typically accomplished by defining duty-cycles based on the normalized commanded line-to-ground voltages [13], which may be expressed as

$$d_a = \frac{1}{2} \left[1 + m \cos(\theta_c) - \frac{m}{6} \cos(3\theta_c) \right] \quad (10)$$

$$d_b = \frac{1}{2} \left[1 + m \cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6} \cos(3\theta_c) \right] \quad (11)$$

$$d_c = \frac{1}{2} \left[1 + m \cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6} \cos(3\theta_c) \right] \quad (12)$$

where m represents the modulation index, which is defined by

$$m = \frac{2\sqrt{2}v_s^*}{v_c}. \quad (13)$$

The variable m has a range from 0 to $2/\sqrt{3}$. It is often convenient to define a modulation index that has a range from 0 to 100% by

$$\bar{m} = \frac{\sqrt{3}}{2}m. \quad (14)$$

The inverter switching states s_x may be determined by comparing the duty-cycles to multiple triangle waveforms [9], [11], the frequency of which is $1/T_s$. For example, Fig. 4 demonstrates the generation of the switching states s_x by using sine-sawtooth modulation. Alternatively, some drive systems utilize a digital signal processor (DSP) implementation [13] in which definition of the triangle waveforms is not necessary. As an example, consider the a -phase switching state. The first step is to integerize the duty cycle to determine the nearest switching states

$$l_a = \text{INT}(3d_a) \quad (15)$$

where INT is the integerization function which returns the nearest integer less than or equal to its argument. The nearest switching states are then $s_a = l_a$ and $s_a = l_a + 1$. If the clock frequency of the DSP controller is $1/T_s$, then the a -phase switching states for one DSP cycle T_s are

$$s_a = \begin{cases} l_a + 1, & 0 \leq t < t_a \\ l_a, & t_a \leq t \leq T_s \end{cases} \quad (16)$$

where

$$t_a = (3d_a - l_a)T_s. \quad (17)$$

The b -phase and c -phase switching states are computed in a similar manner. Typically, the switching frequency is set to roughly 100 times the fundamental electrical frequency ($1/T_s \geq 100f^*$).

C. Hysteresis Current-Regulator

The multilevel hysteresis current-regulator is based on defining a set of $n - 1$ hysteresis levels; n being the number of converter voltage levels. Denoting the maximum allowable excursion of the actual current from the desired current as i_h , then $n - 1$ evenly distributed hysteresis levels are computed from

$$h_j = \frac{j}{n-1}i_h \quad j = 1, 2, \dots, (n-1). \quad (18)$$

The current error for phase x is defined by

$$i_{xerr} = i_{xr}^* - i_{xr}. \quad (19)$$

When the current error is positive, the controller decreases the level of phase x by one each time the error crosses a hysteresis level. Likewise, the phase level is increased when the current error is negative and crosses a hysteresis level. For the four-level rectifier, $n = 4$ and thus three hysteresis levels are defined. Fig. 5 presents a hysteresis current control example for the four-level rectifier, where i_{ar}^* and i_{ar} denote the a -phase reference current and a -phase actual current, respectively. The

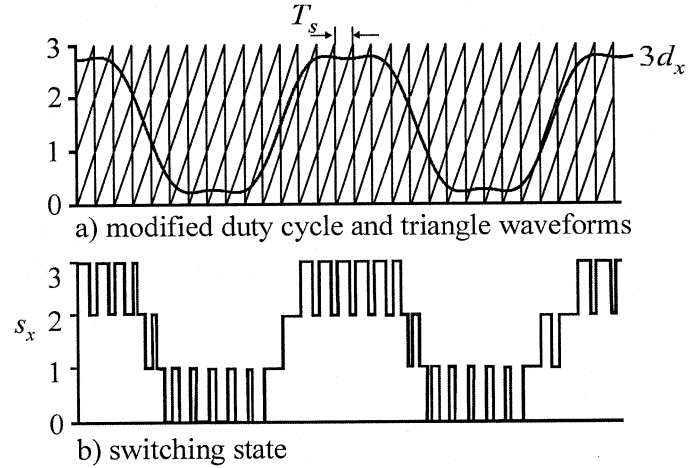


Fig. 4. Four-level sine-triangle modulation technique.

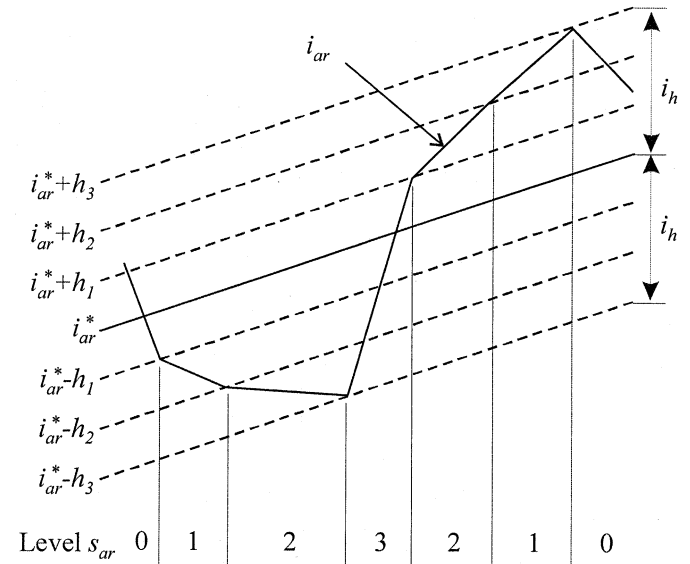


Fig. 5. Four-level current-regulated control switching.

a -phase voltage levels are also shown to illustrate the converter switching. As can be seen, the primary goal of the rectifier switching is to regulate the current. Interested reader may refer to [7] for more detail information about hysteresis current control. Capacitor voltage balance is achieved through redundant state selection described in the following section.

D. Redundant State Selector

In order for the four-level power conversion processes (rectifier and inverter) to operate properly, the voltages on all three capacitors must be equal. However, current drawn from the junctions d_1 and d_2 as shown in Fig. 3 will tend to unbalance the capacitor voltages. Assuming that the capacitor voltage error is small, redundant switching states can be used which result in the same AC load voltages but have different effect on the charging and discharging of the capacitors [10], [11]. For the four-level inverter, the problem may be reduced to four cases defined by the number of capacitors that the phases are connected across [10]. Fig. 6 shows examples of the four

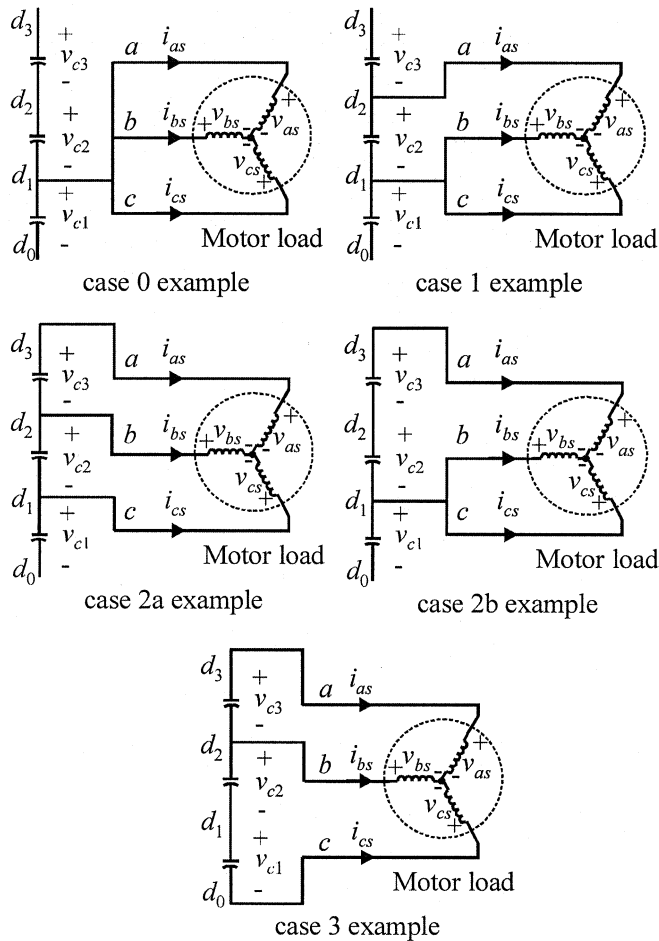


Fig. 6. Redundant state selection examples.

cases. The redundant switching states of these cases may be found by incrementing or decrementing the switching states of all three phases. For example, case 0 is obtained by setting $(s_a = 1, s_b = 1, s_c = 1)$. The induction motor voltages will be the same if the redundant states $(s_a = 0, s_b = 0, s_c = 0)$ or $(s_a = 2, s_b = 2, s_c = 2)$ or $(s_a = 3, s_b = 3, s_c = 3)$ are used. However, for case 0, the redundant states do not change the currents drawn from the capacitor junctions. Therefore, redundant state selection is not applied to case 0. From Fig. 6, it can be seen that the switching state $(s_a = 2, s_b = 1, s_c = 1)$ will charge or discharge capacitor voltage v_{c2} depending on the direction of the a -phase current. This is an example of case 1 where the phases are connected across one capacitor. If the a -phase current is positive the phases will tend to discharge the capacitor and the phases should be connected across the capacitor with the highest voltage by selecting between the appropriate redundant states which in this example are $(s_a = 1, s_b = 0, s_c = 0)$ and $(s_a = 3, s_b = 2, s_c = 2)$. If the a -phase current is negative, the phases should be connected across the capacitor with the lowest voltage. There are two ways in which the phases may span two capacitors. These are shown in Fig. 6 as case 2a and case 2b. As can be seen, case 2a has the potential to change the voltages on any capacitor. A decision about the most appropriate redundant state for this case should be based on the primary goal of controlling the voltage v_{c2}

and a secondary goal of controlling the voltages v_{c1} and v_{c3} . The purpose of these goals is that the connection of the motor phases to the capacitor junctions will tend to discharge the center capacitor when commanding high load voltage [10], [11]. From the example shown in Fig. 6, it can be seen that the c -phase current direction will determine the center capacitor charge or discharge for the state shown ($s_a = 3, s_b = 2, s_c = 1$). For the redundant state ($s_a = 2, s_b = 1, s_c = 0$), the a -phase current will depict the capacitor charge or discharge. In the event that neither state improves the center capacitor voltage balance, the decision is made based on capacitor voltages v_{c1} and v_{c3} . Case 2b in Fig. 6 will not assist in controlling the center capacitor voltage since the state shown ($s_a = 3, s_b = 1, s_c = 1$) and the redundant state ($s_a = 2, s_b = 0, s_c = 0$) have the same charging or discharging effect on v_{c2} . In this case, the redundant state could be used to balance the capacitor voltages v_{c1} and v_{c3} . However, this imbalance is typically not a difficulty and redundant state selection in this case will only increase the switching frequency [10]. There are no redundant states that correspond to case 3 and therefore redundant state selection is not applied.

All cases discussed above can be analyzed off-line and programmed as a table into an EPROM or EPLD. Based on the direction of the desired switching state (s_a^*, s_b^*, s_c^*), the phase currents and capacitor voltages, the memory or logic device will select the appropriate state [10]. The redundant state selector for the four-level rectifier is identical to that of the inverter.

E. DC Link Voltage Control

The overall dc link voltage v_c is regulated through standard synchronous current regulation [14]. The source voltages may be described by

$$v_a = \sqrt{\frac{2}{3}} V_{LL} \cos(\theta_u) \quad (20)$$

$$v_b = \sqrt{\frac{2}{3}} V_{LL} \cos\left(\theta_u - \frac{2\pi}{3}\right) \quad (21)$$

$$v_c = \sqrt{\frac{2}{3}} V_{LL} \cos\left(\theta_u + \frac{2\pi}{3}\right) \quad (22)$$

whereupon transformation to the synchronous reference frame yields a q -axis voltage equal to the peak phase voltage and a d -axis voltage equal to zero [12]. For unity power factor operation, it is necessary to command the d -axis rectifier current to zero. The q -axis current can be used to regulate the dc link voltage resulting in commanded currents of

$$i_{dr}^{u*} = -K_p e_v - K_i \int_0^t e_v d\tau \quad (23)$$

$$i_{dr}^{u*} = 0 \quad (24)$$

where e_v is the dc voltage error defined by

$$e_v = v_c^* - v_c. \quad (25)$$

The inverse transformation necessary to determine i_{ar}^* , i_{br}^* , and i_{cr}^* relies on knowledge of the input electrical position θ_u . Methods for aligning the transformation to this reference

frame include using a phase locked loop, voltage sensors, or an on-line observer. For this system, the voltage sensor method was used. These sensors have the advantage of straightforward and accurate implementation and relatively low-cost. Helpful transformation terms may be directly computed from the measured voltages as

$$\cos\left(\theta_u + \frac{\pi}{6}\right) = \frac{v_{ab}}{\sqrt{2}V_{LL}} \quad (26)$$

$$\cos\left(\theta_u - \frac{\pi}{2}\right) = \frac{v_{bc}}{\sqrt{2}V_{LL}}. \quad (27)$$

All necessary transformation terms can be determined from these terms using trigonometric identities [12]. Furthermore, V_{LL} can be found by

$$V_{LL} = \frac{\sqrt{6}}{3} \sqrt{v_{ab}^2 + v_{bc}^2 + v_{ab}v_{bc}}. \quad (28)$$

Harmonics in the line voltages will appear in the sensor outputs, but may be eliminated using a low-pass filter. Compensation for the filter amplitude attenuation and phase delay can be incorporated in the control software since the source voltage magnitude and frequency are known.

III. FOUR-LEVEL CONVERTER AVERAGE-VALUE MODEL

Although detailed modeling of power electronic systems provides information about semiconductor switching, dynamic average-value models are typically better suited for predicting the salient features of system performance. This is especially true for large systems, such as Naval ship propulsion systems, involving many components and machines with long time constants. By representing the converter switching on an average-value basis, the simulation times can be greatly reduced allowing a system designer to consider several operating scenarios.

The average-value model development for the four-level converter is based on computing line-to-ground voltages and capacitor junction currents which represent the average-value of these quantities over one switching cycle of the PWM controller. Fig. 7 shows the structure of the average-value model for the four-level inverter. Therein, the $\hat{}$ symbol is used to denote average-value over one switching cycle. Determining the average-value quantities involves considering the switching states over one DSP cycle including the redundant state selector. This is done at each time step in the simulation by considering one cycle of the DSP switching. Fig. 8 shows an example of the switching with possible redundant states. The ideal switching states s_a^* , s_b^* , and s_c^* are determined by the DSP controller using (10)–(15). As can be seen, each phase transition defines an interval in which the inverter is in a particular switching state. The redundant switching states are determined using the commanded switching state, the load currents, and the capacitor voltages using the redundant state selection table described above. The average value of the x^{th} phase line-to-ground voltage is then computed as

$$\hat{v}_{xg} = \frac{1}{T_s} \sum_{k=1}^4 t_k v_{xgk} \quad (29)$$

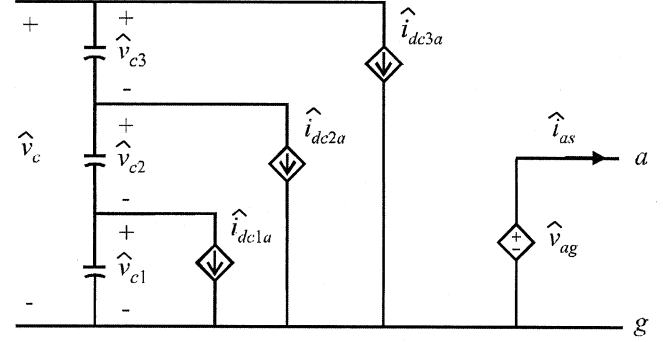


Fig. 7. Four-level inverter a-phase average-value model.

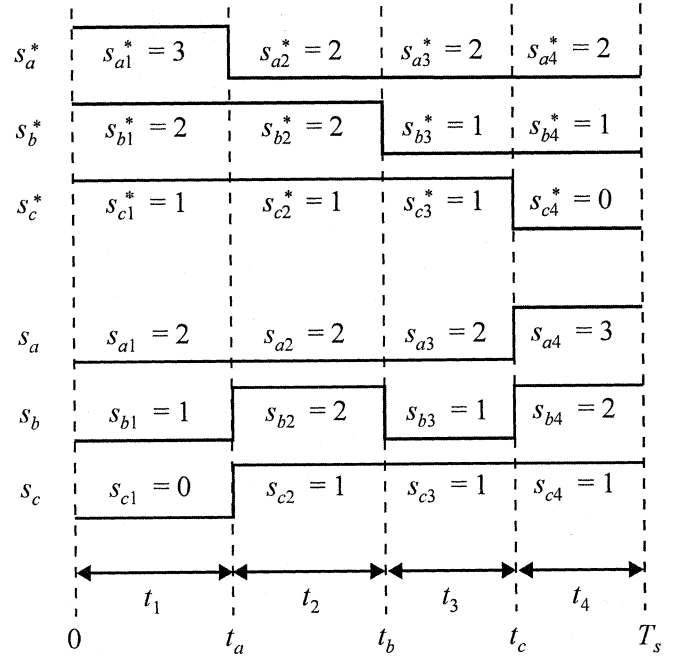


Fig. 8. Example inverter switching and redundant states.

where t_k denotes the specific interval time as defined in Fig. 8 and v_{xgk} is determined from (1) with $s_x = s_{xk}$. From (16), it can be seen that this computation is independent of PWM controller switching frequency. The average-value capacitor junction currents are determined by a contribution from each phase as

$$\hat{i}_{dcj} = \frac{1}{T_s} \sum_{k=1}^4 t_k i_{xsk} \delta_{(s_{xk}-j)}. \quad (30)$$

In (30), j represents capacitor junction and may be 1, 2, or 3 and δ is the delta function which is equal to 1 if $s_{xk} = j$ and 0 otherwise. The total current in junction j is then

$$\hat{i}_{dcj} = \hat{i}_{dcja} + \hat{i}_{dcjb} + \hat{i}_{dcjc}. \quad (31)$$

Although the average-value model described herein has been developed for a voltage-source PWM control, it can be used to model the current-regulated four-level rectifier by determining the source voltage required in order to obtain the commanded

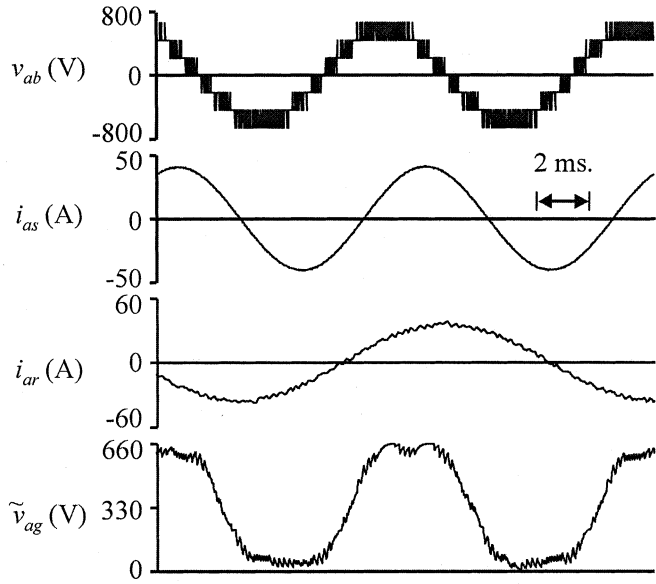


Fig. 9. Four-level system detailed simulation.

currents. From the q - and d -axis model of the voltage source in the electric utility reference frame

$$v_{qr}^{u*} = v_q^u + \omega_u L i_{dr}^{u*} \quad (32)$$

$$v_{dr}^{u*} = v_d^u - \omega_u L i_{qr}^{u*} \quad (33)$$

where ω_u is the ac source radian frequency and v_q^u and v_d^u are

$$v_q^u = \sqrt{\frac{2}{3}} V_{LL} \quad (34)$$

$$v_d^u = 0 \quad (35)$$

from the synchronous reference frame transformation. It should be noted that (32)–(35) neglect the source dynamics which is a good approximation considering the source electrical time constant compared to the system dynamics. The effective modulation index and phase shift for the rectifier are then computed from

$$m_r = \frac{2}{v_c} \sqrt{(v_{qr}^{u*})^2 + (v_{dr}^{u*})^2} \quad (36)$$

$$\phi_{vr} = \tan^{-1} \left(\frac{-v_{dr}^{u*}}{v_{qr}^{u*}} \right). \quad (37)$$

Using the phase shift, modulation index, and θ_u , as defined in (20)–(22), a set of duty cycles can be defined for the rectifier similar to (10)–(12), which allow the average-value mode presented herein to be used for the four-level rectifier (see Fig. 9).

IV. SIMULATION AND LABORATORY RESULTS

A. Steady-State Study

An 18 kW laboratory test system with the structure shown in Fig. 1 has been constructed for model validation. The input is a 60 Hz source with $V_{LL} = 450$ V and $L = 2.7$ mH. The rectifier control PI gains are set to $K_p = 0.1$ A/V and $K_i =$

TABLE I
INDUCTION MACHINE PARAMETERS

$P = 4$	$M = 55$ mH
$r_s = 0.2 \Omega$	$L_{ls} = 1.91$ mH
$r_r' = 0.326 \Omega$	$L_{lr}' = 2.32$ mH

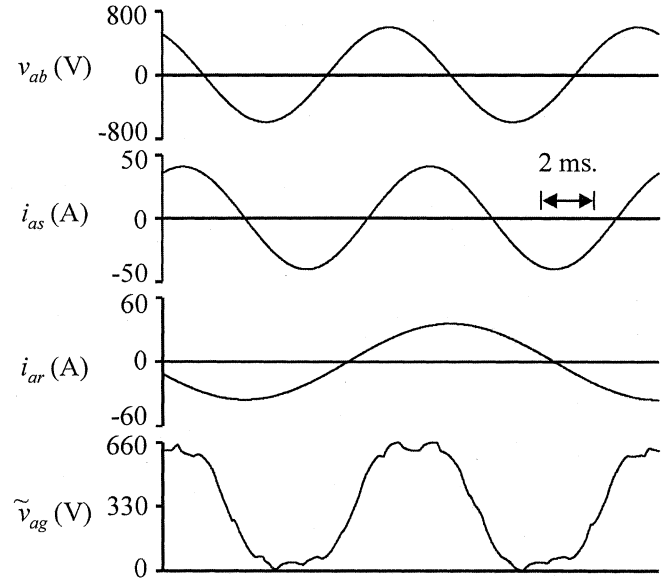


Fig. 10. Four-level system average-value model simulation.

5 A/V · s in order to regulate the dc link voltage to $v_c^* = 660$ V. The hysteresis level has been set to $i_h = 1$ A. The induction motor parameters are shown in Table I. For the steady-state study that follows, the induction motor is mechanically loaded using a synchronous generator so that it operates at a speed of $\omega_{rm} = 301.6$ rad/s. The inverter modulation control parameters have been set to $\bar{m} = 0.9$ and $f^* = 100$ Hz in order to demonstrate frequency changing operation at 90% voltage utilization. Figs. 10, 11, and 12 show the four-level system performance as predicted by a detailed simulation, and average-value simulation, and as measured in the laboratory respectively. Therein, the inverter line-to-line voltage v_{ab} , the motor a-phase current i_{as} , the rectifier a-phase current i_{ar} , and the inverter line-to-ground voltage v_{ag} are shown. Capacitor voltage balance is ensured at this operating point as noted by the even voltage steps in the motor line-to-line voltage. The line-to-ground voltage has been filtered so that a suitable comparison can be made between the two models. As can be seen, the average-value model can predict the steady state operation features of the four-level inverter system. In this study, the average-value model prediction was 48 times faster than the detailed model. However, it should be pointed out that a large gain in simulation speed came from eliminating the event-driven calculations of the hysteresis control. Simulation studies of the inverter and voltage-source modulation alone demonstrated that the average-value model predicted identical performance to the detailed model at a speed of four times faster.

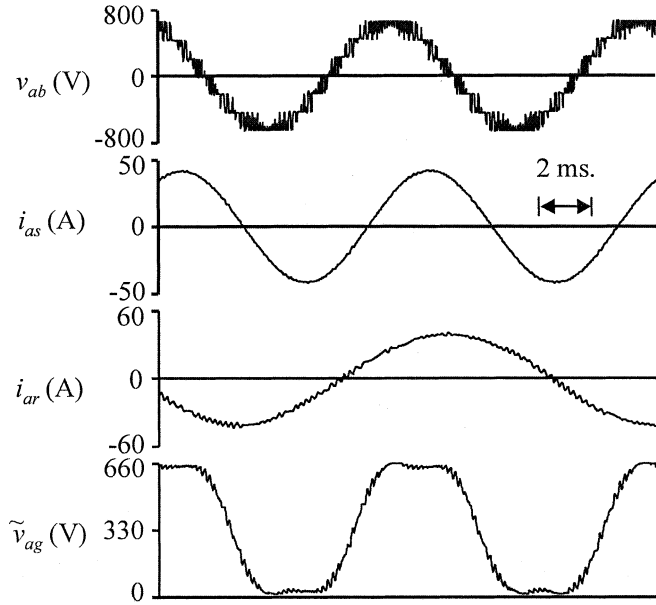


Fig. 11. Four-level system laboratory measurements.

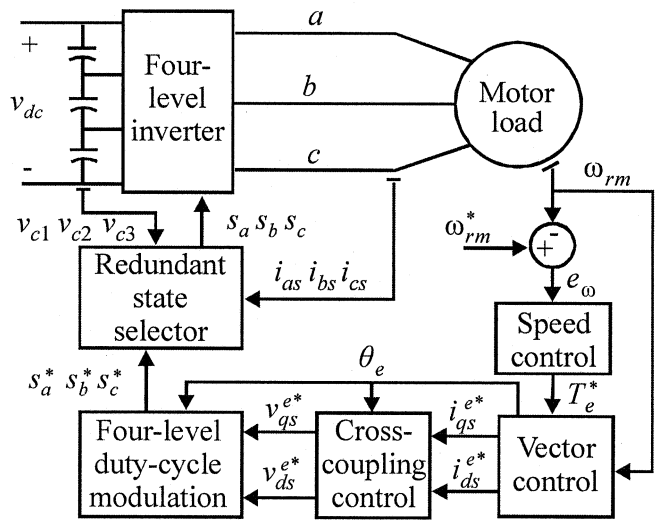


Fig. 12. Four-level inverter transient state simulator.

B. Four-level Inverter Transient Study

A computer simulation has been created following the structure shown in Fig. 11. In this study, a four-level inverter is directly powered by a fixed dc voltage source with $v_{dc} = 700$ V. The speed control is a standard PI control with the control law

$$T_e^* = K_{pt}e_\omega - K_{it} \int_0^t e_\omega d\tau \quad (38)$$

where $K_{pt} = 10 \text{ N}\cdot\text{m}\cdot\text{s}$, $K_{it} = 5 \text{ N}\cdot\text{m}$ and e_ω defined in Fig. 12. A vector control followed by a voltage decoupler [15] has been used in this simulation. Table II lists the parameters of a 3.7 kW motor used herein. At the beginning of this transient study, both the motor speed and load torque are zero. After the machine flux builds up, the motor is started by ramping the commanded speed to the motor's rated speed. After running for 3 s under no

TABLE II
INDUCTION MACHINE PARAMETERS

$P = 4$	$M = 64.43 \text{ mH}$	$J = 0.15 \text{ kg}\cdot\text{m}^2$
$r_s = 0.3996 \Omega$	$L_{ls} = 5.73 \text{ mH}$	$B_m = 0$
$r_r' = 0.2266 \Omega$	$L_{lr}' = 4.64 \text{ mH}$	

load condition, the load torque is stepped to $20 \text{ N}\cdot\text{m}$. After running under full-load condition for about 4 s, the motor speed is ramped down to zero without changing the load, and motor will work under block mode. Fig. 13 shows the simulation waveform of the electrical torque, a -phase stator current, modulation index and rotation speed. During this transient study, the redundant state selector maintained the inverter capacitor balance. It can be seen that the average-value model has nearly identical performance to that of the detailed model during these transients.

C. Power Factor Versus Modulation Index

The capacitor balancing situation strongly relates to the load condition. Let \bar{m}_{\max} denote the maximum possible modulation index for maintaining balanced capacitor voltages, and Z denotes the load impedance. Roughly speaking, with the same magnitude of Z , the higher the load power factor is, the lower the \bar{m}_{\max} can be. Fig. 14 shows \bar{m}_{\max} vs. power factor simulation waveform acquired from the average-value model and the detailed model. In this simulation, a three-phase $R-L$ load is connected to a four-level inverter where the magnitude of Z per phase is maintained as 11.9Ω and the dc voltage is set to 660 V. As can be seen, the waveforms predicted by the average model matches with the one acquired from the detailed model very well. For a typical load with a 0.8 power factor, the detailed and average-value model predict a maximum modulation index of $\bar{m} = 0.5$. This same value has been noted by other researchers [10], [11] and was also validated on the laboratory system.

D. Capacitor Voltage Balancing Transient State Studies

It is informative to compare the capacitor balancing transient performance between the average-value model and the detailed model. To simulate such a transient state, a switch-controlled resistor branch can be shunted to the middle dc link capacitor of the four-level inverter shown in Fig. 2. When the switch is closed, the middle capacitor will tend to discharge through the resistor branch while the other two capacitors will be overcharged to maintain the total dc voltage. When reopening the switch, the capacitor voltages should recover to $v_{dc}/3$. Fig. 15 shows capacitor voltage waveforms of this transient study. In this study, v_{dc} was set to 660 V, \bar{m} was set to 0.5 and the resistance of the shunted branch was set to 0.5Ω . It can be seen that waveform predicted by the average-value model matches that of the detailed model.

From the above steady-state and transient-state studies, it can be seen that the average-value model predicts the salient features of the system performance but neglects the high-frequency transistor switching, which results in a much faster simulation speed

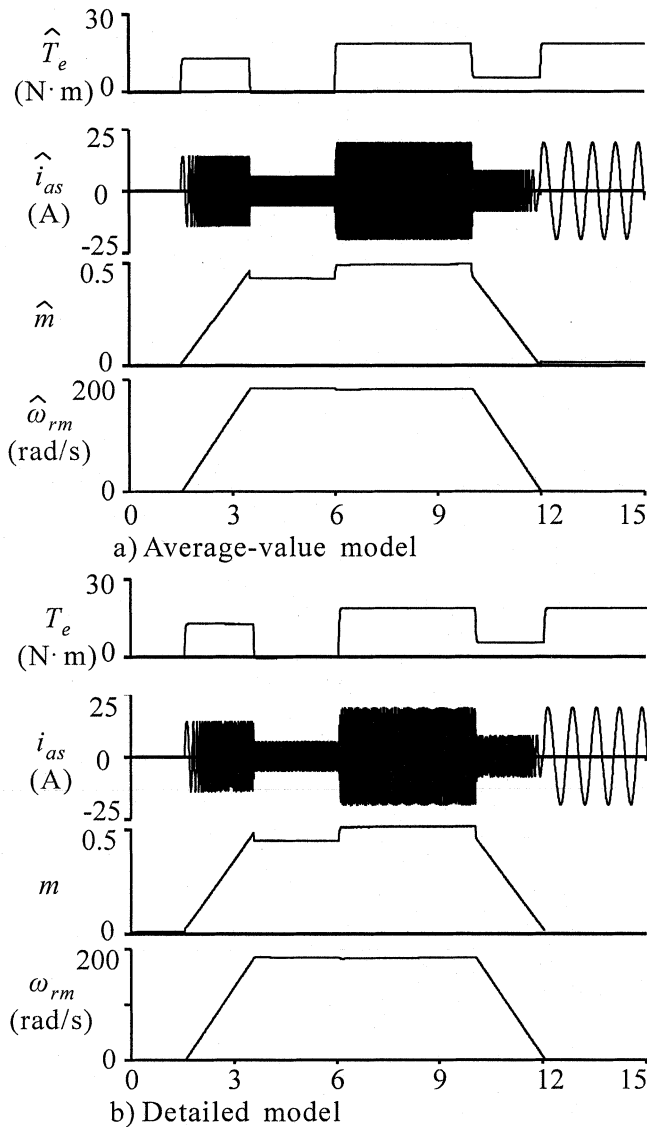


Fig. 13. Variable load and speed transient study.

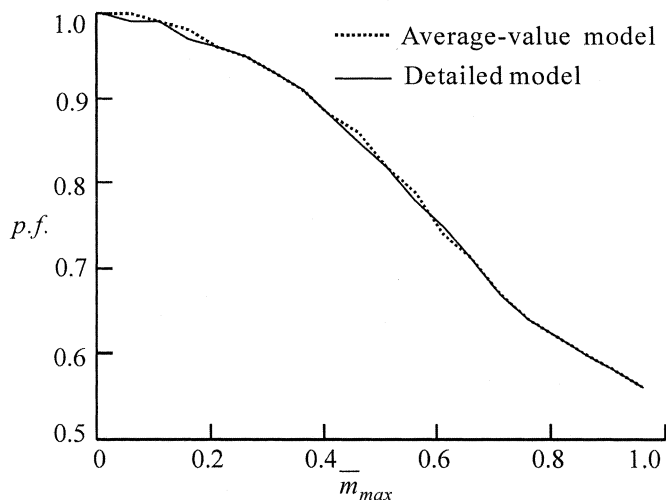


Fig. 14. Maximum modulation index versus power factor.

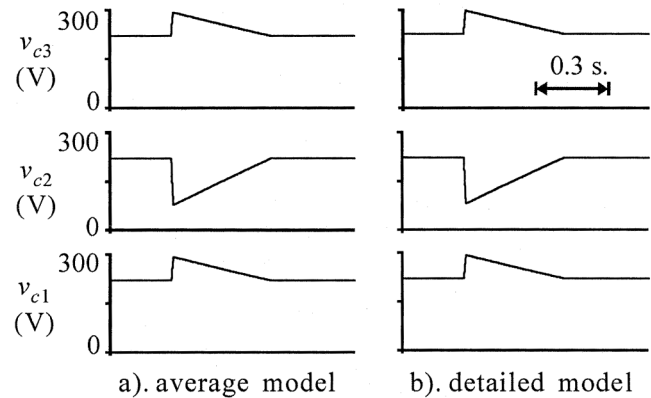


Fig. 15. Capacitor voltage transient study.

compared to the detailed simulation and is of particular meaning for the complex simulation systems. Thus the average-value model can be a practical tool for system design when considering several operating scenarios and selecting controller gains.

V. CONCLUSION

An average-value model for the popular four-level diode-clamped power electronic converter has been developed. The model performance prediction has been compared to a detailed simulation and laboratory measurements based on a four-level rectifier/inverter system. It was shown that the average-model rapidly and accurately predicted the steady-state and transient-state operation including the effect of the capacitor voltage balancing control. The average-model introduced herein may be used as a valuable tool for design of four-level converters; potentially including future Naval ship propulsion systems.

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REFERENCES

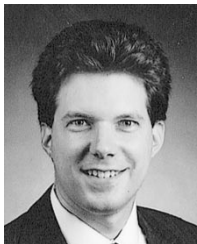
- [1] D. Divan, "Low stress switching for efficiency," *IEEE Spectrum*, vol. 33, no. 12, pp. 33–39, Dec. 1996.
- [2] J. He and N. Mohan, "Parallel resonant DC link circuit—a novel zero switching loss topology with minimum voltage stresses," *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 687–694, October 1991.
- [3] R. W. DeDoncker and J. P. Lyons, "The auxiliary resonant commutated pole converter," in *Proc. IEEE Ind. Applicat. Soc. Conf.*, vol. 2, Oct. 1990, pp. 1228–1335.
- [4] B. T. Kuhn and S. D. Sudhoff, "Modeling considerations in ARCP versus hard switched drives," in *Proc. Naval Symp. Electric Mach.*, July 1997, pp. 161–168.
- [5] A. Nabe, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Applicat.*, vol. 17, pp. 518–523, Sept./Oct. 1981.
- [6] K. A. Corzine, S. D. Sudhoff, and C. A. Whitcomb, "Performance characteristics of a cascaded two-level converter," *IEEE Trans. Energy Conv.*, vol. 14, pp. 433–439, Sept. 1999.
- [7] K. A. Corzine, "A hysteresis current-regulated control for multilevel converters," *IEEE Trans. Energy Conv.*, vol. 15, pp. 169–175, June 2000.
- [8] K. A. Corzine and S. D. Sudhoff, "High state count power converters: an alternate direction in power electronics technology," in *Proc. Soc. Automotive Eng. Aerosp. Power Syst. Conf.*, Williamsburg, VA, Apr. 1998, pp. 141–151.

- [9] K. A. Corzine, S. D. Sudhoff, E. A. Lewis, D. H. Schmucker, R. A. Youngs, and H. J. Hegner, "Use of multilevel converters in ship propulsion drives," in *Proc. All Electric Ship Conf.*, vol. 1, London, U.K., Sept. 1998, pp. 155–163.
- [10] M. Fracchia, T. Ghiara, M. Marchesoni, and M. Mazzucchelli, "Optimized modulation techniques for the generalized N-level converter," in *Proc. IEEE Power Electron. Spec. Conf.*, vol. 2, 1992, pp. 1205–1213.
- [11] G. Sinha and T. A. Lipo, "A four-level inverter based drive with a passive front end," *IEEE Trans. Power Electron.*, vol. 15, pp. 285–294, Mar. 2000.
- [12] P. C. Krause, O. Wasynczuk, and S. D. Sudhoff, *Analysis of Electric Machinery*. Piscataway, NJ: IEEE Press, 1995.
- [13] K. A. Corzine and J. R. Baker, "Multilevel voltage-source duty-cycle modulation: analysis and implementation," *IEEE Trans. Ind. Electron.*, vol. 49, pp. 1009–1016, Oct. 2002.
- [14] T. M. Rowan and R. J. Kirkman, "A new synchronous current regulator and an analysis of current-regulated PWM inverters," *IEEE Trans. Ind. Applicat.*, vol. 22, pp. 678–690, July/Aug. 1986.
- [15] D. W. Novotny and T. A. Lipo, *Vector Control and Dynamics of AC Drives*. London, U.K.: Oxford Science Publications, 1996.



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