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DC Power-Bus Design Using FDTD Modeling With Dispersive Media and Surface Mount Technology Components

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***Abstract*—DC power-bus modeling in high-speed digital design using the finite-difference time-domain (FDTD) method is demonstrated herein. The dispersive character of the dielectric layers used in printed circuit board substrates is taken into account in this study. In particular, *FR-4* is considered. The complex permittivity of the dielectric is approximated by a Debye model. A wide-band frequency response (100 MHz–5 GHz) is obtained through a single FDTD simulation. Good agreement is achieved between the modeled and measured results for a typical dc power-bus structure with multiple surface mount technology (SMT) decoupling capacitors placed on the printed circuit board (PCB). The FDTD method is then applied to investigate some general approaches of power-bus noise decoupling.**

***Index Terms*—DC power-bus, Debye model, dispersive media, finite-difference-time-domain method, power-bus noise decoupling, surface mount technology.**

I. Introduction

A DC power-bus structure in a multi-layered printed circuit board (PCB) that employs multiple planes as dc power and ground, is common in high-speed digital circuits. The power and ground plane pair is essentially a parallel-plane waveguide [1]. A sudden change in current consumption of a switching chip (Delta-I noise) at a certain point initiates a voltage disturbance that propagates in the space between the power and ground layers, and excites different modes of the parallel-plane waveguide [2]. This voltage fluctuation can lead to faulty switching of either the exciting chip or other ICs at some distance from the excitation point [3]–[5], and is one of the major concerns for proper signal integrity and electromagnetic compatibility design of high-speed digital circuits. In addition, the propagating noise voltage can lead to EMI as a result of fringing electric fields at the board edges, or can couple to I/O lines that transit through the power/ground layer set and be radiated [6]. Surface-mount technology (SMT) decoupling capacitors are often placed in proximity to switching devices to mitigate both switching noise and RF noise propagation on the power planes [7], [8]. However, as clock speeds and edge rates increase, the effectiveness of the discrete capacitors decreases at the higher frequencies because of the influence of the parasitic interconnect series inductance. The inter-plane capacitance then plays a key role in power-bus noise reduction.

Achieving adequate noise mitigation in dc power-bus design requires proper selection of the values of decoupling capacitors, and their location relative to specific ICs, as well as the material and geometry of the PCB. When applicable, a reliable power-bus model is a powerful tool that can be used for developing design guidelines. Several approaches have been applied to power bus modeling. At frequencies below distributed PCB resonances, a lumped element model, where the power bus is a parallel-plane capacitor, is suitable [7]. At higher frequencies, wire-antenna and radial transmission-line models are appropriate, since they take into account the distributed nature of the power bus [9]. The finite element method (FEM) [10], and the finite-difference-time-domain (FDTD) [11], are widely applied full-wave numerical methods for modeling PCBs. Another class of modeling approaches are equivalent-circuit models extracted from full-wave formulations. Such methods include the partial element equivalent circuit (PEEC) method [12], [13], which is based on a volume integral-equation formulation, and the method of circuit extraction based on a mixed-potential integral equation (CEMPIE) [14], which is a layered-media or PCB substrate PEEC formulation.

For complex PCB design, e.g., boards with a significant number of SMT capacitors, or boards with segmented power or ground planes, the number of unknowns for traditional frequency-domain methods can increase significantly, and the computation can be time and memory intensive. A significant advantage of the FDTD method is that it allows straightforward extension of the approach to more complicated layouts and multiple PCB layers with only a modest increase in the computational domain. The versatility, robustness, and user-friendliness of the FDTD method has been widely demonstrated when dealing with electrodynamic structures of complicated geometry and various materials [15]. Its utility for power-bus modeling and design with dispersive PCB materials is shown in this study. FDTD algorithms have been reported with direct linkage to SPICE to model the lumped circuits, and with the full 3-Dimensional solution to Maxwell's equations to model other distributed circuits [16]. The FDTD and SPICE

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computer programs are coupled using various interprocess communication techniques.

Another advantage of the FDTD method is that it allows for analyzing structures in a wide frequency band with a single time-domain simulation. However, special treatment is necessary to model the dielectric substrates utilized in PCB circuit design, especially at high frequencies when the dispersive nature of the substrates can not be neglected. The FDTD method presented in this paper uses a Debye material model to approximate the frequency dependence of the complex dielectric permittivity, and the dispersive character of the *FR-4* dielectric layers is taken into account. A wide-band frequency response (100 MHz–5 GHz) is obtained through a single FDTD simulation. Good agreement is achieved between the modeled and measured results for a typical dc power-bus structure with multiple surface mount technology (SMT) decoupling capacitors placed on the printed circuit board.

In Section II, the FDTD formulation for modeling a dc power-bus with dispersive media is given in detail. The Debye parameters are determined for the *FR-4* material, which is used as the dielectric substrate in this study. In Section III, the modeled and measured results are compared for a typical dc power bus stack, which is a power/ground parallel plane structure with 16 SMT decoupling capacitors uniformly placed on the board. Applications of the FDTD method for power-bus design are considered in Section IV.

II. FDTD Formulation for Modeling Dispersive Media

The derivation of the basic FDTD updating equations used to advance Maxwell's equations in time and space has been documented extensively [15], [17]. The basic FDTD updating equations can model the dispersive dielectric media within a relatively narrow frequency range by specifying a constant value of effective dielectric conductivity, as will be shown in Section III. However, multiple simulations are often necessary to generate the results for a wide bandwidth, and it turns out to be inefficient. An approach using recursive convolution of constitutive parameters and corresponding field components in the time domain for linear isotropic frequency-dependent complex permittivity improves the computational efficiency of the FDTD method [18], [19]. There are also alternative approaches. One of them, applicable to media with a dispersive permittivity (including nonlinear cases) is based on formulating and discretizing an auxiliary differential equation that expresses the relation between the displacement vector $\vec{D}$ and the electric field $\vec{E}$ [20]. Both approaches—using convolution or an auxiliary differential equation between the correspondent field components—can also be applied to media with frequency-dependent permeability.

Recursive convolution is straightforward and is memory and time efficient for modeling linear materials [15]. However, the frequency dependence of the material permittivity or permeability must be a "well-behaved" function having a causal Fourier (or Laplace) transform, and must be written as a sum of complex exponentials of time with constant coefficients. Only linear, isotropic, nonmagnetic dielectric materials are considered in this work. Therefore, only equations for updating the E-field components require special treatment. Equations for updating the H-fields are the same as for a nondispersive dielectric medium.

A Debye dielectric with a frequency-dependent permittivity function given by [21] is used to model an *FR-4* material commonly used in PCB substrates

$$\varepsilon(\omega) = \varepsilon_0\varepsilon_\infty + \varepsilon_0\frac{\varepsilon_s - \varepsilon_\infty}{1 + j\omega\tau_r} \tag{1}$$

where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, ε_s is the static relative dielectric constant, ε_∞ is the relative "optic" permittivity, and τ_r is the relaxation time. The Debye model describes the behavior of a low-loss dielectric in the lower part of the microwave band (300 MHz– *several* gigahertz), where dispersion and loss are primarily associated with the polarization of the molecules. However, for higher frequencies and high-loss dielectrics, especially composite materials with metal or magnetic particle inclusions, this model may be not valid, and a more general single-pole or multipole Lorentzian model must be applied [22]. A more suitable approximation of the Debye model for FR-4 incorporates the conductivity of the dielectric, σ_e, into the complex relative permittivity (considered in the frequency domain) [23]

$$\varepsilon_r = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{1 + j\omega\tau_r} - \frac{j\sigma_e}{\omega\varepsilon_0} \tag{2}$$

and the functions for updating the E-fields for a Debye material are [18]

$$\begin{aligned}\vec{E}^{n+1}(m) =& \frac{\varepsilon_0\varepsilon_\infty}{\varepsilon_0(\varepsilon_\infty + \chi_0) + \sigma_e\Delta t}\cdot\vec{E}^n \\ &+ \frac{\varepsilon_0}{\varepsilon_0(\varepsilon_\infty + \chi_0) + \sigma_e\Delta t}\cdot\vec{\Phi}^n(m) \\ &+ \frac{\varepsilon_0\Delta t}{\varepsilon_0(\varepsilon_\infty + \chi_0) + \sigma_e\Delta t}\cdot\nabla_d\times\vec{H}^{n+(1/2)}\end{aligned} \tag{3}$$

where $\nabla_d\times$ is the discrete curl operator derived from applying central differencing on the H field in space [15], and m denotes a node (i, j, k). The function $\vec{\Phi}^n(m)$ corresponds to the discrete convolution

$$\vec{\Phi}^n(m) = \vec{E}^n\cdot(\varepsilon_s - \varepsilon_\infty)\cdot\left(1 - e^{-\Delta t/\tau_r}\right)^2 + e^{-\Delta t/\tau_r}\vec{\Phi}^{n-1}(m) \tag{4}$$

and

$$\chi_0 = \int_0^{\Delta t}\frac{\varepsilon_s - \varepsilon_\infty}{\tau_r}e^{-\tau/\tau_r}d\tau = (\varepsilon_s - \varepsilon_\infty)\left(1 - e^{-\Delta t/\tau_r}\right). \tag{5}$$

Then, in calculating $\vec{\Phi}^n(m)$, only the value at the current time step must be stored during the numerical computation. The updating equation for the H-field components is unchanged from that normally used, because only frequency-dependent permittivity materials are considered for the dc power-bus structures of concern herein.

Equations (2)–(4) are the required time-marching equations for modeling a dispersive dielectric media. Special treatment is needed for modeling the interface between lossy and lossless dielectrics. The displacement vector $\vec{D}$ at the dielectric-dielectric interface is the weighted average of $\vec{D}^\varepsilon$ and $\vec{D}^0$ as

$$\vec{D} = \alpha\vec{D}^\varepsilon + \beta\vec{D}^0 \tag{6}$$

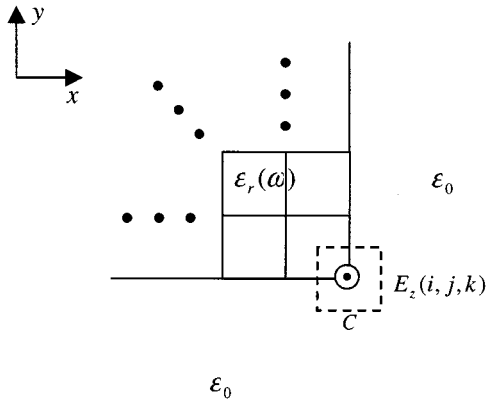

Fig. 1. Contour of integration at the dielectric-free space boundary.

where $\vec{D}^{\varepsilon}$ is the displacement vector for a lossy dielectric, and $\vec{D}^{0}$ is the displacement vector for the lossless air dielectric, and in this case $\alpha+\beta=1$. An example of determining coefficients α and β is shown in Fig. 1. The FDTD node (i,j,k) is located at the corner of a dielectric substrate. The integral form of Ampere's Law for the contour C and area $\Delta x\Delta y$ is

$$\begin{aligned}\iint_{\Delta x\times\Delta y} D_z\cdot ds &= \iint_{1/4(\Delta x\times\Delta y)} D_z^{\varepsilon}\cdot ds \\ &\quad+\iint_{3/4(\Delta x\times\Delta y)} D_z^{0}\cdot ds \\ &= \oint_{\mathrm{C}} \vec{H}\cdot d\vec{l}+\iint_{1/4(\Delta x\times\Delta y)} \sigma E_z\cdot ds.\end{aligned} \tag{7}$$

It is straightforward to get the value of $\alpha=1/4$ and $\beta=3/4$ for the D_z component at node (i,j,k). The result is a simple averaging of the dielectric media over the surface bounded by the contour C, which includes the dispersive dielectric. The weights of α and β may vary for different electric-field components of the same node, but for brevity in the formulation α and β are used for all three components, and

$$\begin{aligned}\vec{D}^{n}(m) =&\alpha\cdot\left(\varepsilon_0\varepsilon_\infty\vec{E}^{n}(m)+\varepsilon_0\sum_{p=0}^{n-1}\vec{E}^{n-p}\cdot\chi^{p}\right)\\ &+\beta\cdot\varepsilon_0\vec{E}^{n}(m)\end{aligned} \tag{8}$$

$$\frac{\vec{D}^{n+1}(m)-\vec{D}^{n}(m)}{\Delta t}=\nabla_d\times\vec{H}^{n+(1/2)}+\alpha\cdot\sigma_e E^{n+1}. \tag{9}$$

The final updating equation for the electric-field component at (i,j,k) shown in Fig. 1 is

$$\begin{aligned}\vec{E}^{n+1}(m) =&\frac{\varepsilon_0(\alpha\varepsilon_\infty+\beta)}{\varepsilon_0(\alpha\varepsilon_\infty+\alpha\chi_0+\beta)+\alpha\sigma_e\Delta t}\cdot\vec{E}^{n}\\ &+\frac{\alpha\varepsilon_0}{\varepsilon_0(\alpha\varepsilon_\infty+\alpha\chi_0+\beta)+\alpha\cdot\sigma_e\Delta t}\cdot\vec{\Phi}^{n}(m)\\ &+\frac{\varepsilon_0\Delta t}{\varepsilon_0(\alpha\varepsilon_\infty+\alpha\chi_0+\beta)+\alpha\cdot\sigma_e\Delta t}\\ &\cdot\nabla_d\times\vec{H}^{n+(1/2)}.\end{aligned} \tag{10}$$

Equation (3) is a special case of (10) with $\alpha=1$ and $\beta=0$. Equation (10) can also be extended for updating the electric-field at the interface of two lossy dielectric materials A and B as shown in (11) at the bottom of the page. Both cases are encountered in modeling the *FR-4* dielectric material and air interface for a PCB substrate.

The Debye constants for the dielectric material must be determined in order to apply the FDTD algorithm to model the *FR-4* PCB substrate. The relative permittivity of the *FR-4* material, which is widely used as PCB substrates in circuit designs, varies with frequency and temperature. Therefore, some preliminary measurements are necessary. A cavity method for measuring the relative dielectric constant of *FR-4* used in the PCB substrate is reported in [24]. For glass-filled epoxies (*FR-4* belongs to this group) the reference data gives $\varepsilon_r=4.7\pm20\%$ at 1 MHz, which decreases at high frequency to 4.2, and the loss tangent ranges between 0.01–0.03 depending on the frequency [25]. The *FR-4* material used in this paper has a relative dielectric constant $\varepsilon_r=4.3$ at 500 MHz, which decreases as the frequency increases. Four constants, ε_s, ε_∞, τ_r, and σ_e must be determined for modeling the dielectric as a Debye material represented by (2), and they must approximate the properties of the material in a wide frequency range (at least 100 MHz–5 GHz, the operating frequency band of the PCB under consideration). By letting $\varepsilon_r=4.3+j0.0946$ at 500 MHz and $\varepsilon_r=4.2+j0.105$ at 5 GHz, which specifies $\tan\delta=0.022$ at 500 MHz and 0.025 at 5 GHz, respectively (which corresponds to the *FR-4* manufacturer's measured data), four equations with four unknowns can be generated. The nonlinear system of equations yields a sixth order polynomial equation of unknown τ_r. Of the six solutions, only one is a real positive number with $\tau_r=0.333\,169\times10^{-10}$ s. Then ε_s, ε_∞, and σ_e are obtained as 4.3021, 4.1068, and 0.002 068 S/m, respectively. The dc conductivity is incorporated in the complex permittivity [23], which leads to the divergent behavior of the loss tangent for frequencies approaching zero. However, the frequencies of interest for dc power bus design in this paper are higher than 100 MHz,

$$\begin{aligned}\vec{E}^{n+1}(m) =&\frac{\varepsilon_0\left(\alpha\varepsilon_\infty^{A}+\beta\varepsilon_\infty^{B}\right)}{\varepsilon_0\left(\alpha\varepsilon_\infty^{A}+\alpha\chi_0^{A}+\beta\varepsilon_\infty^{B}+\beta\chi_0^{B}\right)+\left(\alpha\sigma_e^{A}+\beta\sigma_e^{B}\right)\Delta t}\\ &\cdot\vec{E}^{n}+\frac{\alpha\varepsilon_0\cdot\vec{\Phi}_A^{n}(m)+\beta\varepsilon_0\cdot\vec{\Phi}_B^{n}(m)}{\varepsilon_0\left(\alpha\varepsilon_\infty^{A}+\alpha\chi_0^{A}+\beta\varepsilon_\infty^{B}+\beta\chi_0^{B}\right)+\left(\alpha\sigma_e^{A}+\beta\sigma_e^{B}\right)\Delta t}\\ &+\frac{\varepsilon_0\Delta t}{\varepsilon_0\left(\alpha\varepsilon_\infty^{A}+\alpha\chi_0^{A}+\beta\varepsilon_\infty^{B}+\beta\chi_0^{B}\right)+\left(\alpha\sigma_e^{A}+\beta\sigma_e^{B}\right)\Delta t}\cdot\nabla_d\times\vec{H}^{n+(1/2)}.\end{aligned} \tag{11}$$

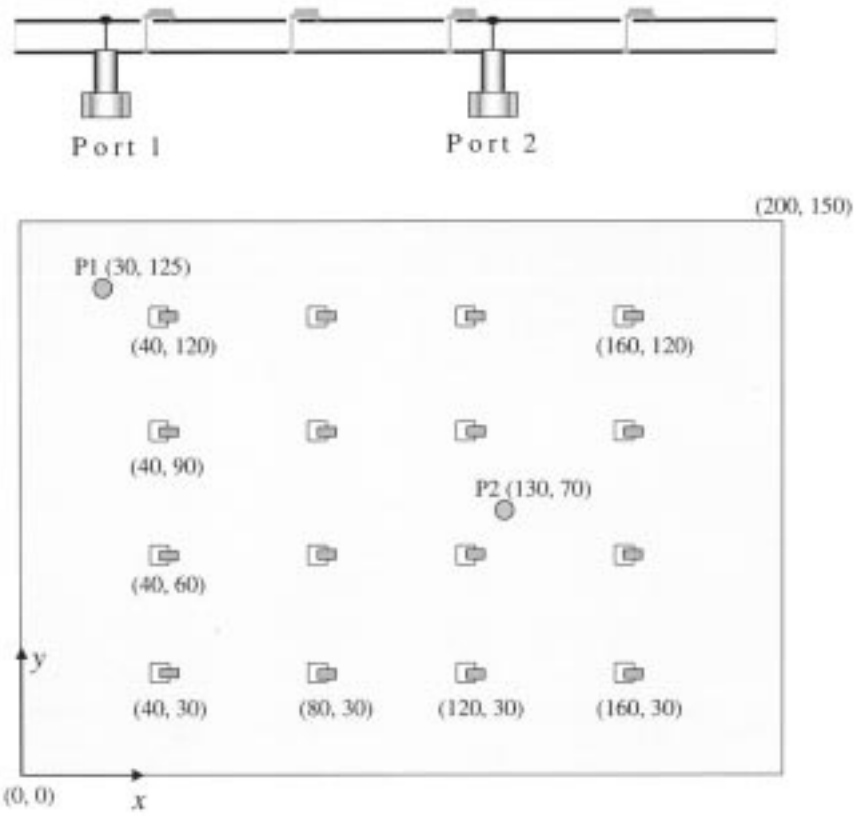

Fig. 2. Schematic of the test board with 16 decoupling capacitors—side view and top view. All dimensions are in millimeters. The coordinates of each decoupling capacitor correspond to the center of the square aperture.

which is beyond the divergent range of the Debye model presented in (2).

III. Modeled and Measured Results

The FDTD algorithm described previously was then applied to model a dc power-bus comprised of two metallization layers with an *FR-4* dielectric spacer. The power-bus geometry schematically shown in Fig. 3 has a power-ground structure with SMT decoupling capacitors distributed over the board[1]. It is a 150 mm $\times$ 200 mm double-sided PCB, and the dielectric layer is a 1.65 mm (65 mil.) thick *FR-4* material. Sixteen decoupling capacitors are uniformly distributed over the board. One end of each decoupling capacitor is soldered directly to the top plane, while the other end is connected to the bottom plane by a short length of *AWG 24* wire (with a diameter of 24 mils.). Sixteen 2-mm $\times$ 2 mm square apertures were cut in the upper plane to allow the *AWG 24* wires to penetrate the plane without electrically contacting the top metal layer. The coordinates (in millimeters) of the aperture centers where the wires penetrate through the plane, as well as of the two test ports, are indicated in Fig. 2. Port 1 (30 mm, 125 mm) is located close to the board corner to excite as many modes of the parallel-plane waveguide as possible. Port 2 (130 mm, 70 mm) is selected arbitrarily. Both test ports were constructed using semirigid coaxial cables. The outer shields were soldered to the ground plane with a 360 ° connection, and the center conductors extended through the thickness of the board and soldered to the upper plane as shown in Fig. 2. MACOM-type SMA connectors are mounted on the other ends of the semirigid cables for the connection of test instruments. Two-port measurements were conducted using an *HP 8753D* network analyzer, and the electrical lengths of the semirigid coaxial cables and SMA connectors were removed using the port extension feature of a full-path two-port calibration.

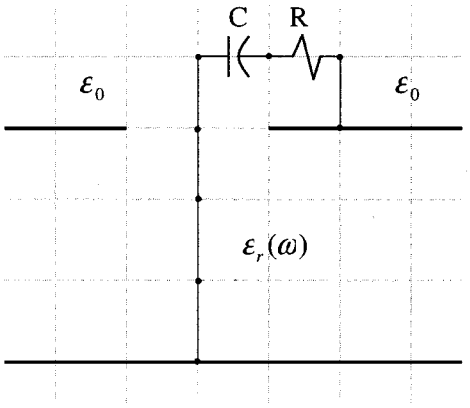

Fig. 3. Local subcells of modeling a decoupling capacitor.

The basic computational domain for the FDTD method consists of a rectangular mesh bounded by perfectly matched layers (PML) to simulate an infinite space [26]. The computational domain was discretized by a uniform mesh of 1 mm $\times$ 1 mm $\times$ 0.055 mm, along x, y, and z-axes, respectively. There were three FDTD cells within the board thickness,

[1]The test board shown in Fig. 2 was also used in a previous study [28].

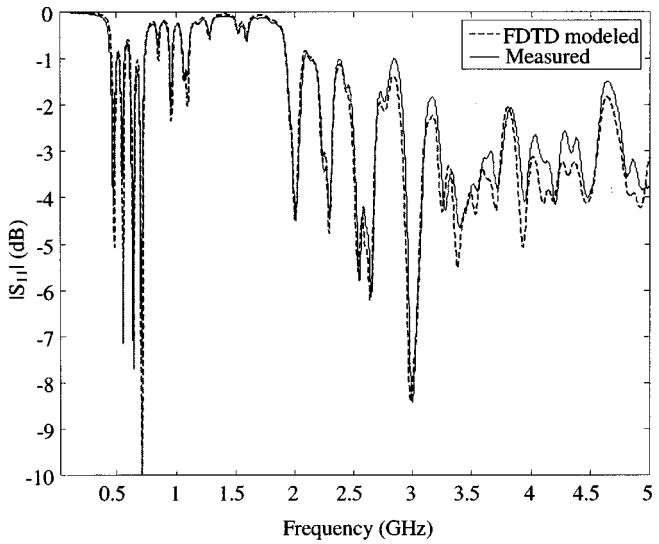

Fig. 4. Measured and FDTD modeled $|S_{11}|$ of the dc power-bus with 16 decoupling capacitors.

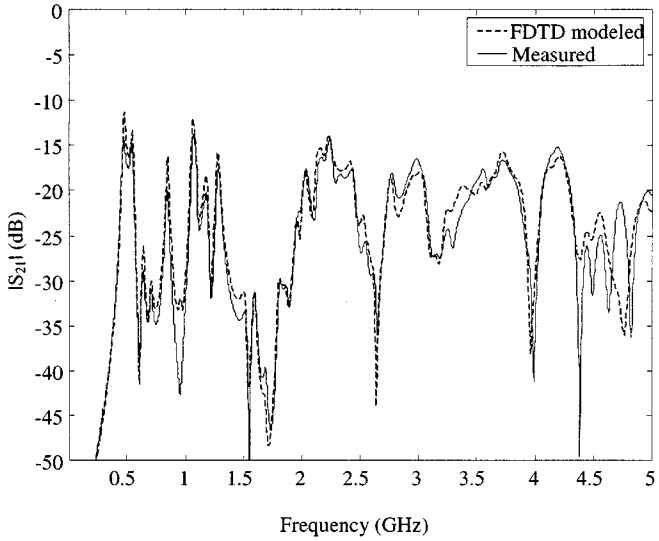

Fig. 5. Measured and FDTD modeled $|S_{21}|$ of the dc power-bus with 16 decoupling capacitors.

and each aperture in the power plane was modeled with four cells. A sinusoidally modulated Gaussian 50 Ω voltage source was applied vertically above the lower plane. The wire structures were modeled using a thin wire algorithm [15]. The upper and lower conducting planes were modeled as perfect electric conductors (PECs) of zero thickness. Eight PML layers were placed at each boundary plane of the computational domain, and seven white space layers were placed between the PML and the test board.

Each SMT decoupling capacitor was modeled as an ideal capacitor with an equivalent series resistance (ESR). Two FDTD cells were used for this purpose, one for the capacitor and one for a resistor, as shown in Fig. 3. The nominal capacitance used was 9 nF, and the resistance was 130 mΩ. These values were determined by an impedance measurement of one of the SMT capacitors using an *HP4291A* impedance/material analyzer. By including the lead wires of the capacitor in the modeling, the parasitic inductance of the interconnect was taken into account. The algorithm for incorporating capacitor and resistor subcells in the FDTD modeling was realized on the basis of an approach proposed in [27]. The Debye model parameters determined in Section II were used to approximate the *FR-4* material in the FDTD modeling of the power-bus geometry shown in Fig. 2. The modeled and measured results ($|S_{11}|$ and $|S_{21}|$) are shown in Figs. 4 and 5. Good agreement is achieved in a wide frequency band from 100 MHz to 5 GHz. The discrepancies may be due in part to the inconsistency and variation in *FR-4* over the power-bus volume.

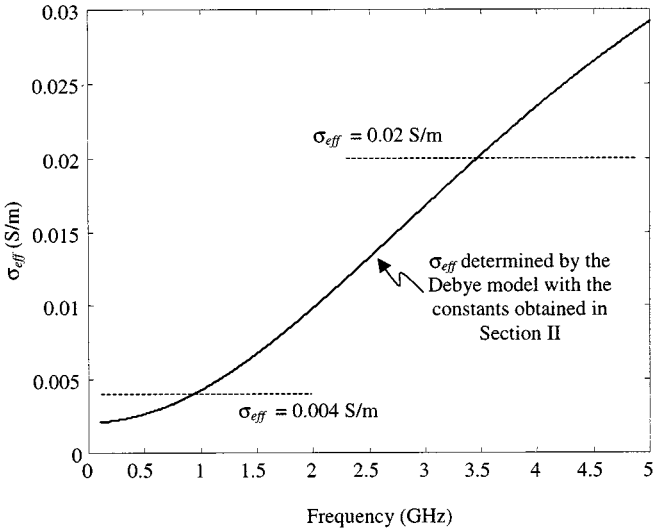

Fig. 6. The calculated effective dielectric loss of the Debye model with the constants obtained in Section II.

A simple FDTD approach, which describes the frequency dependent loss of the media by a constant real value of effective conductivity in a number of individual narrow frequency bands, was used in a previous study [28]. The effective conductivity was given by (frequency domain)

$$\begin{aligned}\nabla \times \vec{H} &= j\omega\varepsilon\vec{E} + \vec{J} = j\omega\varepsilon'\vec{E} + (\omega\varepsilon'' + \sigma_e)\vec{E} \\ &= j\omega\varepsilon'\vec{E} + \sigma_{\text{eff}}\vec{E} \end{aligned} \tag{12}$$

where σ_{eff} is frequency-dependent as seen in the equation. The calculated σ_{eff} from the Debye model with the constants obtained in Section II is shown in Fig. 6. By specifying a constant value of σ_{eff}, the dielectric loss can by included in the model using the normal Yee-algorithm updating equations. Two simulations were conducted using the normal FDTD method with $\sigma_{\text{eff}} = 0.004$ S/m and $\sigma_{\text{eff}} = 0.02$ S/m, respectively, and the real part of the relative dielectric constant was 4.2 for both cases. The modeled and measured results are shown in Fig. 7. The modeled result with the smaller σ_{eff} is adequate at lower frequencies, while the discrepancy is significant at higher frequencies due to insufficient loss in the FDTD modeling. The modeled result with the larger σ_{eff} agrees well with the measured results at higher frequencies, while the discrepancy is significant at lower frequencies due to excessive loss in the modeling. Multiple simulations are necessary to generate the results for a wide frequency band. FDTD modeling using the dispersive algorithm shown in Section II for the dielectric material applied in this

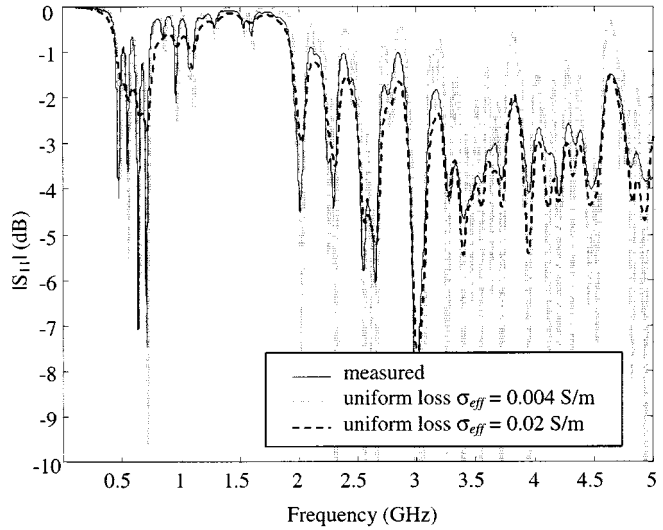

Fig. 7. FDTD modeled $|S_{11}|$ of the dc power-bus using uniform effective dielectric loss.

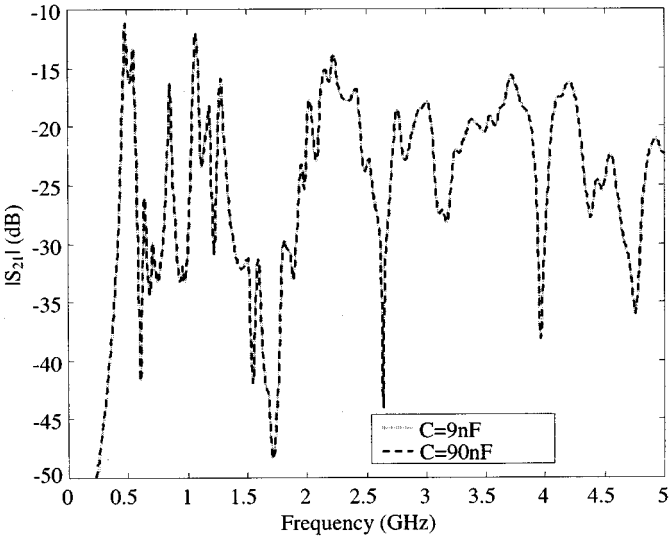

Fig. 8. FDTD modeled $|S_{21}|$ of the power-bus structure with 16 decoupling capacitors for different values of decoupling capacitor.

paper is advantageous, since only one simulation is required for a wide bandwidth. Furthermore, there is only a negligible increase of time and memory requirement for the single simulation using a Debye dispersive model compared to those for one individual narrow-band simulation in the nondispersive case.

IV. Design Applications

In this section, the FDTD algorithm detailed in Sections I–III is applied to several *what-if* scenarios to demonstrate the effectiveness and robustness of the approach in dc power-bus design. The first case investigated is changing the value of the decoupling capacitors from 9 to 90 nF. By assuming the package size of the capacitors remains the same, the parasitics remain the same, and the only difference between these two cases is the value of C shown in Fig. 3. The FDTD modeled results for the two cases are shown in Fig. 8. They are virtually identical for the studied frequency range. At 500 MHz or higher frequencies,

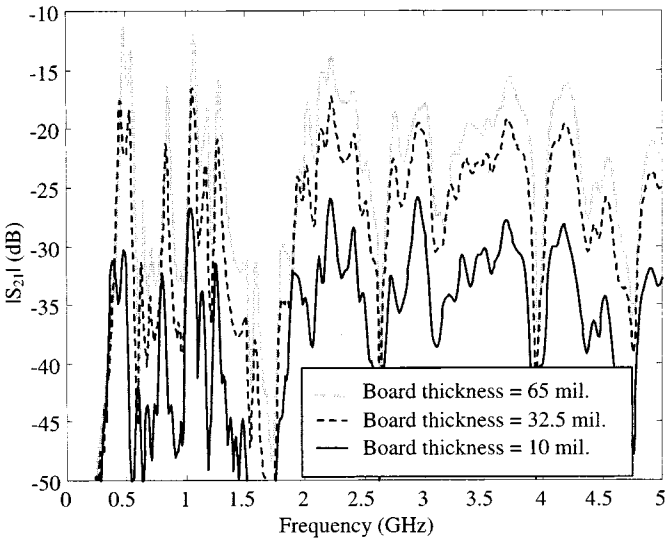

Fig. 9. FDTD modeled $|S_{21}|$ of the power-bus structure with 16 decoupling capacitors for different board thickness.

the impedance of a 9 nF ideal capacitor is much smaller than the parasitic impedance of the interconnect (the equivalent series resistance and the inductance of the vias). Therefore, increasing the value of the decoupling capacitor (while the parasitics remain the same) only marginally changes the impedance of each individual capacitor at these frequencies, and the modeled $|S_{21}|$ is virtually the same. Meanwhile, at high frequencies, the parasitic impedance of the interconnect is usually larger than the impedance of the parallel plane, and these discrete SMT decoupling capacitors are ineffective in reducing the power bus noise. On the other hand, using the largest value of capacitance in a given package provides the best lower frequency performance (below approximately 100 MHz).

Fig. 9 shows the comparison of modeled $|S_{21}|$ with different board thicknesses. When the board thickness is decreased from 1.65 mm (65 mil.) to 0.825 mm (32.5 mil.), there is a 3–5 dB decrease of the modeled $|S_{21}|$. The decrease of $|S_{21}|$ is 12–15 dB when the board thickness is decreased from 1.65 mm to 0.254 mm (10 mil.). This power-bus noise reduction results from the larger interplane capacitance, which plays a key role in decoupling the noise at high frequencies when the discrete capacitors lose their effectiveness due to the parasitic interconnect inductance. Fig. 10 shows the FDTD modeled input impedance of the power-bus structure for different board thickness. Smaller power/ground separation results in smaller input impedance of the plane set, and hence, better bypassing of the noise on the power plane. Another benefit of using smaller power/ground separation is that it also reduces the EMI due to fringing edge fields [28], and due to noise coupling from the power bus to an I/O line transitioning through the power/ground layers [29].

The effect of the lossy dielectric substrate on power-bus noise decoupling was also investigated. When the loss tangent was chosen five times larger than the original value, the modeled $|S_{21}|$ decreased significantly (8–12 dB), as shown in Fig. 11. Increasing the dielectric loss of the material in the power/ground layer space reduces the power-bus noise at high frequencies.

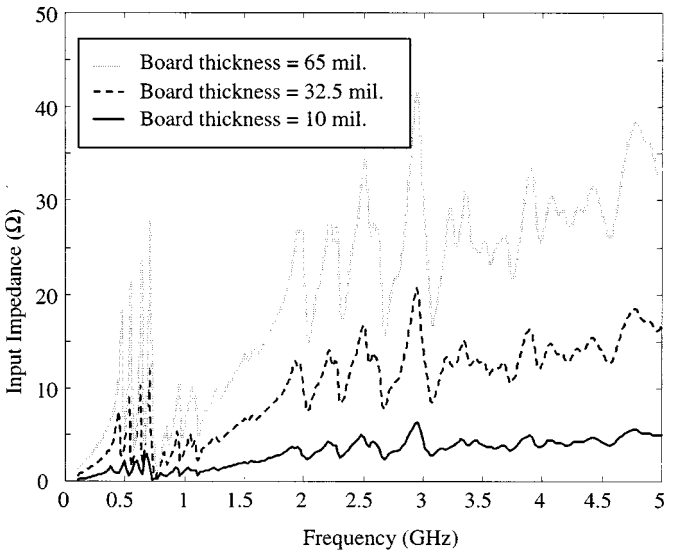

Fig. 10. FDTD modeled input impedance of the power-bus structure with 16 decoupling capacitors for different board thickness.

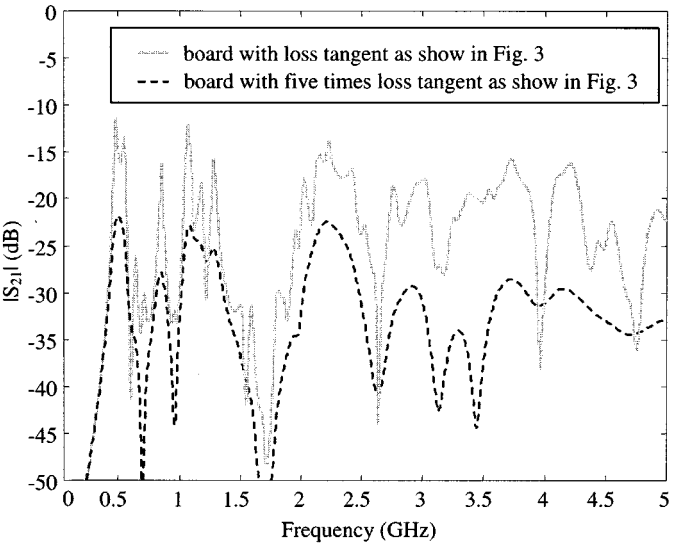

Fig. 11. FDTD modeled $|S_{21}|$ of the power-bus structure with 16 decoupling capacitors for different dielectric loss.

Another effective way of mitigating power-bus noise for larger power/ground layer spacings is to place decoupling capacitors close to the IC. The capacitor can then be tightly coupled to the power pins of the IC as a result of mutual inductance between the vias of the IC and the decoupling capacitor [30]. At high frequencies, the parasitic self-inductance of the decoupling capacitor dominates the electrical performance, and the capacitor itself can not provide a low impedance path for bypassing of the noise current on the power-bus. However, the mutual inductance between the vias of the IC and the decoupling capacitor works as a current divider over a wide frequency range, and it reduces the power-bus noise magnitude. This effect of locally placed decoupling capacitors was investigated in detail in [31]. The following example demonstrates that the FDTD method can be a suitable modeling tool to investigate this phenomenon. Four local decoupling capacitors

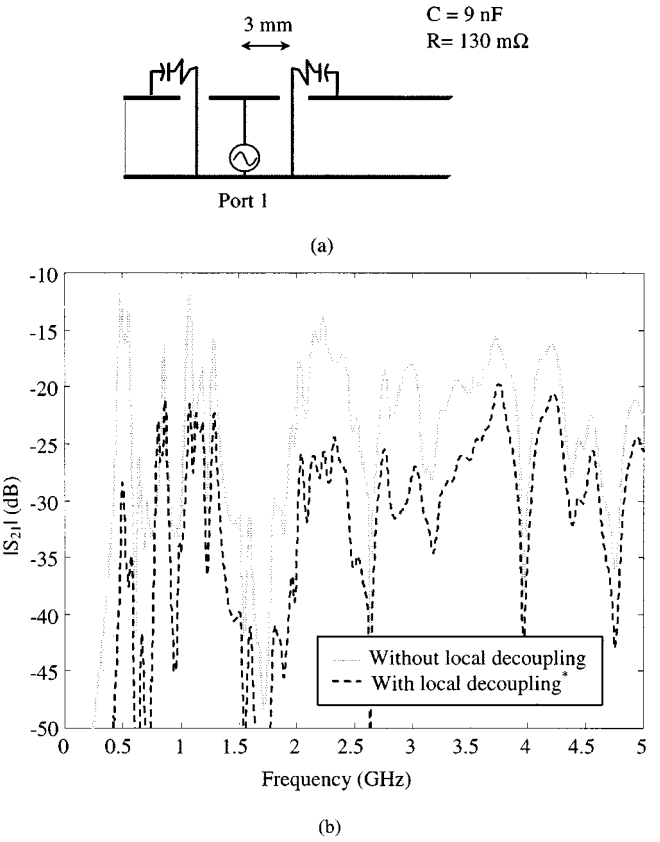

Fig. 12. (a) Geometry for local decoupling. (b) FDTD modeled $|S_{21}|$ of the power-bus structure with 16 decoupling capacitors and the effect of local decoupling for 65-mil. substrate.

were placed symmetrically (two in the x direction and two in the y direction) around Port 1 for the geometry shown in Fig. 2. The 16 global decoupling capacitors remained in plane. The thickness of the *FR-4* layer was 65 mils. Each capacitor had the same individual value of 9 nF, and the same parasitics as shown in Fig. 3. The spacing between the via of the decoupling capacitor and the via of the feeding pin was 3 mm. The modeled $|S_{21}|$ is shown in Fig. 12. These local decoupling capacitors significantly reduce the power-bus noise over a wide frequency band. The mutual inductive coupling between the vias of the feed port and decoupling capacitor is a function sensitive to the layer thickness [31]. While significant benefits can be achieved with local decoupling for the 65-mil. substrate shown, the noise mitigation for a thin substrate is much less, as detailed in [31]. In this paper, it was also verified with FDTD modeling for a 10-mil. substrate.

The benefits of local decoupling capacitors do not necessarily mean that the global decoupling capacitors are ineffective for decoupling power-bus noise. The comparison between "local only" and "global only" cases shown in Fig. 13 indicates that the global decoupling capacitors are more effective in reducing the power bus noise for frequencies lower than approximately 400 MHz for the particular board dimensions being used. This is because at lower frequencies these global decoupling capacitors still effectively provide low impedance bypassing for the noise propagating on the power bus. Further, adequate global decoupling is also necessary to ensure signal integrity.

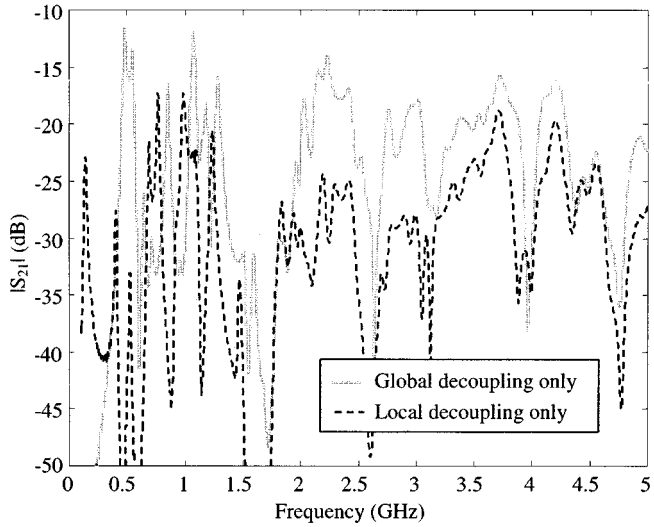

Fig. 13. FDTD modeled $|S_{21}|$ of the power-bus structure with 16 global decoupling capacitors or with only four local decoupling capacitors.

V. Conclusion

FDTD modeling for dc power-bus design in high-speed digital circuits has been presented. A Debye model for approximating the frequency dependent behavior of the permittivity of the *FR-4* dielectric material commonly used in printed circuit boards was shown to be suitable over the frequency range of 100 MHz to 5 GHz. The necessary frequency dependence of the material parameters for the Debye approximation was developed from manufacturer measured data. Then, a wide-band frequency response (100 MHz–5 GHz) was obtained through a single FDTD simulation. SMT decoupling capacitors including the ESR and parasitic interconnect inductance are easily included in the modeling. Good agreement was achieved between the modeled and measured results for a typical dc power-bus structure with multiple SMT decoupling capacitors placed on the PCB.

The good agreement between the measurements and modeling over a very wide frequency band demonstrates that the FDTD method incorporating the dispersive and lossy nature of *FR-4* is a powerful tool for dc power bus design. The examples considered in Section IV illustrate that it is suitable for addressing typical issues in power bus design such as the value and location of discrete SMT decoupling capacitors, power/ground layer separation, incorporating loss into the power bus, and noise transfer functions between a switching IC and a susceptible device.

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