

01 Nov 2006

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Recommended Citation

P. Xiao et al., "Cancellation Predictive Control for Three-Phase PWM Rectifiers under Harmonic and Unbalanced Input Conditions," *Proceedings of the 32nd Annual Conference on IEEE Industrial Electronics IECON 2006*, Institute of Electrical and Electronics Engineers (IEEE), Nov 2006.

The definitive version is available at <https://doi.org/10.1109/IECON.2006.347994>

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Cancellation Predictive Control for Three-Phase PWM Rectifiers under Harmonic and Unbalanced Input Conditions

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Abstract – This paper presents an intuitive and simple-to-implement control scheme to improve the performance of three-phase boost-type PWM rectifiers under harmonic and unbalanced input conditions. Unlike most other control strategies, the proposed method does not need to extract either the harmonic or the negative-sequence components in the supply voltages and currents. A near-synchronous reference frame is used to determine the positive-sequence fundamental-frequency component in the input voltages. Utilizing only the extracted component, the dc-link voltage control and power factor control are implemented independently to determine the phase angle and magnitude of the PWM reference voltage. The commanded rectifier voltage adjustments are superimposed upon the grid voltages in such a way that the distortions (both harmonic and negative sequence components) are effectively cancelled. By employing a near-synchronous reference frame, no line-synchronization algorithm or hardware PLL is needed, so very little computational effort is required for its implementation. Simulation results show that the proposed method performs very well under extreme harmonic and unbalanced conditions such as when one or even two phases of the grid voltages are zero. In order to further verify its effectiveness, a laboratory hardware platform has been developed.

I. INTRODUCTION

Three-phase PWM active rectifiers have received significant attention in recent years due to their superiority over the traditional line-side diode or phase-controlled thyristor rectifiers. Their advantages include low distortion line currents, unity power factor, and bi-directional power flow capability.

Since harmonics and unbalanced conditions are not uncommon in power distribution networks, the behaviour of PWM rectifiers under these non-ideal conditions draws particular attention. On the one hand, the rectifier must be able to operate normally under various supply conditions. According to recommended harmonic standard IEEE 519, these conditions include maximum allowable 5% supply voltage harmonics, $\pm 10\%$ supply voltage sags/swells, up to 10% supply voltage unbalance, etc. On the other hand, the rectifier itself must meet the harmonic standard and should not inject harmonic currents into the distribution system, even in the presence of non-ideal supply voltages.

Harmonics in distribution systems are mainly caused by nonlinear loads, while unbalance may arise under severe fault conditions in the system where both line impedance and voltages could become unsymmetrical. Voltage distortion due to current harmonics is becoming a major issue for distribution networks. Elimination of the effects of these

non-ideal conditions using passive filters proved to be very costly in terms of size, weight, and maintenance. So the best strategy is to design the rectifier controller such that rectifier operation is immune to these conditions. If the controller is only designed to operate under ideal supply voltages, harmonic components in the supply voltages may degrade the rectifier performance and result in harmonic currents, even if the controller can keep the output dc voltage constant. The effects of input unbalance on rectifier operations were studied in detail in [1], which concludes that unbalanced input voltages or impedances can result in the appearance of even harmonics at the dc output and odd harmonics in the input currents.

Numerous papers [2-6] have dealt with the issue of PWM boost-type rectifier operations under harmonic and/or unbalanced input conditions. However, many of them tried to extract the harmonic or negative sequence components with complex algorithms. In [2], a feed-forward control method was proposed based on sequence component analysis, which adds negative sequence component to the commanded reference currents to eliminate second harmonic in the dc output voltage. Unfortunately, power factor cannot be adjusted when unbalance is present. In [3], a novel control method was used for rectifier operation under unbalanced input voltages and unequal line impedances. The method does not require the use of synchronous reference transformation, but the computational effort gain is marginal considering its high-order current regulator.

This paper presents a control scheme that cancels simultaneously both harmonic and unbalance components in the supply voltages. It features decoupled dc voltage and power factor control. A predictive delay compensator is used to further improve its performance. The method is simple to implement and straightforward to analyze, and it can perform very well even under extreme non-ideal conditions.

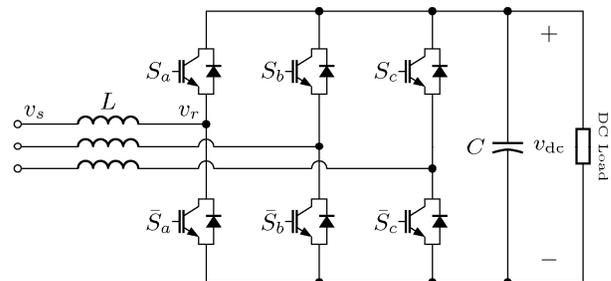


Fig.1. PWM Boost-type rectifier topology.

II. DECOUPLED RECTIFIER CONTROL UNDER BALANCED CONDITIONS

Fig. 1 shows the schematic of a three-phase three-wire PWM boost-type rectifier. The three rectifier switch arms are connected to the grid network via a three-phase boost inductor L . Under balanced conditions and without harmonics, the grid voltage v_s and the rectifier average voltage v_r can be represented by two voltage vectors with magnitude V_s and V_r , and a phase angle difference $\phi_r = \angle v_r - \angle v_s$. It is shown that the power transferred from the grid to the rectifier can be expressed by

$$S = 3 \frac{V_s V_r}{X} \sin \phi_r + 3j \frac{V_s V_r \cos \phi_r - V_r^2}{X} \quad (1)$$

where X is the reactance of the boost inductor and the inductor resistance is assumed to be negligible.

Obviously there is a nonlinear relationship between power and the rectifier voltage. However, ϕ_r generally is small and the voltage magnitude V_r is close to V_s . Thus it follows that real power is mainly determined by the phase angle ϕ_r , while reactive power can be effectively adjusted by changing the commanded rectifier voltage magnitude V_r . Based on this observation, a decoupled control of real and reactive power is developed, where the phase angle and magnitude of commanded rectifier voltage are controlled independently.

A. DC Voltage Control

To develop the dc voltage control model, assume that the dc load resistance is R and the dc-link capacitance is C . The energy stored in the capacitor is $E_C = CV_{dc}^2/2$, so the instantaneous power flowing into the capacitor is

$$P_C = \frac{dE_C}{dt} = \frac{C}{2} \frac{dV_{dc}^2}{dt}. \quad (2)$$

The power into the dc load is

$$P_R = \frac{V_{dc}^2}{R}. \quad (3)$$

If switching device losses are assumed to be negligible compared to the power consumed by the load, the ac-side active power equals to the dc-side power. Let V_{dc}^2 be the output Y and $\sin(\phi_r)$ be the input U , a transfer function can be derived as

$$G(s) = \frac{Y(s)}{U(s)} = \frac{V_{dc}^2(s)}{\sin \phi_r} = 3 \frac{V_s V_r}{X} \frac{R}{1 + \frac{RC}{2}s}, \quad (4)$$

which shows that appropriate choice of input/output variables gives a linear first-order system model. For such a system, a controller $H(s)$ can be readily designed to meet stability and transient specifications. It should be noted that since the pole location of the system varies for different loads, the controller should be robust enough to give desired performance under all load conditions.

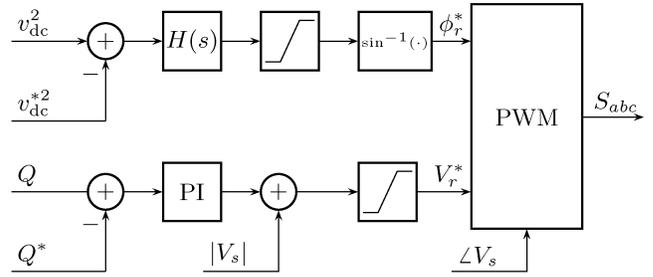


Fig. 2. Decoupled rectifier control scheme

B. Power Factor Control

The power factor of the rectifier is controlled via the regulation of the reactive power. From (1) it can be seen that for a fixed ϕ_r , increasing V_r tends to decrease the reactive power into the rectifier, while decreasing V_r would increase the reactive power. A PI controller is used to keep the reactive power at a desired level Q^* .

The complete decoupled control diagram is shown in Fig. 2. The generated reference ϕ_r^* and V_r^* , together with the phase angle of v_s , can be sent directly to a PWM modulator to produce the appropriate switching signals. This control method is advantageous in that the switching frequency is constant and no additional current regulation loop is necessary. Unity power factor can be achieved by setting the reference reactive power Q^* to zero. Actually, the method offers controllable power factor which is a desirable feature for certain power system applications.

III. RECTIFIER CONTROL UNDER HARMONIC AND UNBALANCED CONDITIONS

A. Harmonics and Unbalance in q-d Reference Frame

To better explain the operation of PWM boost-type rectifiers under harmonic and unbalanced conditions, it is appropriate to transform three-phase quantities into the synchronous q - d reference frame. Here it is assumed that the fundamental frequency of the grid voltage is f_0 . The source voltage v_s consists of four types of components. After the transformation, the fundamental positive-sequence component V_s^+ becomes dc in the synchronous reference frame. The fundamental negative-sequence component V_s^- becomes a signal with twice the fundamental frequency, i.e. $2f_0$. All non-zero-sequence harmonics V_s^h would have a shift in their frequency by either f_0 or $-f_0$, depending on their phase sequences. The zero-sequence components V_s^0 are not changed by the transformation. However, for a three-wire system there is no current path for zero-sequence components, so their presence does not affect the rectifier operation. It has been shown in [3] that the zero-sequence current component does not exist in any reference frame.

Table I.
Harmonic and unbalance components in the synchronous q-d reference frame.

| <i>abc</i> | | <i>qd</i> |
|------------|----------|-----------|
| Frequency | Sequence | Frequency |
| f_0 | + | dc |
| f_0 | - | $2f_0$ |
| $5f_0$ | + | $4f_0$ |
| $5f_0$ | - | $6f_0$ |
| $7f_0$ | + | $6f_0$ |
| $7f_0$ | - | $8f_0$ |
| $11f_0$ | + | $10f_0$ |
| $11f_0$ | - | $12f_0$ |
| $13f_0$ | + | $12f_0$ |
| $13f_0$ | - | $14f_0$ |

Common harmonics in distribution systems include 5th, 7th, 11th, 13th, and so on. Under three-phase balanced conditions, 5th and 11th harmonics are negative sequence, so they would appear in the synchronous reference frame as 6th and 12th harmonics, respectively. Since 7th and 13th harmonics are positive sequence, they also appear as 6th and 12th harmonics in the synchronous reference frame. If the system is unbalanced, it is possible that there exist positive-sequence 5th harmonic and negative-sequence 7th harmonic, and they would be transformed to 4th and 8th harmonics in the synchronous reference frame. Table I summarizes the transformation for different harmonics.

B. Extraction of Fundamental Component

The proposed methodology ensures that only the fundamental positive-sequence component V_s^+ in the source voltage is used for power transfer between the grid and the rectifier. All other components are not supposed to deliver either real or reactive power and should be cancelled. Since V_s^+ becomes dc quantities in both q and d axes, they can be readily extracted using a low-pass filter. The cut-off frequency of the filter can be designed to be several hertz or even lower. Since the lowest possible harmonic frequency in q - d is $2f_0$, even a simple single-pole low-pass filter would provide significant attenuation for both negative-sequence and harmonic components. Hence, only V_s^+ is extracted after the filtering. However, the cut-off frequency should also be high enough to avoid a slow transient response of the controller.

The decoupled rectifier control described in the last section is used for dc-link voltage and power factor control. Let the extracted V_s^+ component be v_{qs}^+ and v_{ds}^+ in q and d axes, respectively, as shown in the vector diagram in Fig. 3. Its phase angle in the q - d fram can be calculated as

$$\theta_s = \tan^{-1} \left(\frac{-v_{ds}^+}{v_{qs}^+} \right). \quad (5)$$

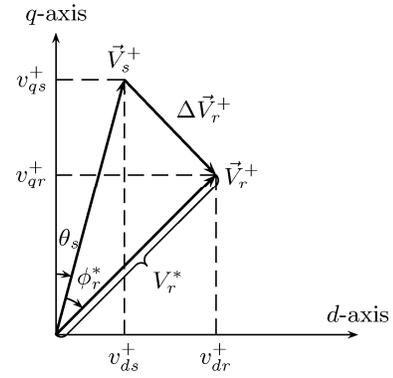


Fig. 3. Source and rectifier voltage vector diagram.

Then with the reference phase angle ϕ_r^* and magnitude V_r^* obtained from the decoupled control, the phase angle of the desired rectifier voltage can be determined as $\theta_r = \theta_s + \phi_r^*$, and the fundamental positive-sequence rectifier voltage V_r^+ can be established as:

$$\begin{aligned} v_{qr}^+ &= V_r^* \cos \theta_r \\ v_{dr}^+ &= -V_r^* \sin \theta_r \end{aligned} \quad (6)$$

C. Harmonic and Unbalance Cancellation

If the source voltage is ideal, v_{qr}^+ and v_{dr}^+ can be inverse transformed into the abc frame and directly used for PWM modulation. However, since harmonics and/or unbalance may be present in the source voltage, an extra step is necessary. The difference between voltage vectors V_r^+ and V_s^+ is ΔV_r^+ , and its q - and d -axis quantities are

$$\begin{aligned} \Delta v_{qr}^+ &= v_{qr}^+ - v_{qs}^+ \\ \Delta v_{dr}^+ &= v_{dr}^+ - v_{ds}^+ \end{aligned} \quad (7)$$

When transformed into the abc frame the above quantities become Δv_{ar}^+ , Δv_{br}^+ , and Δv_{cr}^+ , which are the three-phase voltage adjustments for the rectifier control. The commanded rectifier voltages (v_{ar}^* , v_{br}^* , and v_{cr}^*) are obtained by adding these adjustments to the three-phase source voltages (v_{as} , v_{bs} , and v_{cs}), that is

$$\begin{aligned} v_{ar}^* &= v_{as} + \Delta v_{ar}^+ \\ v_{br}^* &= v_{bs} + \Delta v_{br}^+ \\ v_{cr}^* &= v_{cs} + \Delta v_{cr}^+ \end{aligned} \quad (8)$$

Since the voltages at the two terminals of the boost inductor contain exactly the same harmonic and unbalanced components, ideally they would cancel each other and do not produce any harmonic current in the inductor.

IV. DELAY COMPENSATION WITH PREDICTIVE CONTROL

When the rectifier is implemented with a digital controller such as a DSP, inevitable time delay is introduced. Part of the

delay is due to A/D conversion and calculations, therefore faster processor and shorter control time period can reduce the amount of time. Another phenomenon that contributes to the time delay is PWM averaging. For a given reference voltage V at time t , it takes a switching period T_{sw} to generate a PWM waveform V that has an average value equal to V . The averaged voltage is equivalent to a constant voltage V centered at time $t + T_{sw}/2$.

As an example, suppose the control period and switching period are synchronized with a frequency $f_{sw} = 20$ kHz, as shown in Fig. 4. At $t = 0$, A/D converter starts sampling and converting the measured signals. When all the data is ready, the DSP performs calculations to determine the desired rectifier voltage. Note that this voltage is based on measurement taken at time $t = 0$, but it can only be generated during the next switching period, i.e. from $t = 50 \mu\text{s}$ to $t = 100 \mu\text{s}$. The effective voltage is actually centered at $t = 75 \mu\text{s}$, so there is a time delay of $T_d = 75 \mu\text{s}$.

This time delay may result in deviations of the actual averaged PWM voltage from the ideal reference voltage, especially for applications with relatively slow micro-processor or low switching frequency. A discussion of effects of computational time delay on PWM power converters can be found in [4] and [5].

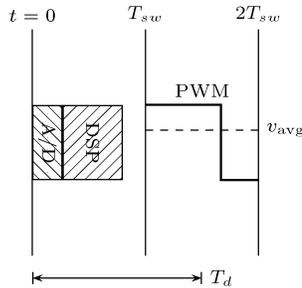


Fig. 4. Time delay due to computation and PWM.

A. Effects of Time Delay on Power Control

A time delay between the reference voltage and the actual averaged PWM voltage can be represented by a phase angle change $\Delta\phi$. Equation (1) indicates that an increase in the phase angle difference ϕ would result in more active power transfer. However, due to the use of feedback control, the controller would output a smaller reference angle ϕ^* , which effectively compensates the time delay. Therefore, computational delay can be automatically compensated for dc voltage and power factor control.

B. Effects of Time Delay on Harmonic Cancellation

The harmonics and unbalance in the source voltages can only be cancelled when the rectifier generates exactly the same components as those in the source. A time delay in the generation of rectifier voltage thus results in differences between the harmonic components in the source and the rectifier. For higher control and switching frequency, the differences are small and the cancellation, although not exact, still gives satisfactory performance. The lower the

control/switching frequency is, the larger the differences are and the cancellation performance would degrade. In addition, the time delay has a larger impact on high frequency harmonics because the same amount of time means larger phase lag for higher frequencies.

C. Predictive Delay Compensation

To improve the performance of the harmonic/unbalance cancellation control, a predictive method was chosen to compensate the effects of time delay. In a DSP implementation, the source voltage is generally sampled at the beginning of every control period. After the measured voltages are converted to digital values, quadratic extrapolation is performed to predict the voltage values at time $t + T_d$, where T_d is the time delay. This requires two history voltage data points to be stored.

Assume the measured voltages are v_1 , v_2 , and v_3 at time t_1 , t_2 , and t_3 , then the voltage v_4 at t_4 can be predicted as follows:

$$v_4 = \frac{(t_4 - t_2)(t_4 - t_3)}{(t_1 - t_2)(t_1 - t_3)}v_1 + \frac{(t_4 - t_1)(t_4 - t_3)}{(t_2 - t_1)(t_2 - t_3)}v_2 + \frac{(t_4 - t_1)(t_4 - t_2)}{(t_3 - t_1)(t_3 - t_2)}v_3. \quad (9)$$

Let $t_3 = t$, then the previous two data points are sampled at $t_1 = t - 2T_{sw}$ and $t_2 = t - T_{sw}$, respectively. Define

$$k = \frac{T_d}{T_{sw}}, \quad (10)$$

then $t_4 = t + T_d = t + kT_{sw}$. It can be derived from (9)

$$v_4 = K_1v_1 + K_2v_2 + K_3v_3, \quad (11)$$

where

$$\begin{aligned} K_1 &= 0.5(k + k^2) \\ K_2 &= -2k - k^2 \\ K_3 &= 1 + 1.5k + 0.5k^2. \end{aligned} \quad (12)$$

Generally the time delay due to computation and PWM is constant and can be pre-determined based on the control and switching frequency, therefore the three coefficients K_1 , K_2 and K_3 in (12) can be calculated beforehand and used as constants in the control program.

The predicted supply voltages \hat{v}_{as} , \hat{v}_{bs} , \hat{v}_{cs} are then used in (8) in the place of v_{as} , v_{bs} , v_{cs} to produce the reference voltages for PWM modulation.

V. CONTROL IMPLEMENTATION

One concern which may arise is how to obtain the synchronous angle for reference frame transformation. The most common procedures include using a phase-lock-loop (PLL) circuit or a line-synchronization algorithm. The first approach obviously adds to system cost, while the second one consumes computational power. In addition, it can be very difficult to extract phase information from distorted

source voltages.

A close examination of the proposed control method indicates that the reference frame does not have to be obtained from the source voltage measurements. First, as shown in Fig. 3, the q -axis of the reference frame used does not have to be aligned with the source voltage vector. Moreover, even the frequency of the reference frame need not be exactly the same as the system frequency, as long as they are close enough. For example, if there is a 0.1 Hz difference between the two frequencies, v_{gr}^+ and v_{dr}^+ would become ac quantities with a frequency of 0.1 Hz. However, this is not a problem if the cut-off frequency of the low-pass filter is much higher than 0.1 Hz, say 5 Hz, which still provides sufficient attenuation for the harmonic and negative-sequence components. Considering that the normal frequency variation of most commercial power systems is about $\pm 0.5\%$, a natural choice of the reference frame is one that has the rated system frequency f_0 and an arbitrary initial angle, which greatly simplifies the implementation.

Another issue is the measurement of source voltages. Generally two voltage sensors are used to measure

instantaneous line-to-line voltages v_{ab} and v_{bc} , while the proposed method requires the use of line-to-neutral voltages v_{as} , v_{bs} , and v_{cs} . If the source voltage is distorted, it is not possible to determine the true v_{as} , v_{bs} , and v_{cs} from the line-to-line voltage measurements. However, since zero-sequence components have no effect on the rectifier operation, they can be removed and a unique set of voltages can be determined:

$$\begin{aligned} v_{as} &= \frac{2}{3}v_{ab} + \frac{1}{3}v_{bc} \\ v_{bs} &= -\frac{1}{3}v_{ab} + \frac{1}{3}v_{bc} \\ v_{cs} &= -\frac{1}{3}v_{ab} - \frac{2}{3}v_{bc}. \end{aligned} \quad (13)$$

These voltages contain all the information of the actual line-to-neutral voltages except the zero-sequence components, and thus are suitable for the transformation and control calculations. The complete control diagram is shown in Fig. 5.

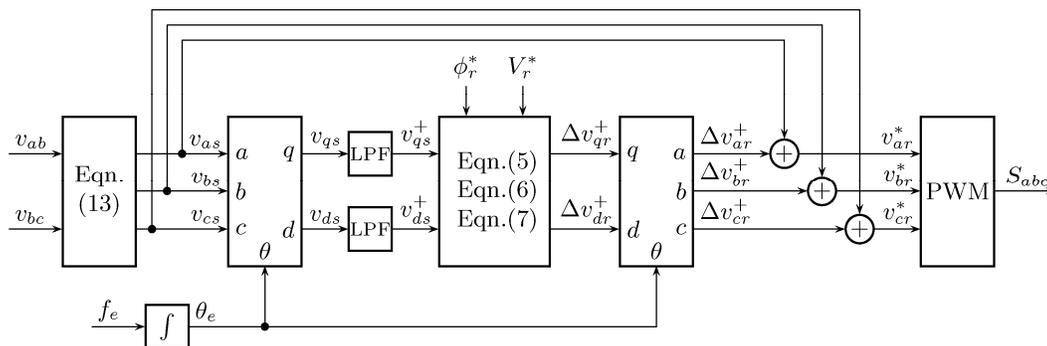


Fig. 5. Complete control block diagram.

VI. SIMULATION RESULTS

Simulation results are shown in Figs. 6-8 to confirm the proposed control methodology. To verify the effectiveness of the predictive time delay compensation method, the rectifier is operated under a relatively small amount of distortions, where the magnitude of a -phase voltage is 10% higher than its nominal value, and the source voltages contain 5th (6%) and 7th (1%) harmonics.

In the first simulation as shown in Fig. 6, the time delay compensation is not used. The switching frequency is set to 20 kHz and the time delay is around $75 = \mu\text{s}$. For fundamental frequency negative-sequence components, the delay would cause a phase shift of 1.6° ; while for the 7th harmonic, the same delay would introduce a phase shift of 11.3° . As can be seen, the three-phase currents are balanced and the dc voltage contains very little second harmonic, which means that the cancellation control method works very well in eliminating the unbalance components. However, it can be seen that the time delay results in some harmonic currents, especially for harmonics of higher frequencies,

The simulation results with time delay compensation are shown in Fig. 7. Obviously the harmonic contents in the three-phase currents are much less than those for the case without delay compensation.

To further illustrate the effectiveness of the proposed control methodology, the rectifier is tested under conditions where highly unbalanced voltages are present with very large amount of harmonics.

For extreme condition test, the a -phase voltage magnitude is set to 0, and there is a significant amount of harmonics (20% for 5th, 10% for 7th, 4% for 11th, and 1% for 13th). The results are shown in Fig. 8. It can be seen that the input voltages are highly distorted. The results in Fig. 8 show that the residue harmonic currents are very low even under severe conditions. It should be noted that because the currents are balanced while the source voltages are not, a 120-Hz real power component exists and causes the ripple in the dc voltage.

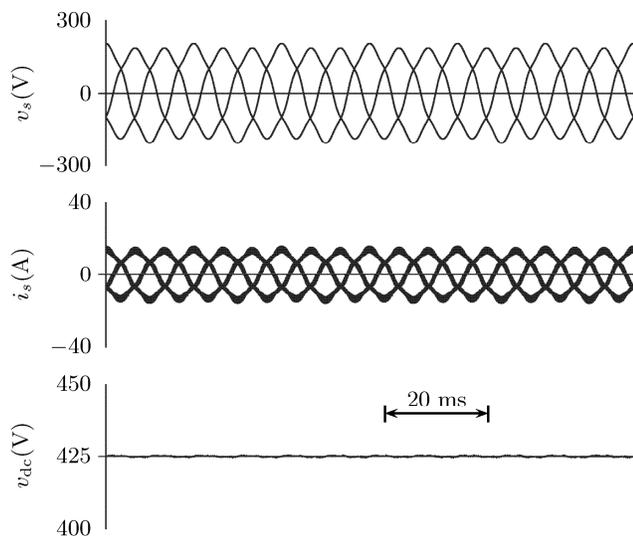


Fig. 6. Operation under small distortions without delay compensation.

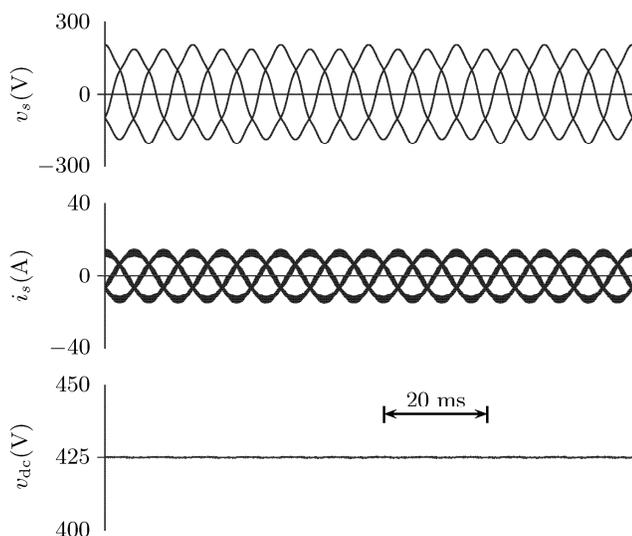


Fig. 7. Operation under small distortions with delay compensation.

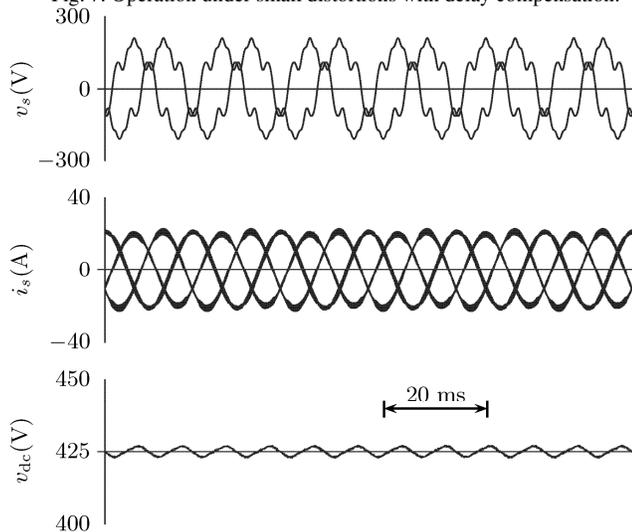


Fig. 8. Operation under severe voltage distortion.

VII. CONCLUSIONS

A novel control method for three-phase voltage source rectifiers under harmonic and unbalanced conditions is proposed. The method has the following features:

- Decoupled dc voltage and power factor control with fixed switching frequency
- Both harmonics and unbalanced input conditions can be cancelled at the same time.
- No line synchronization or PLL is needed for reference frame transformation. Instead, a near-synchronous reference frame is used.
- A predictive method is used to compensate for delay caused by A/D and DSP computations.
- The control method gives satisfactory performance even under extreme harmonic and unbalanced conditions.

Simulation results show that the proposed control methodology can effectively eliminate harmonics in the line currents and dc output voltage due to harmonic and unbalanced input voltages.

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