1-1-2000

Analysis of a Novel Four-Level DC/DC Boost Converter

Keith Corzine
Missouri University of Science and Technology

Sonal K. Majeethia

Analysis of a Novel Four-Level DC/DC Boost Converter

Keith A. Corzine, *Member, IEEE,* and Sonal K. Majeethia, *Student Member, IEEE*

***Abstract*—In this paper, novel two-quadrant buck/boost and one-quadrant boost four-level dc/dc converters are introduced. The primary application for these converters is that of interfacing a low-voltage dc source, such as a fuel cell or battery, to a high-voltage four-level inverter. One important feature of the four-level dc/dc converters proposed herein is the ability to perform the power conversion and balance the inverter capacitor voltages simultaneously. With the capacitor voltage balancing, it is possible to obtain the full voltage from the inverter. For the boost converter, the steady-state and nonlinear average-value (NLAM) models are developed. The NLAM is verified against a detailed simulation of a four-level converter/inverter drive system. The proposed converter is experimentally verified using an 18-kW converter/inverter system.**

***Index Terms*—Average-value modeling, dc/dc converters, four-level converters, multilevel converters.**

I. Introduction

THE general trend in power electronics devices has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. However, the increase in switching frequency increases the switching losses which become especially significant at high power levels. Several methods for decreasing switching losses have been proposed including constructing resonant inverters and multilevel inverters [1].

Resonant inverters avoid switching losses by adding an *LC* resonant circuit to the hard-switched inverter topology. The inverter transistors can be switched when their voltage or current is zero, thus mitigating switching losses. Examples of this type of inverter include the resonant dc link [2], and the auxiliary resonant commutated pole inverter (ARCP) [3], [4]. One disadvantage of resonant inverters is that the added resonant circuitry will increase the complexity and cost of the inverter control. Furthermore, high insulated gate bipolar transistor (IGBT) switching edge rates can create switch-level control problems.

Multilevel inverters offer another approach to reducing switching losses. In particular, these converters offer a high number of switching states so that the inverter output voltage can be "stepped" in smaller increments [5]–[11]. This allows mitigation of harmonics at low switching frequencies, thereby reducing switching losses. In addition, EMC concerns are reduced through the lower common-mode current facilitated by lower *dv/dt*s produced by the smaller voltage steps. One disadvantage of these techniques is that they require a high number of switching devices. The primary disadvantage of multilevel inverters is that they must be supplied from isolated dc voltage sources or a bank of series capacitors with balanced voltages. In systems where isolated dc sources are not practical, capacitor voltage balancing becomes the principal limitation for multilevel inverters.

One of the most popular industrial multilevel inverters is the diode-clamped three-level inverter [5], [7], [8], [10]. It has been well established that the dc capacitor voltages can be readily balanced through the use of straightforward selection of redundant inverter switching states [10]. However, for inverters with a higher number of levels, the voltage balancing through redundant state selection limits the output voltage to 50% of the maximum [12], [13]. For this reason, some systems incorporate auxiliary dc/dc converters for capacitor voltage balancing [14]–[17]. Some interesting three-level boost dc/dc converters have been proposed for systems that are powered from a low-voltage source such as a battery, fuel cell, or superconducting magnetic energy storage (SMES) [18]–[20]. In this paper, a novel four-level dc/dc converter is presented. The standard steady-state and average-value modeling techniques are applied to this new converter. Detailed and average-value model simulation demonstrates the converter performance.

II. Proposed Four-Level DC/DC Converter

A. Converter Description

Fig. 1 shows the novel four-level two-quadrant converter proposed herein. This converter can operate as a boost or buck converter depending on weather the dc source $v_{\rm dc}$ is supplying or absorbing power respectively. For many applications, bidirectional power flow is not necessary and the semiconductor parts count can be reduced to the topology shown in Fig. 2. In a standard boost converter, one transistor and one diode are used for the boost process [21], [22]. In this new topology, two additional transistors are added in order to provide additional switching states that can be used to balance the capacitor voltages. It should be pointed out that although there are three times as many transistors as with a standard boost converter, the switches are rated at 1/3 of the dc voltage and, thus, the overall semiconductor cost is roughly the same. Fig. 3 shows the possible switching states of the four-level dc/dc converter. States 0 and 4 are the two states typically used for dc/dc boost

Paper IPCSD 00–023, presented at the 1999 Industry Applications Society Annual Meeting, Phoenix, AZ, October 3–7, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Drives Committee of the IEEE Industry Applications Society. Manuscript submitted for review July 1, 1999 and released for publication March 31, 2000.

K. A. Corzine is with the Department of Electrical Engineering, University of Wisconsin, Milwaukee, WI 53211 USA (e-mail: corzine@umw.edu).

S. K. Majeethia is with the Automotive and Industrial Electronics Group, Motorola, Northbrook, IL 60062 USA (e-mail: Sonal_Majeethia-G16550@email.mot.com).

Publisher Item Identifier S 0093-9994(00)07626-X.

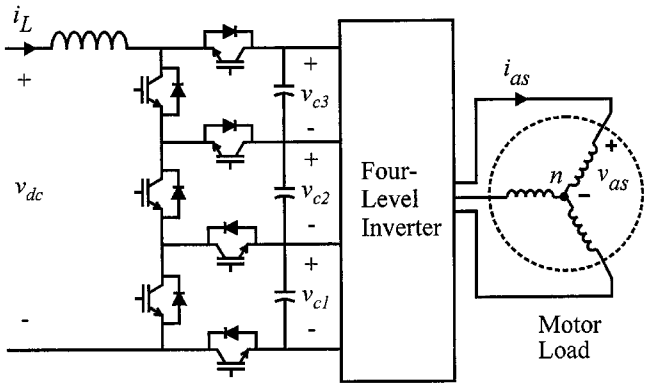

Fig. 1. Proposed four-level two-quadrant dc/dc converter.

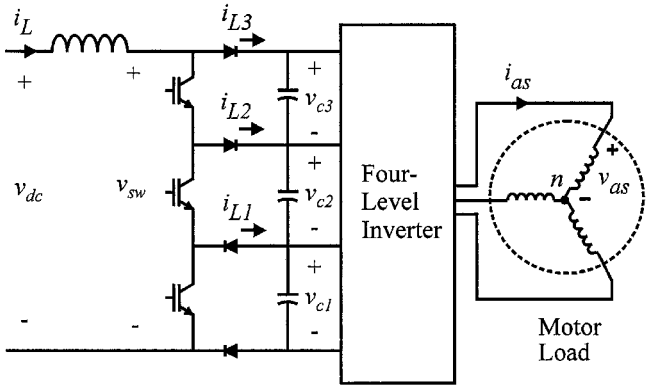

Fig. 2. Proposed four-level one-quadrant boost converter.

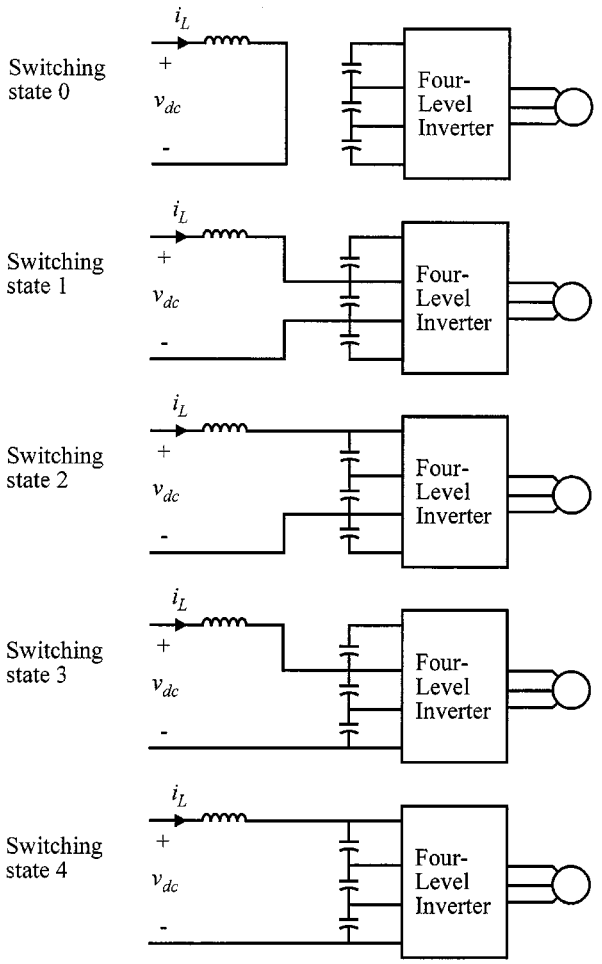

Fig. 3. Four-level one-quadrant converter switching states.

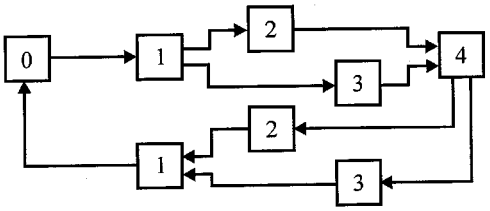

Fig. 4. Four-level converter switching sequence.

conversion. Due to the nature of the motor impedance load and the switching of the four-level inverter transistors, the voltage of the center capacitor v_{c2} tends to discharge to zero in this system. For this reason, state 1 is inserted in the switching sequence in order to increase the charge on the center capacitor. A secondary goal of this converter is to balance the voltages on the upper and lower capacitors. Although this is typically not difficult in four-level inverters, states 2 and 3 can be added to ensure this balance.

B. Switching Sequence

One advantage of multilevel dc/dc power conversion is a reduction in the inductor current ripple when compared to a standard dc/dc converter. For the three-level dc/dc converter, a reduction in current ripple can be accomplished by defining the switching sequence as a function of the input and output voltages [18]–[20]. In the case of the four-level converter, it is not possible to reduce the current ripple for all operating conditions and simultaneously balance the capacitor voltages. Therefore, one sequence has been chosen with the objective of balancing the capacitor voltages. The overall switching state sequence suggested for this converter is 0–1–(2 or 3)–4–(2 or 3)–1–0. The state diagram for this sequence is shown in Fig. 4. Note that this sequence is similar to that of a standard dc/dc converter with two additional switching states. Two additional duty cycles are defined in the sequence timing for control of the additional states. The timing sequence is defined by

$$\text{state} = \begin{cases} 0, & 0 \le t < d_1 T \\ 1, & d_1 T \le t < (d_1 + d_2) T \\ 2/3, & (d_1 + d_2) T \le t < (d_1 + d_2 + d_3) T \\ 4, & (d_1 + d_2 + d_3) T \le t < T \end{cases} \tag{1}$$

where d_1, d_2, and d_3 are the controller duty cycles and T is the total time spent in the switching states. The remainder of the sequence is to reverse the order spending the same amount of time in each state as before. Therefore, the total time of the switching controller is $T_{\text{sw}} = 2T$.

The amount of time spent at the particular switching state can be controlled depending on the desired output voltage and the capacitor voltage imbalance. For example, the time spent at switching state 1 can be increased in order to increase the voltage across the center capacitor. The time spent at states 2 and 3 can be controlled to maintain the voltage balance between the upper and lower capacitors. The choice as to which state to switch to during the sequence (2 or 3) is made depending on which of the two capacitor voltages v_{c1} or v_{c3} is lower.

C. Duty-Cycle Regulation

The control of the cycles d_1, d_2, and d_3 can be challenging since the system is multi-input multi-output (MIMO). A MIMO control design may be the work of future research in this area. However, a straightforward proportional-plus-integral (PI) control can be implemented. Use of this control was justified by examining the sensitivity of the system outputs (capacitor voltages) to the changing inputs (duty cycles). It was observed that the capacitor voltage v_{c2} was more sensitive to changes in d_2 than v_{c1} or v_{c3}. Furthermore, v_{c1} and v_{c3} were more sensitive to changes in d_1 than v_{c2}. This sensitivity somewhat decouples the system and allows for the following control to be used

$$d_1 = K_{p1} e_1 + K_{i1} \int e_1 \, dt \tag{2}$$

$$d_2 = K_{p2} e_2 + K_{i2} \int e_2 \, dt. \tag{3}$$

The errors e_1 and e_2 are defined by

$$e_1 = v_c^* - v_c \tag{4}$$

$$e_2 = v_{c2}^* - v_{c2} \tag{5}$$

where v_c is the sum of v_{c1}, v_{c2}, and v_{c3}. The commanded voltage on the center capacitor can be set to

$$v_{c2}^* = \frac{1}{3} v_c. \tag{6}$$

The third duty cycle d_3 can set to small a constant value since it is used to control the imbalance between v_{c1} and v_{c3} and this imbalance is typically not much of a problem in four-level systems.

III. Steady-State Modeling

As with other types of dc/dc converters, it is instructive to perform a steady-state analysis of the converter driving a resistive load [18]–[21]. In the case of the four-level boost converter, the circuit topology is that of Fig. 5. Since the goal of this converter is to equalize the capacitor voltages, it will be assumed that the controller duty cycles have been set so that the capacitor voltages are equal, or

$$v_{c1} = v_{c2} = v_{c3} = \frac{v_c}{3}. \tag{7}$$

It will also be assumed that $R_3 > R_1$ so that switching state 3 is used during the time when there is a choice between states 2 and 3. The resulting inductor current waveform is shown in

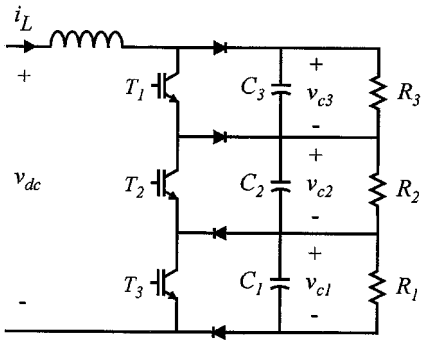

Fig. 5. Four-level converter with resistive load.

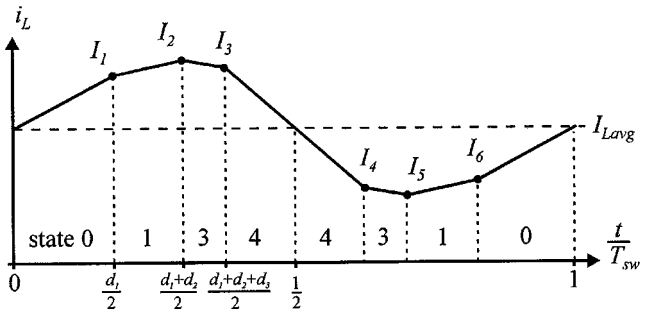

Fig. 6. Steady-state inductor current waveform.

Fig. 6. For steady-state periodic operation, it is necessary that the average inductor voltage be zero. From this requirement, the output to input voltage ratio can be determined as

$$\frac{v_c}{v_{\rm dc}} = \frac{1}{1 - d_1 - \frac{2}{3} d_2 - \frac{1}{3} d_3}. \tag{8}$$

Assuming that the converter losses are negligible, the average inductor current can be found from the output power and input voltage as

$$I_{L\rm avg} = \frac{v_c^2}{9 v_{\rm dc}} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right). \tag{9}$$

From the load equations and the fact that the average capacitor currents must be zero, it can be shown that the steady-state currents, defined in Fig. 6, are

$$\begin{aligned} I_1 = {} & I_{L\rm avg} + \frac{d_3 T_{\rm sw}}{6L} (2 v_c - 3 v_{\rm dc}) \\ & + \cdots \frac{T_{\rm sw}}{2L} (1 - d_1 - d_2 - d_3)(v_c - v_{\rm dc}) \\ & + \cdots \frac{d_2 T_{\rm sw} (v_c - 3 v_{\rm dc})}{6L} \end{aligned} \tag{10}$$

$$\begin{aligned} I_2 = {} & I_{L\rm avg} + \frac{d_3 T_{\rm sw}}{6L} (2 v_c - 3 v_{\rm dc}) \\ & + \cdots \frac{T_{\rm sw}}{2L} (1 - d_1 - d_2 - d_3)(v_c - v_{\rm dc}) \end{aligned} \tag{11}$$

$$\begin{aligned} I_3 = {} & I_{L\rm avg} + \frac{d_3 T_{\rm sw}}{3L} (2 v_c - 3 v_{\rm dc}) \\ & + \cdots \frac{T_{\rm sw}}{2L} (1 - d_1 - d_2 - d_3)(v_c - v_{\rm dc}). \end{aligned} \tag{12}$$

By waveform symmetry

$$I_4 = 2I_{\text{Lavg}} - I_3 \tag{13}$$
$$I_5 = 2I_{\text{Lavg}} - I_2 \tag{14}$$
$$I_6 = 2I_{\text{Lavg}} - I_1. \tag{15}$$

For design purposes, it is often desirable to calculate the inductor current ripple ΔI_L. From (5) to (10), it can be seen that

$$\Delta I_L = 2\left[\max\left(I_1, I_2, I_3\right) - I_{\text{Lavg}}\right]. \tag{16}$$

Note that the maximum current (I_1, I_2, or I_3) depends on the shape of the inductor current and thus depends on the dc input and capacitor voltages. Regardless of which current is the maximum, it can be seen that the inductor current ripple decreases with increasing switching frequency, inductance, and load resistance as is typical of dc/dc converters.

It may be desirable to calculate the required duty cycles for a given set of load resistances. In this case, setting the average capacitor currents to zero yields three equations which can be solved for duty cycles resulting in

$$d_1 = 1 - \frac{3v_{\text{dc}}}{R_2 v_c\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)} \tag{17}$$

$$d_2 = \frac{3v_{\text{dc}}\left(\frac{1}{R_2}-\frac{1}{R_1}\right)}{v_c\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)} \tag{18}$$

$$d_3 = \frac{v_{\text{dc}}\left(\frac{1}{R_1}-\frac{1}{R_3}\right)}{v_c\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)}. \tag{19}$$

Although the steady-state model is useful for design calculations, a dynamic model is needed for evaluating system transient performance.

IV. Nonlinear Average-Value Modeling

The general concept of nonlinear average-value models (NLAMs) is that the high-frequency switching of the power converter is represented on an average-value basis. These models provide insight into the operation of switching converters as well as suggest control strategies. Another advantage of NLAMs is that some simulation packages can linearize these models about an operating point and determine the state space matrices. From this information, classical control theory can be applied and the system stability can be evaluated [22], [23].

Fig. 7 shows the general structure of the NLAM where the converter switches have been replaced by dependant voltage and current sources. Therein, the $\hat{}$ symbol denotes the fast average which is the average value of the quantity over one switching cycle of the converter T_{sw}. The converter waveforms used for determining the dependent source equations are shown in Fig. 8 with the assumption that $v_{c3} > v_{c1}$ and state 2

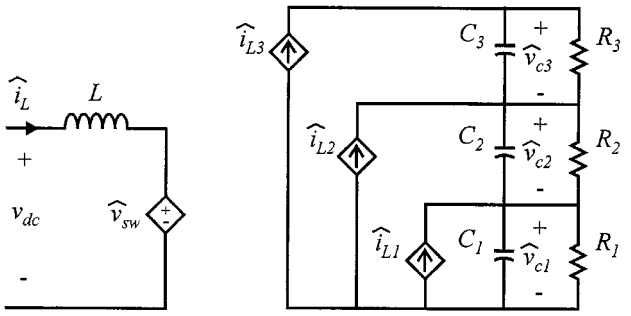

Fig. 7. Converter average-value model structure.

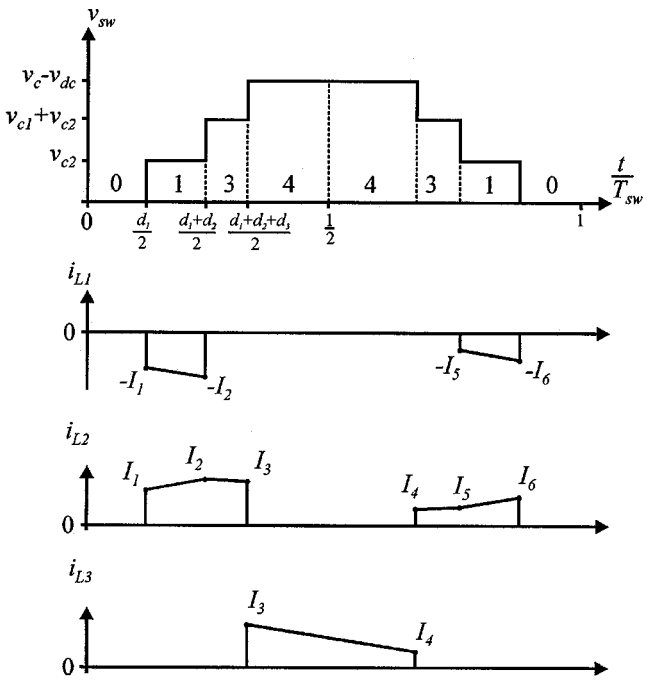

Fig. 8. Converter switching waveforms.

is not used. If the inductor current ripple is neglected, the average-value equations are

$$\hat{v}_{\text{sw}} = \hat{v}_{c2}\left(1-d_1\right) + \hat{v}_{c1}\left(1-d_1-d_2\right) + \cdots \hat{v}_{c3}\left(1-d_1-d_2-d_3\right) \tag{20}$$
$$\hat{i}_{L1} = -\hat{i}_{\text{dc}} d_2 \tag{21}$$
$$\hat{i}_{L2} = \hat{i}_{\text{dc}}\left(d_2+d_3\right) \tag{22}$$
$$\hat{i}_{L3} = \hat{i}_L\left(1-d_1-d_2-d_3\right). \tag{23}$$

If $v_{c1} > v_{c3}$, then the average-value equations become

$$\hat{v}_{\text{sw}} = \hat{v}_{c2}\left(1-d_1\right) + \hat{v}_{c3}\left(1-d_1-d_2\right) + \cdots \hat{v}_{c1}\left(1-d_1-d_2-d_3\right) \tag{24}$$
$$\hat{i}_{L1} = -\hat{i}_{\text{dc}}\left(d_2+d_3\right) \tag{25}$$
$$\hat{i}_{L2} = \hat{i}_{\text{dc}} d_2 \tag{26}$$
$$\hat{i}_{L3} = \hat{i}_L\left(1-d_1-d_2\right). \tag{27}$$

For four-level inverter loads, the unbalance of capacitor voltages v_{c1} and v_{c3} is not severe and the controller will select state 2 over state 3 about one-half of the time. In this case,

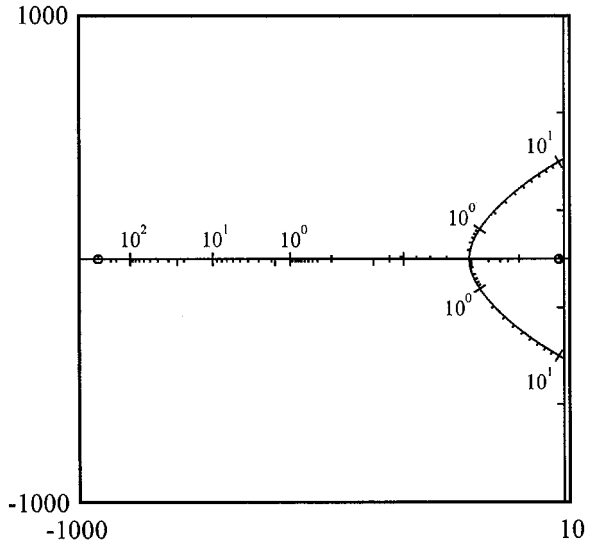

Fig. 9. Four-level dc/dc converter root locus.

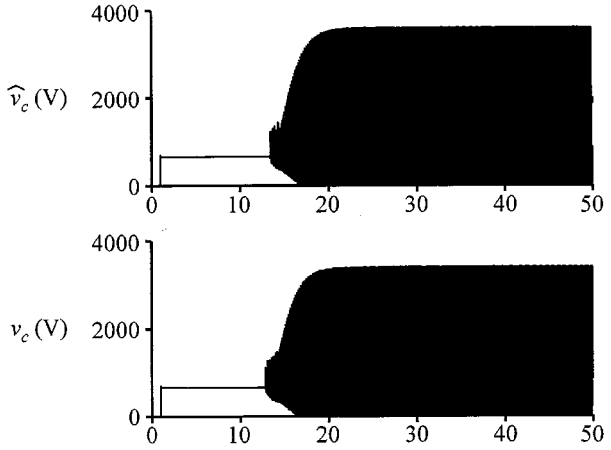

Fig. 10. Capacitor voltage versus controller gain k.

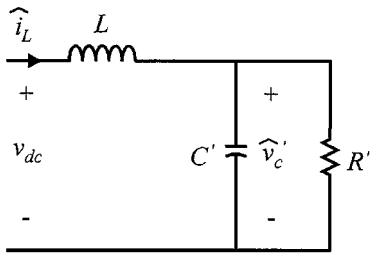

Fig. 11. Standard boost converter NLAM.

the two sets of equations can be averaged to yield one model. For example, an equation for $\hat{v}_{\rm sw}$ can be obtained by averaging (20) and (24).

The NLAM can be used to evaluate the dynamic and steady-state performance of the converter without including the high-frequency switching of the controller. If a resistive load is connected to the NLAM, (8), (9), and (17)–(19) can readily be derived. Alternatively, an NLAM of a four-level inverter can be connected to the converter NLAM for dynamic modeling a drive system as depicted in Fig. 2.

In order to demonstrate stability analysis using the NLAM, consider the four-level dc/dc converter supplying a resistive load, as shown in Fig. 5. For this example, the resistors are set to $R_1 = R_3 = 22.1\ \Omega$ and $R_2 = 11.1\ \Omega$ in order to mimic an imbalance that would exist with an inverter load. The capacitor values are $C_1 = C_2 = C_3 = 6200\ \mu$F and the inductor value is $L = 8.7$ mH. Duty-cycle regulation is used to boost the input voltage from $v_{\rm dc} = 200$ V to $v_c^* = 660$ V using controller gains of $K_{p1} = 0.001$, $K_{i1} = 0.01$, $K_{p2} = 0.2$, and $K_{i2} = 0.5$ with $d_3 = 0.05$. Fig. 9 shows the root locus plot obtained in by linearization of the average-value model about the operating point as predicted using the advanced continuous simulation language (ACSL). The root locus plot is performed by varying the loop gain of the control loop which is regulating the output voltage v_c. As can be seen, there is a complex pole pair crossing into the right-half plane when the loop gain k is increased above 11. This indicates an instability if the controller gains K_{p1} and K_{i1} are increased by a factor of 11. Fig. 10 shows the converter output voltage as predicted by the average-value model and as predicted by a detailed simulation. An instability is clearly seen when the controller gain is increased above 11.

It should be pointed out that the stability of the four-level system has different characteristics than that of a typical two-level boost converter [21] due to the added control loop which regulates v_{c2}. To illustrate this point, an example of a standard boost converter is included herein. The NLAM for this converter may be expressed by its equivalent circuit shown in Fig. 11. The dependent sources have been replaced by referring the output circuit to the input circuit as per a Steinmetz transformer model [24]. In this model, the referred quantities are related to the actual circuit values by the duty cycle d as

$$v_c' = (1-d)v_c \tag{28}$$

$$C' = \frac{C}{(1-d)^2} \tag{29}$$

$$R' = (1-d)^2 R. \tag{30}$$

In this example, the input and desired output voltage have been set to $v_{\rm dc} = 200$ and $v_c^* = 660$ V, respectively. The parameters have been adjusted so that the operation is similar to the four-level example. In particular, $R = 49.8\ \Omega$, $C = 2067\ \mu$F, and $L = 8.7$ mH. The regulator proportional gain is set to zero and the integral gain is set to 0.001. Fig. 12 shows the resulting root locus diagram. As can be seen, a pole pair crosses into the right-half plane for a loop gain of about 4.5. Therefore, the integral gain needs to be less than 0.0045 for stability at this operating point.

V. Four-Level Inverter

Fig. 13 illustrates a four-level diode-clamped inverter [6]–[8], [12], [13]. The general theory of this inverter is that each phase (a, b, or c) can be electrically connected to the junctions d_0, d_1, d_2, and d_3 by appropriate switching of the inverter transistors. By pulsewidth modulation (PWM), the inverter line-to-ground voltages v_{ag}, v_{bg}, and v_{cg} can be directly controlled.

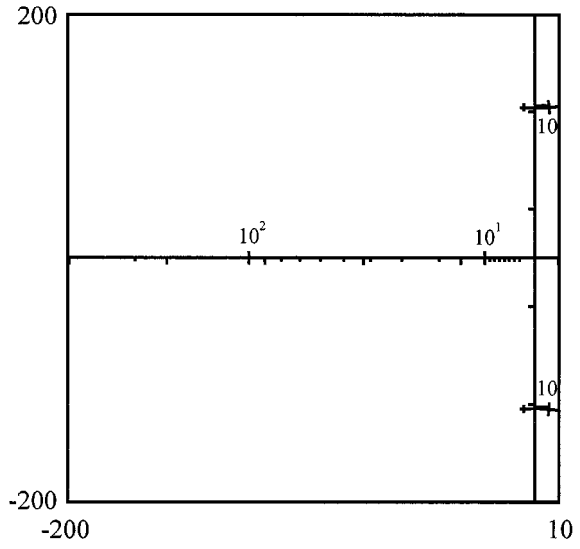

Fig. 12. Standard boost converter root locus.

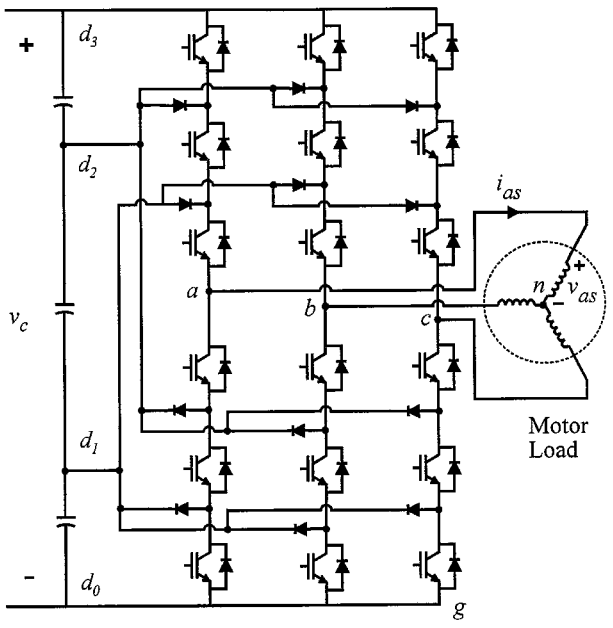

Fig. 13. Four-level inverter topology.

The motor line-to-neutral voltages can be calculated from the line-to-ground voltages by [25].

$$v_{as} = \frac{2}{3}v_{ag} - \frac{1}{3}v_{bg} - \frac{1}{3}v_{cg} \tag{31}$$

$$v_{bs} = \frac{2}{3}v_{bg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{cg} \tag{32}$$

$$v_{cs} = \frac{2}{3}v_{cg} - \frac{1}{3}v_{ag} - \frac{1}{3}v_{bg}. \tag{33}$$

Modulation of the line-to-ground voltages may be accomplished with hysteresis current-regulated control [8] or space-vector modulation [7], [10]. Time— domain-based voltage-source methods such as sine-triangle modulation [11] [12] and

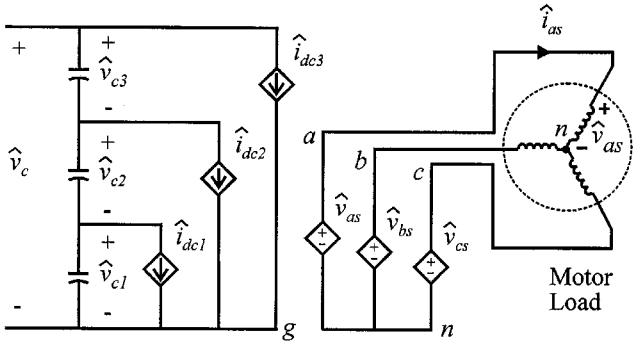

Fig. 14. Average-value model of the four-level inverter.

duty-cycle modulation [26] rely on a three-phase set of duty cycles which may be expressed as

$$d_a = \frac{1}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \tag{34}$$

$$d_b = \frac{1}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{35}$$

$$d_c = \frac{1}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{36}$$

where θ_c is the inverter electrical angle and m is the modulation index which ranges from zero to 1.15 [26].

For the purposes of system model comparison, an NLAM has been developed for the four-level inverter based on the duty cycles. Fig. 14 shows the general structure of the model. Although the derivation of the average voltages and currents is too extensive to be included herein, the general procedure has been described in [26]. The resulting equations are

$$\hat{i}_{\rm dc1} = \frac{9}{2}i_{qs}^{c}\left[C_o - \frac{m}{2}\right] \tag{37}$$

$$\hat{i}_{\rm dc2} = -\hat{i}_{\rm dc1} \tag{38}$$

$$i_{\rm dc3} = \frac{3}{2}i_{qs}^{c}C_o \tag{39}$$

where i_{qs}^{c} is the motor q-axis current in the converter reference frame and

$$C_o = \frac{3m\theta_1}{2\pi} - \frac{1}{\pi}\sin(\theta_1) + \frac{5m}{8\pi}\sin(2\theta_1) - \frac{m}{16\pi}\sin(4\theta_1). \tag{40}$$

In (40), θ_1 is the converter angle where d_a crosses $2/3$ [26]. The average-value motor voltages are

$$\hat{v}_{as} = v_1\cos(\theta_c) \tag{41}$$

$$\hat{v}_{bs} = v_1\cos\left(\theta_c - \frac{2\pi}{3}\right) \tag{42}$$

$$\hat{v}_{cs} = v_1\cos\left(\theta_c + \frac{2\pi}{3}\right) \tag{43}$$

where

$$v_1 = (\hat{v}_{c1} + \hat{v}_{c2} + \hat{v}_{c3})\,C_o + \frac{3m}{2}\,\hat{v}_{c2}. \tag{44}$$

Equations (41)–(43) may be transformed to the converter reference frame for an average-value model with variables that are constant in the steady state [25].

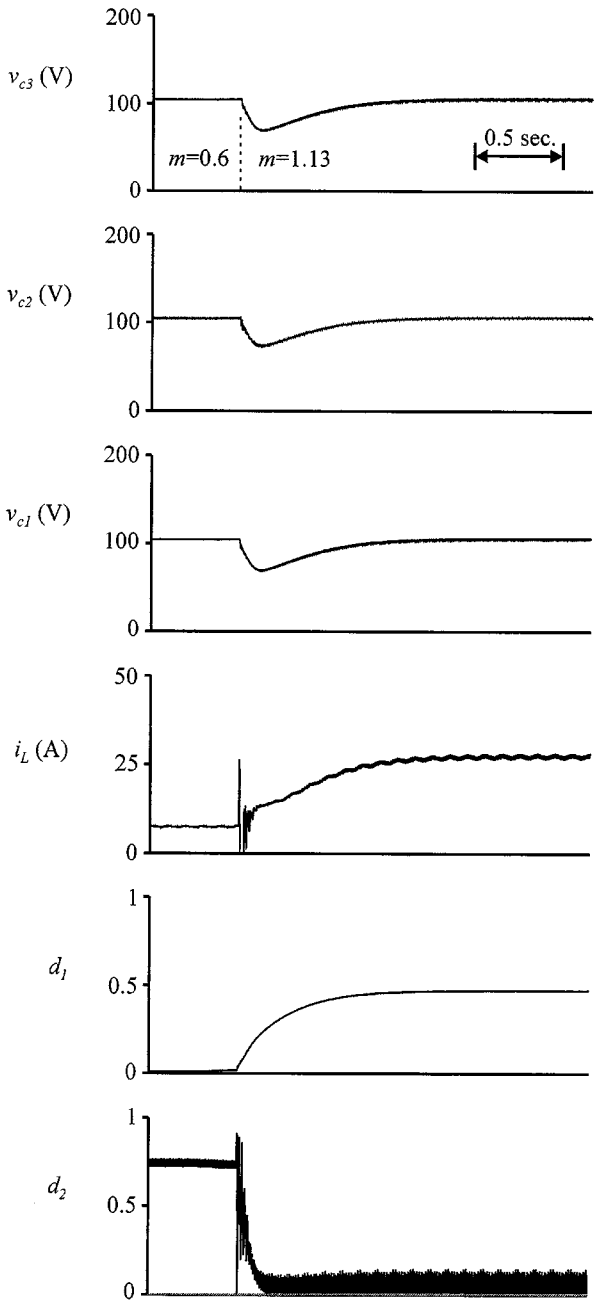

Fig. 15. Detailed model prediction of system performance during a step change in modulation index.

VI. Four-Level System Simulations

Detailed and NLAM-based simulations were performed on the converter/inverter system shown in Fig. 2. The induction motor used in these studies is a 3.7-kW machine [26] operating at a constant speed of 183.3 rad/s and a constant electrical frequency of 60 Hz ensured by setting

$$\theta_c = 2\pi f t \tag{45}$$

in the inverter control. The modulation index m is stepped from 0.6 to 1.13 resulting in a step change in applied voltage on the motor. For the detailed simulation, the PWM switching period is set to $T_s = 0.185$ ms. The commanded converter output voltage v_c^* was set to 318 V. The controller gains for regulating duty cycles d_1 and d_2 were $K_{p1} = 0.001$, $K_{i1} = 0.01$, $K_{p2} = 0.2$, and $K_{i2} = 0.5$. The third duty cycle was set to $d_3 = 0.05$. The dc input voltage was $v_{\rm dc} = 150$ V and the controller switching period was $T_{\rm sw} = 0.1$ ms. The converter inductance value was $L = 10$ mH. The capacitor values were unevenly distributed so that the voltage ripple of all capacitors would be roughly the same in the detailed model. The values used were $C_1 = C_3 = 9900$ μF and $C_2 = 3300$ μF.

Figs. 15 and 16 show the simulation results for the detailed and NLAM models respectively. As can be seen, the capacitor voltages drop when the inverter modulation index is increased. The regulating control on the dc/dc converter then controls the duty cycles so that the capacitor voltages return to their desired values. The inductor current increases as the power to the motor increases. Notice from the detailed model that there are two components to the inductor current ripple. One component is due to the converter switching and the other is due to the capacitor voltage ripple. Figs. 15 and 16 also display the controller duty cycles. Note that for $m = 0.6$, the duty cycle d_1 is very low. This suggests an alternate switching sequence for $m = 0.6$ where the switching state 0 is eliminated and the inductor current ripple is reduced as compared to a standard boost converter.

VII. Four-Level System Laboratory Studies

The proposed four-level drive system shown in Fig. 2 was constructed in the laboratory driving an 18-kW induction motor. The system parameters and operating conditions for this study are shown in Table I.

The input voltage for this study was $v_{\rm dc} = 375$ V and the motor was loaded to rated power resulting in a speed of $\omega_{rm} = 246.8$ rad/s. The switching frequency for the inverter PWM was 5 kHz and the switching frequency for the dc/dc converter was 2.2 kHz. Fig. 17 shows the measured line-to-line motor voltage and line current. Perfect capacitor voltage balance was achieved even though the modulation index was set to 98% of its maximum value. This is evident in the evenly distributed voltage steps in the motor voltage. In the absence of the dc/dc converter, capacitor voltage balance would only be possible for modulation indexes less than 0.6 [13]. Fig. 18 shows the dc/dc converter waveforms. Therein, the switch voltage and inductor current, as defined in Fig. 2, are shown. The controller settles to duty cycles of $d_1 = 0.417$ and $d_2 = 0.065$. The small value of d_2 is noted by the switch voltage shown in Fig. 18. This indicates that a small amount of charge is required to balance the center capacitor voltage.

An additional laboratory study was performed in order to compare the efficiency of the proposed converter to that of a standard two-level converter rated at 1/3 power. For this comparison, a resistive load is used as shown in Fig. 5. Table II shows the parameters and operating conditions for the four- and two-level converters.

The four-level converter operated with an output voltage of $v_c = 614.5$ V and an efficiency of 91.9%. The two-level converter operated with an output voltage of 194 V and an efficiency of 92.3%. The average inductor current was about 25 A in each case. For the four-level converter, this current flows through all

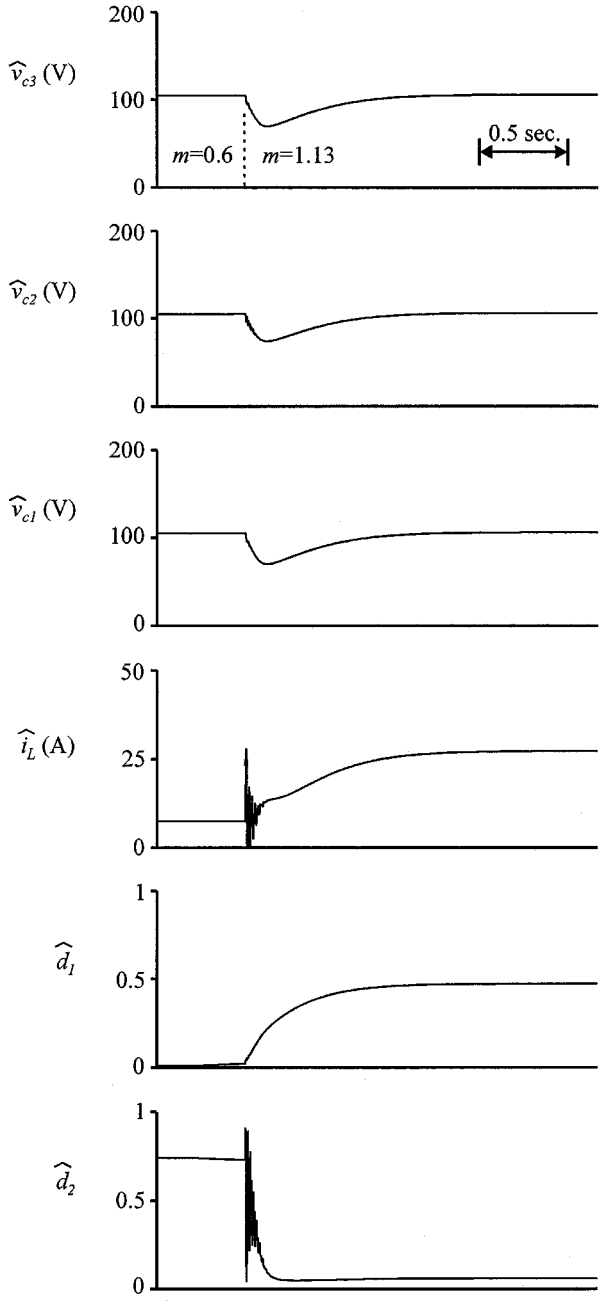

Fig. 16. NLAM model prediction of system performance during a step change in modulation index.

three IGBT's leading to increased conduction losses. However, the output power is three times greater leading to an efficiency that is almost the same as that of the standard two-level converter.

VIII. Conclusion

A novel four-level dc/dc converter has been introduced. The main objective of this converter is to supply a four-level diode-clamped inverter and provide capacitor voltage balancing as well as perform a boost operation. With the capacitor balancing controlled by the converter, the inverter can be operated up to its full output voltage (as compared to 50% of full output voltage when balancing the capacitors with the inverter switching). Steady-state and average-value modeling of the

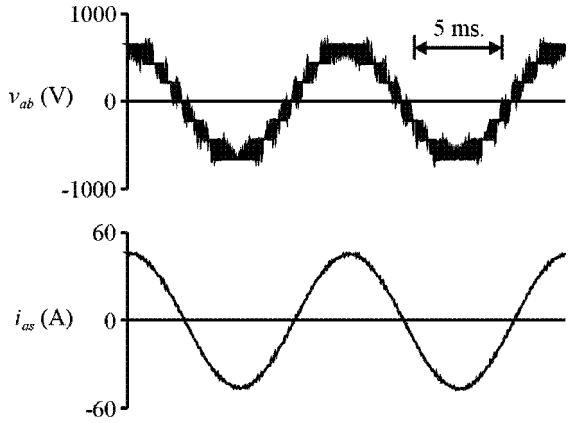

Fig. 17. Four-level inverter laboratory measurements.

TABLE I
Laboratory Drive System Parameters

Motor parameters		
$r_s = 0.2\ \Omega$	$P = 4$	$r_r' = 0.421\ \Omega$
$L_{ls} = 1.91$ mH	$M = 55$ mH	$L_{lr}' = 1.91$ mH
Converter parameters		
$C_1 = C_2 = C_3 = 6200\ \mu$F	$L = 8.7$ mH	
Drive controller parameters		
$m = 1.13$	$f = 80$ Hz	
Converter controller parameters		
$K_{p1} = K_{p2} = 0.001$	$K_{i1} = K_{i2} = 0.1$	
$v_c^* = 660$ V	$d_3 = 0.05$	

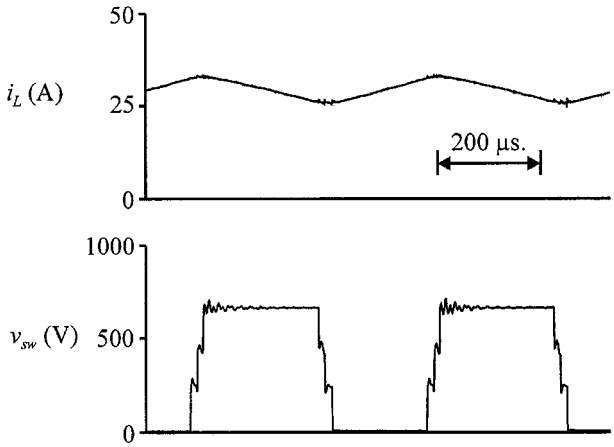

Fig. 18. Proposed converter laboratory measurements.

TABLE II
Laboratory Converter Parameters

Four-level converter	
$R_1 = R_3 = 21.9\ \Omega$	$R_2 = 11.3\ \Omega$
$C_1 = C_2 = C_3 = 6200\ \mu$F	$L = 8.7$ mH
$d_1 = 0.309$	$d_2 = 0.314$
$d_3 = 0.05$	$v_{dc} = 300.6$ V
Two-level converter	
$R = 18.2\ \Omega$	$C = 6200\ \mu$F
$L = 2.9$ mH	$d = 0.518$
$v_{dc} = 100.5$ V	

proposed converter is presented. A simulation study on the converter/inverter system demonstrates that the average-value model prediction compares favorably to a detailed simulation. Laboratory measurements verify the operation of the proposed drive system.

ACKNOWLEDGMENT

The authors express their appreciation to D. E. Delisle at the U.S. Naval Sea Systems Command for partial financial support of this project.

REFERENCES

[1] D. Divan, "Low stress switching for efficiency," *IEEE Spectrum*, vol. 33, pp. 33–39, Dec. 1996.
[2] J. He and N. Mohan, "Parallel resonant DC link circuit—A novel zero switching loss topology with minimum voltage stresses," *IEEE Trans. Power Electron.*, vol. 6, pp. 687–694, Oct. 1991.
[3] R. W. DeDoncker and J. P. Lyons, "The auxiliary resonant commutated pole converter," *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 2, pp. 1228–1335, Oct. 1990.
[4] B. T. Kuhn and S. D. Sudhoff, "Modeling considerations in ARCP versus hard switched drives," in *Proc. Naval Symp. Electric Machines*, July 1997, pp. 161–168.
[5] A. Nabe, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Applicat.*, vol. 17, pp. 518–523, Sept./Oct. 1981.
[6] K. A. Corzine, "Topology and control of cascaded multi-level converters," Ph.D. dissertation, Univ. Missouri, Rolla, MO, 1997.
[7] K. A. Corzine, S. D. Sudhoff, and C. A Whitcomb, "Performance characteristics of a cascaded two-level converter," *IEEE Trans. Energy Conversion*, vol. 14, pp. 433–439, Sept. 1999.
[8] K. A. Corzine and S. D. Sudhoff, "High state count power converters: An alternate direction in power electronics technology," in *Proc. Society of Automotive Engineers Aerospace Power Systems Conf.*, Williamsburg, VA, Apr. 1998, pp. 141–151.
[9] K. A. Corzine, S. D. Sudhoff, E. A. Lewis, D. H. Schmucker, R. A. Youngs, and H. J. Hegner, "Use of multi-level converters in ship propulsion drives," in *Proc. All Electric Ship Conf.* London, U.K., Sept. 1998, vol. 1, pp. 155–163.
[10] Y. H. Lee, B. S. Suh, and D. S. Hyun, "A novel PWM scheme for a three-level voltage source inverter with GTO thyristors," *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 260–268, Mar./Apr. 1996.
[11] R. W. Menzies, P. Steimer, and J. K. Steinke, "Five-level GTO inverters for large induction motor drives," *IEEE Trans. Ind. Applicat.*, vol. 30, pp. 938–944, July/Aug. 1994.
[12] G. Sinha and T. A. Lipo, "A four-level rectifier-inverter system for drive applications," *IEEE Ind. Applicat. Mag.*, vol. 4, pp. 66–74, Jan./Feb. 1998.
[13] M. Fracchia, T. Ghiara, M. Marchesoni, and M. Mazzucchelli, "Optimized modulation techniques for the generalized N-level converter," *Proc. IEEE PESC'92*, vol. 2, pp. 1205–1213, 1992.
[14] N. S. Chio, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Proc. IEEE PESC'91*, Oct. 1991, pp. 96–103.
[15] C. Newton, M. Summer, and T. Alexander, "The investigation and development of a multi-level voltage source inverter," in *Proc. Power Electronics and Variable Speed Drives Conf.*, Sept. 1996, pp. 317–321.
[16] Y. Chen, B. Mwinyiwiwa, Z. Wolanski, and B. T. Ooi, "Unified power flow controller (UPFC) based on chopper stabilized multilevel converter," *Proc. IEEE PESC'97*, vol. 1, pp. 331–337, 1997.
[17] R. Rojas, T. Ohnishi, and T. Suzuki, "PWM control method for a four-level inverter," *Proc. IEE—Elect. Power Applicat.*, vol. 142, no. 6, pp. 390–396, Nov. 1995.
[18] H. Mao, D. Boroyevich, and F. C. Lee, "Multi-level 2-quadrant boost choppers for superconducting magnetic energy storage," in *Proc. IEEE APEC'96*, San Jose, CA, Mar. 1996, pp. 876–882.
[19] J. R. Pinheiro, D. L. R. Vidor, and H. A. Grundling, "Dual output three-level boost power factor correction converter with unbalanced loads," in *Proc. IEEE PESC'96*, Jan. 1996, pp. 733–739.
[20] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Proc. IEEE APEC'95*, Mar. 1995, pp. 434–439.
[21] R. W. Erickson, *Fundamentals of Power Electronics*. London, U.K.: Chapman & Hall, 1997.
[22] S. F. Glover, S. D. Sudhoff, H. J. Hegner, and H. N. Robey, "Average value modeling of a hysteresis controlled DC/DC converter for use in electromechanical system studies," in *Proc. Naval Symp. Electric Machines*, Newport, RI, July 1997, pp. 77–84.
[23] S. D. Sudhoff, K. A. Corzine, S. F. Glover, H. J. Hegner, and H. N. Robey Jr., "DC link stabilized field oriented control of electric propulsion systems," *IEEE Trans. Energy Conversion*, vol. 13, pp. 27–33, Mar. 1998.
[24] G. McPherson and R. D. Laramore, *Electrical Machines and Transformers*. New York: Wiley, 1990.
[25] P. C. Krause, S. D. Sudhoff, and O. Wasynczuk, *Analysis of Electric Machinery*. Piscataway, NJ: IEEE Press, 1995.
[26] K. A. Corzine and S. K. Majeethia, "Analysis of a novel four-level DC/DC boost converter," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Phoenix, AZ, Oct. 1999, pp. 1964–1971.

Keith A. Corzine (S'92–M'93) received the B.S.E.E., M.S.E.E., and Ph.D. degrees from the University of Missouri, Rolla, in 1992, 1994, and 1997, respectively.

In 1997, he joined the University of Wisconsin, Milwaukee, as an Assistant Professor. His research interests include power electronics, motor drives, naval ship propulsion systems, and electric machinery analysis.

Sonal K. Majeethia (S'99) received the B.E. degree in instrumentation and control engineering from Bhavnagar University, Saurashtra, India, in 1995. She is currently working toward the M.S. degree in electrical engineering at the University of Wisconsin, Milwaukee.

In 1995, she joined Bhavnagar University as a Lecturer in the Instrumentation and Control Engineering Department. She is currently with the Automotive and Industrial Electronics Group, Motorola, Northbrook, IL. Her research interests include control and dc/dc power converters.