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A Hysteresis Current-Regulated Control for Multi-Level Drives

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Abstract—Currently, most multi-level converters are controlled through the use of voltage-source based control techniques such as space-vector modulation or multi-level sine-triangle modulation. However, in many applications such as field oriented drives, a high-bandwidth current-source inverter based control is more desirable. In this paper, the concept of a multi-level hysteresis current-source control is set forth. The new control is experimentally verified using a four-level converter / induction motor drive system and the results are compared to a space vector modulation controller. A dynamic study involving a step change in current command demonstrates the controls high bandwidth.

Index Terms—Multi-level converters, space vector modulation, voltage vectors, PWM, three-level converters, hysteresis current-regulated control.

I. INTRODUCTION

THE general trend in power electronics devices has been to switch power semiconductors at increasingly high frequencies in order to minimize harmonics and reduce passive component sizes. However, the increase in switching frequency increases the switching losses which become especially significant at high power levels. Several methods for decreasing switching losses have been proposed, and recently discussed [1], including constructing resonant converters and multi-level converters.

Resonant converters avoid switching losses by adding an LC resonant circuit to the hard switched inverter topology. The inverter transistors can be switched when their voltage is zero, thus reducing switching losses. Examples of this type of converter include the resonant DC link [2], and the auxiliary commutated resonant pole converter [3]. One disadvantage of resonant converters is that the inverter voltage or current peak values are considerably higher than those of corresponding hard switched devices, which increases the required device ratings. In the case of the resonant DC link, the resonant circuit causes the inverter voltage to oscillate between zero and twice the DC source voltage. An additional disadvantage is that the added resonant circuitry will increase the complexity and cost ofthe inverter control.

Multi-level converters offer another approach to reducing switching losses. In particular, these converters offer a high number, of switching states so that the inverter output voltage

can be "stepped" in smaller increments [4],[5],[6]. This allows excellent power quality operation at a low switching frequencies and thus low switching losses. In addition, Electromagnetic Compatibility (EMC) concerns are reduced through the lower common mode current facilitated by lower dv/dt's produced by the smaller voltage steps. The primary disadvantage of these techniques is the large number of active semiconductors required.

Controlling multi-level converters presents an interesting problem since there are a large number of transistor devices to be switched. Most control methods are based on an extension of two-level converter control methods such as space vector modulation (SVM) [4],[7] or sine-triangle modulation [8],[9], [10]. SVM methods involve little hardware, but extensive computation is required especially for converters with a high number of levels. The computation can be performed off-line and the resulting transistor gating signals can be stored in EPROM's [7]. The EPROM storage method, however, does not readily handle dynamically changing values of commanded voltage. Extending sine-triangle modulation to multi-level converters involves using $n - 1$ triangle carrier signals for comparison to the sinusoidal voltage references [8],[9], [10]. Although this control requires analog hardware components, it has the advantage of conceptual simplicity which allows straightforward extension to converters with a large number of levels. Furthermore, dynamically changing values of commanded voltage are automatically handled.

Although these multi-level extensions of both space-vector modulation and sine-triangle modulation provide a means to operate multi-level converters in a voltage-source based mode, it is often desirable to operate these converters in a current-source mode in high bandwidth applications such as field oriented drives [11], [12], [13]. Current-source mode operation also has the advantage of better over-current protection since the currents are directly regulated. The main disadvantage of current-source controls is that the controller does not directly determine the switching frequency. This paper sets forth the concept of a novel current-source hysteresis control for multi-level converters based on an extension of two-level hysteresis control. In the control development, it is assumed that the multi-level converter capacitor voltages are supplied from isolated sources as would be the case in industrial applications where the source is a transformer with several secondary windings or in battery power applications such as electric vehicle or torpedo drives. If the application requires a single DC source, capacitor balancing can be accomplished using the proposed control with the addition of a redundant state selector. For three-level converters capacitor voltage

Fig. 1. Four-level converter topology.

Fig. 2. Voltage vector plot for the four-level converter.
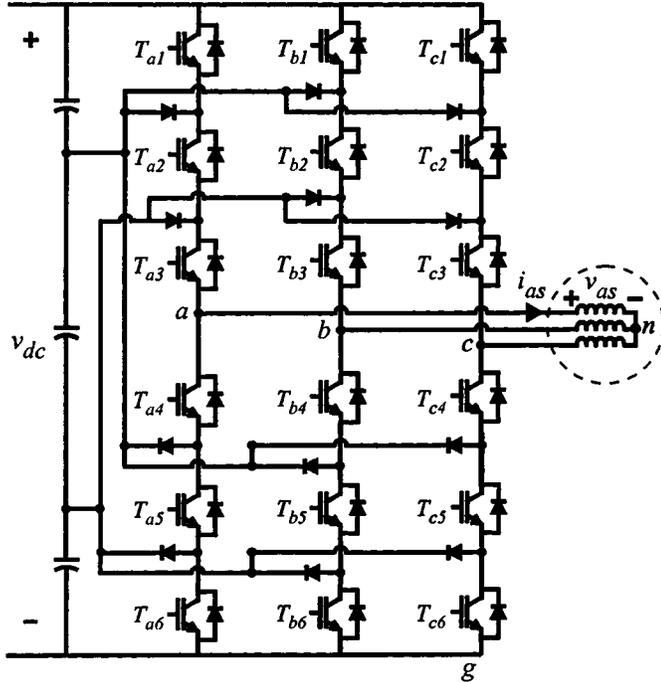
balancing can be achieved over the full range of operation [14]. For four-level drives capacitor balancing is achieved over a limited range of voltage modulation index [5]. The proposed control differs from other proposed multi-level current-regulated control methods for four-level [15], [16] and three level [14], [17] converters in that it does not depend on the machine parameters. The proposed control also differs from another type of current-regulated control [11] in that it is based on the hysteresis principle. Finally, the proposed control differs from most of the previously mentioned methods [11], [15], [16], [17] in that it is expenmentally verified.

II. MULTI-LEVEL CONVERTERS

Although any number of levels are possible, multi-level converters will be described using the four-level converter topology shown in Fig. 1. Therein, the capacitors split the dc rail voltage allowing four different voltage levels to be selected for the phase-to-ground voltages v_{ag}, v_{bg}, and v_{cg} depending on the inverter gating signals. For example, the voltage v_{ag} will be 0 if transistors T_{a4} through T_{a6} are gated on, $\frac{1}{3}v_{dc}$ if transistors T_{a3} through T_{a5} are gated on, $\frac{2}{3}v_{dc}$ if transistors T_{a2} through T_{a4} are gated on, and v_{dc} if transistors T_{a1} through T_{a3} are gated on. In general for an n-level inverter, the phase-to-ground voltages can be expressed as

$$v_{xg} = \frac{l_x}{(n-1)} v_{dc} \quad l_x = 0, 1, \ldots (n-1) \quad (1)$$

where x represents the phase which can be a, b, or c, and l_x represents the phase level selected by the gating signals as described above. For the purpose of discussing the multi-level converter, it is convenient to define the switching state as a function of the phase-to-ground voltage levels. In particular,

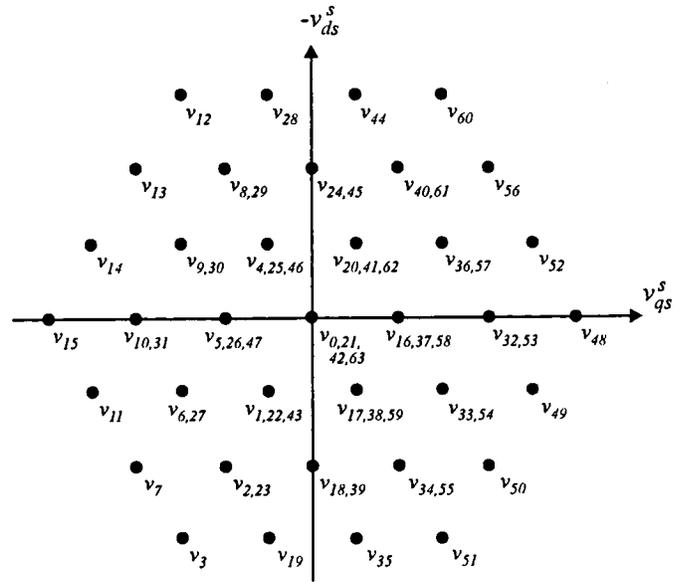$$sw = (n)^2 l_a + (n)^1 l_b + (n)^0 I_c. \quad (2)$$

The number of possible switching states for a multilevel converter is given by

$$n_{sw} = (n)^p. \quad (3)$$

where p is the number of phase legs. For the three-phase four-level converter, the number of possible switching states is $n_{sw} = 64$.

The voltage applied to the machine stator winding can be calculated in the same manner as with a standard six-transistor inverter since the machine connections to the inverter are the same, and the machine is wye connected. The stator voltages are thus given by [18]

$$v_{as} = \frac{2}{3} v_{ag} - \frac{1}{3} v_{bg} - \frac{1}{3} v_{cg} \quad (4)$$

$$v_{bs} = \frac{2}{3} v_{ag} - \frac{1}{3} v_{ag} - \frac{1}{3} v_{cg} \quad (5)$$

$$v_{cs} = \frac{2}{3} v_{cg} - \frac{1}{3} v_{ag} - \frac{1}{3} v_{bg}. \quad (6)$$

The stator voltage vectors achievable from the switching states can be plotted by transforming the a- b- and c-phase stator voltages to the q- and d-axis stationary reference frame. The transformation to the arbitrary reference frame is given by [18]

$$v_{qs}^s = \frac{2}{3} \left(v_{as} \cos(\theta) + v_{bs} \cos\left(\theta - \frac{2\pi}{3}\right) + v_{cs} \cos\left(\theta + \frac{2\pi}{3}\right) \right) \quad (7)$$

$$v_{ds}^s = \frac{2}{3} \left(v_{as} \sin(\theta) + v_{bs} \sin\left(\theta - \frac{2\pi}{3}\right) + v_{cs} \sin\left(\theta + \frac{2\pi}{3}\right) \right). \quad (8)$$

In the stationary reference frame, θ is zero.

Fig. 2 depicts the plot of the stator voltage vectors for the four-level converter. Each vector is numbered v_{sw} where sw
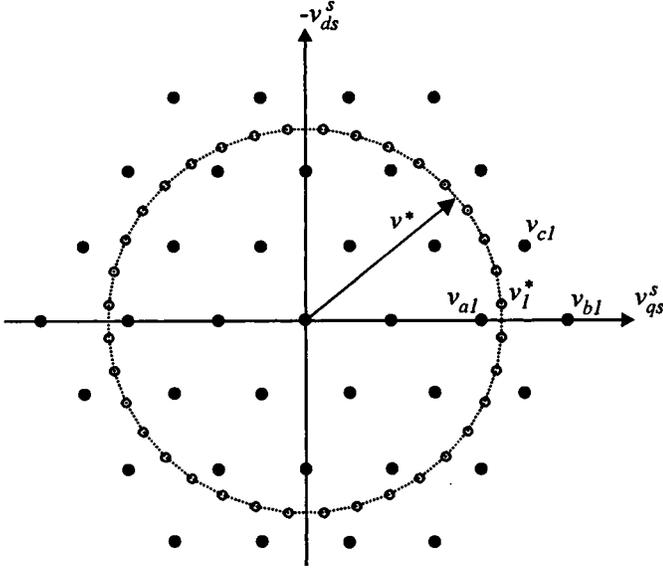
Fig. 3.   Space vector modulation for the four-level converter.

is the switching state which will produce the voltage vector. The phase-to-ground voltages can be determined for a particular voltage vector in Fig. 2 by converting the switching state number sw into base four mathematics (or base n in general for the n-level converter). For example, switching state $sw = 60$ is 330 in base four. Switching the a-phase to level $l_a = 3$, the b-phase to level $l_b = 3$, and the c-phase to level $l_c = 0$ will produce the switching state $sw = 60$. As can be seen, there are only 37 unique voltage vectors produced from the 64 switching states due to switching state redundancy.

III. MULTI-LEVEL SPACE VECTOR MODULATION

The SVM method consist of pulse width modulation (PWM) switching to the available voltage vector in the q-d stationary plane in order to approximate a commanded voltage vector. Fig. 3 shows the voltage vector diagram for a four-level converter along with the complex time-varying commanded voltage vector v^* which follows the path indicated by the circle. Although the path could be arbitrary, a circular commanded voltage vector is chosen in the q-d plane since it results in balanced three-phase sinusoidal voltages in the time domain. Under these conditions, the commanded voltage vector is defined by

$$v^* = \sqrt{2}v_s e^{j\omega_e t} \tag{9}$$

where v_s is the rated RMS value of the stator voltage and ω_e is the rated electrical frequency in radians per second.

The first step in the space vector modulation strategy is to approximate the commanded voltage vector by the discrete vector

$$v_k^* = \sqrt{2}v_s e^{j(\frac{2\pi}{pn}k + \frac{2\pi}{pn})} \qquad k = 1, 2, \ldots pn. \tag{10}$$

In (10), pn is the number of discrete voltage vectors per cycle and is referred to as the pulse number. In Fig. 3, the pulse number is 36 and the discrete voltage vectors v_k^* are represented by the open circles along the path of the commanded voltage.

Since there are pn discrete vectors in one cycle of the fundamental frequency ω_e, the portion of time allocated by the controller for each discrete vector v_k^* is

$$t_s = \frac{2\pi}{pn * \omega_e}. \tag{11}$$

This time shall be referred to as the sampling time.

The next step is to approximate each discrete commanded voltage vector by PWM switching to the nearest three voltage vectors [19]. In Fig. 3 for example, to approximate the vector v_1^*, the PWM switching is done between the three nearest vectors labeled v_{a1}, v_{b1}, and v_{c1}. The times spent at each vector must be computed so that the fast average of the switching of the three vectors is the desired vector v_k^* or

$$t_{ak}v_{ak} + t_{bk}v_{bk} + t_{ck}v_{ck} = t_s v_k^*. \tag{12}$$

The total time spent to approximate the vector v_k^* is the sampling time

$$t_s = t_{ak} + t_{bk} + t_{ck}. \tag{13}$$

Writing the real and imaginary parts of (12) along with (13) in matrix form yields

$$\begin{bmatrix} \text{Re}(v_{ak}) & \text{Re}(v_{bk}) & \text{Re}(v_{ck}) \\ \text{Im}(v_{ak}) & \text{Im}(v_{bk}) & \text{Im}(v_{ck}) \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_{ak} \\ t_{bk} \\ t_{ck} \end{bmatrix} = \begin{bmatrix} t_s\text{Re}(v_k^*) \\ t_s\text{Im}(v_k^*) \\ t_s \end{bmatrix}. \tag{14}$$

Equation (14) can be solved for t_{ak}, t_{bk}, and t_{ck} given the commanded voltage vector and the three nearest voltage vectors.

The order in which to switch from one nearest voltage vector to another can selected to minimize the switching frequency [19], avoid narrow transistor gating signals [4], or balance the input capacitor voltages [4], [5]. The sequence used herein involves switching to v_{ak} then v_{bk} then v_{ck} then v_{ak} (abbreviated as $v_{ak} - v_{bk} - v_{ck} - v_{ak}$). For this sequence, the time t_{ak} must be split since the converter is switched to the vector v_{ak} twice. The time can be split evenly or as a function of the angle of v_k^*. It has been shown for two-level converters that the way that t_{ak} is split has a noticeable effect on the resulting waveforms [20]. For the studies considered herein, the time t_{ak} is split evenly. The transistor gating signals are determined from the switching sequences and switching times.

The switching time and gating signal calculations can be determined on-line using a fast microcomputer or computed off-line and stored in the controllers available memory. The advantage of computation on-line is that flexibility is provided for obtaining arbitrary values of commanded voltage v^*, although an approximate method for incorporating an arbitrary commanded voltage using controller memory storage has been proposed [7]. The advantage of storing the computations in controller memory is that hardware construction is simpler. For the comparisons that follow, the PWM switching sequences are computed off-line and the transistor gating signals are stored in EPROM's for a fixed value of commanded voltage magnitude.

IV. MULTI-LEVEL HYSTERESIS CURRENT-REGULATION

The objective of standard two-level hysteresis current-regulated control is to switch the inverter transistors in a particular phase so that the current in that phase tracks a reference current
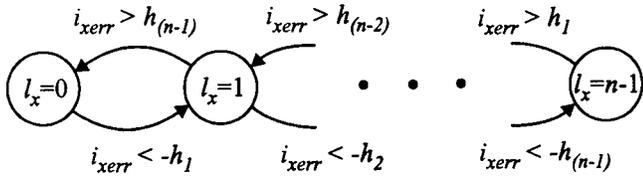
Fig. 4.   Switching state diagram for the n-level hysteresis current-regulated control.

i_{xs}^* within a specified tolerance or hysteresis level [12]. If the phase current becomes greater than the reference current by an amount equal to the hysteresis level h, the phase is switched to its lowest level $l_x = 0$ in order to decrease the current. Likewise, if the phase current becomes less that the reference current by a value of h, the phase is switched to its highest level $l_x = 1$ in order to increase the current. The reference currents for the a- b- and c-phase i_{abcs}^* are typically determined in the q-d synchronous reference frame by a supervisory control and transformed to machine variables.

The extension of the two-level hysteresis control algorithm to the multi-level case is based on defining a set of $n-1$ hysteresis levels. Denoting the maximum allowable excursion of the actual current from the desired current as the hysteresis level $h_{(n-1)}$, the remaining $n-2$ hysteresis levels are computed from

$$h_i = \frac{i}{(n-1)} h_{(n-1)} \qquad i = 1, 2, \ldots, (n-2). \qquad (15)$$

As with the two-level hysteresis control, the switching for a particular phase is governed by that phase's current error which is defined by

$$i_{xerr} = i_{xs}^* - i_{xs}. \qquad (16)$$

When the current error is positive, the controller decreases the level of phase x by one each time the error crosses a hysteresis level. Likewise, the phase level is increased when the current error is negative and crosses a hysteresis level. The general n-level switching state diagram for this operation is shown in Fig. 4. In hardware, this switching state diagram is implemented, for each phase, using several operational amplifiers [21]. The switching principle of Fig. 4 is demonstrated in Fig. 5 which shows the idealized reference and actual a-phase currents of a four-level converter. The a-phase voltage level is shown to illustrate the converter switching. Note that, as presented, the n-level hysteresis control reduces to the two-level case.

From Fig. 4, it can be seen that smaller hysteresis switching cycles are possible (such as switching between $l_x = 0$ and $l_x = 1$). These smaller switching cycles cause a slight current error. For systems where the current commands are dependent on the machine variables, such as field oriented controllers [22], an additional control loop must be added to correct for the error. The synchronous current regulator [23] shown in Fig. 6 implements the required corrective action. Therein, i_{qs}^{e*} and i_{ds}^{e*} represent the commanded currents in the q-d synchronous reference frame determined by a supervisory control such as a field oriented controller. These currents are compared to the measured q- and d-axis currents which are computed from the measured machine variable currents by the transformation K_s^e [18]. The current errors actuate integral controls which determine the ref-
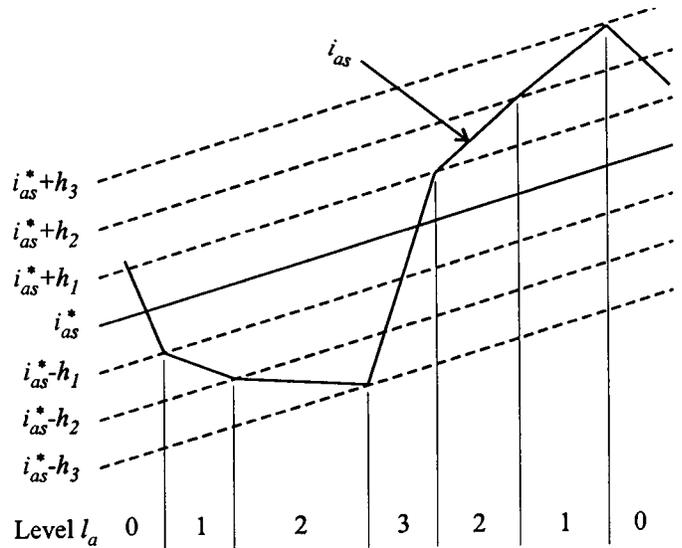

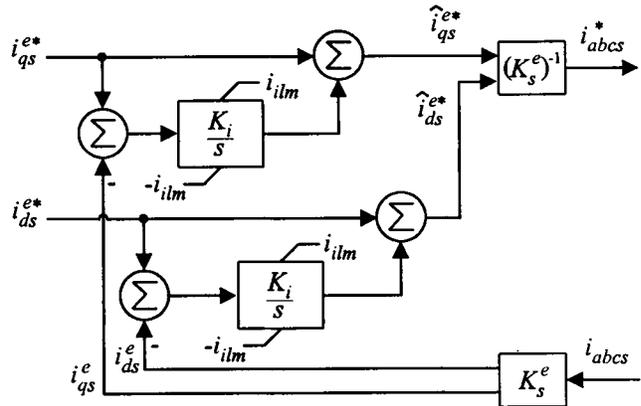Fig. 5.   Operation of the four-level hysteresis current-regulated control.

Fig. 6.   Synchronous current regulator.

erence currents $\hat{i}_{qs}^{e*}$ and $\hat{i}_{qs}^{e*}$. The integral controls must be limited in order to avoid windup in situations where the error does not go to zero in the steady-state. The reference currents are transformed to machine variables to produce the reference currents i_{abcs}^* required by the hysteresis control. When implementing the synchronous current regulator, it is important to set the integral gain K_i so that the added control loop does not significantly effect the system dynamics. Note that the integral control attenuates signals that are higher than K_i rad/sec. Since the integral control should not operate on the high-frequency switching of the hysteresis control reflected in the measured and axis currents, it is important to set K_i to a frequency much lower than that of the hysteresis current regulator switching frequency. With the gain selected as mentioned, the synchronous current regulator will trim out the current error without effecting the system dynamic performance. Simulation results on a four-level / induction motor drive system indicate that the synchronous current regulator reduces the current error from 2.4% to zero.

V. EXPERIMENTAL VERIFICATION

The four-level SVM and hysteresis controls were tested and compared using a laboratory system consisting of a

Table I. 3.7 kW induction machine parameters.	
$P = 4$	$L_m = 64.43$ mH
$r_s = 0.3996\ \Omega$	$L_{ls} = 5.73$ mH
$r'_r = 0.3996\ \Omega$	$L'_{lr} = 4.64$ mH
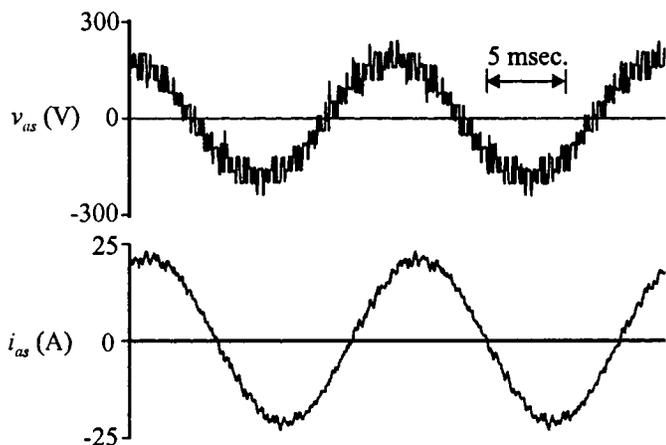
Fig. 7. Four-level converter performance using SVM control.

Fig. 8. Voltage vectors utilized by the SVM control.

reconfigurable IGBT converter and a 4-pole 3.7 kW induction machine with the parameters listed in Table I. The dc capacitor voltages were supplied from isolated rectified three-phase sources. For the studies presented herein, the SVM control technique was used to create phase voltage waveforms with a 60 Hz, 187.8 V peak fundamental component. For the hyseteresis control, a sinusoidal reference current waveform was used without the synchronous current regulator. The magnitude of the hysteresis control reference cunent was set so that the resulting RMS current matched that of the SVM control (14.4A). The induction machine was operated at a speed of 183.3 rad/sec. In order to provide a baseline for comparison of the two control methods, the current THD was set to 5.8% by settling the pulse number of the SVM control to 36 and the hysteresis level of the hysteresis control to 1.6A.

Figs. 7 and 8 show the *a*-phase induction motor waveforms and the voltage vectors utilized respectively for the system using SVM control. Figs. 9 and 10 show the same waveforms and vector plots for the system using hysteresis current-regulated control. It should be pointed out that these waveforms are measured directly at the output of the inverter without additional power filtering circuitry, however, this filtering could be added [24]. In the case of the voltage vectors utilized, the plots are determined for one 60 Hz cycle. As expected, the voltage waveform of the SVM control is more regular than that for the hysteresis control since the voltage vectors are computed off-line whereas the hysteresis control switching depends on the current error. It can be seen from the voltage vector plots that the converter sometimes appears to switch to vectors that are not possible considering the voltage vector plot of Fig. 2. This is due to measurement noise which not generated to the control algorithm. It should also be pointed out that the vectors are slightly
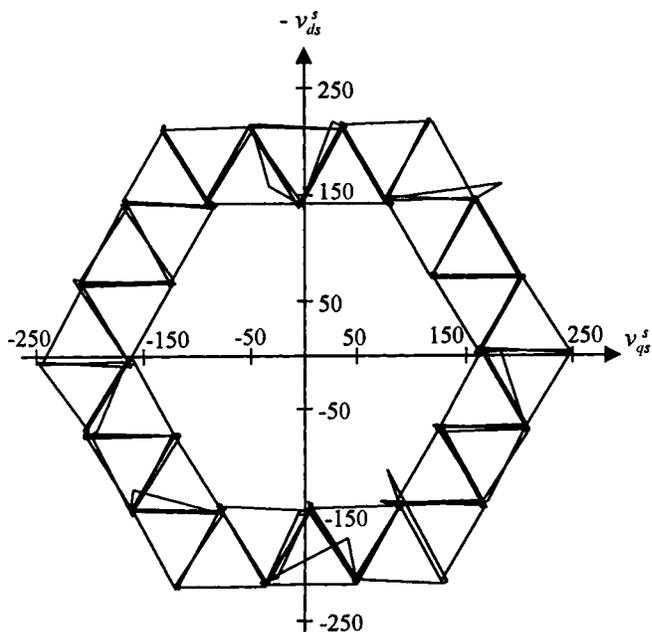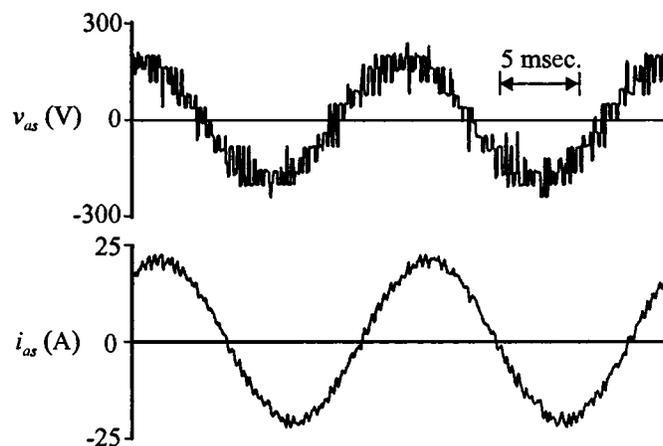

Fig. 9. Four-level converter performance using hysteresis current regulation.

displaced from their expected positions due to semiconductor voltage drops that were not taken into account when producing Fig. 2. Table II shows the voltage THD's and switching frequencies of the two control methods. The THD was determined by storing the waveforms on a digital oscilloscope and evaluating the THD using [12]

$$\text{THD}(v_{as}) = \frac{\sqrt{v_{as}^2 RMS - v_{as1}^2}}{v_{as1}} \qquad (17)$$

where $V_{as}RMS$ and v_{as1} are the RMS value and fundamental component of the voltage waveform respectively. The switching frequencies are listed in order of $T_{a1}/T_{a3}/T_{a5}$. The switching frequencies of the transistors T_{a2}, T_{a4}, and T_{a6} are identical to those of transistors T_{a5}, T_{a1}, and T_{a3} respectively.

In the case of the hysteresis control the switching is not predetermined and the switching frequencies were computed by averaging over six cycles. It is interesting to observe that the switching frequencies of the hysteresis control are lower
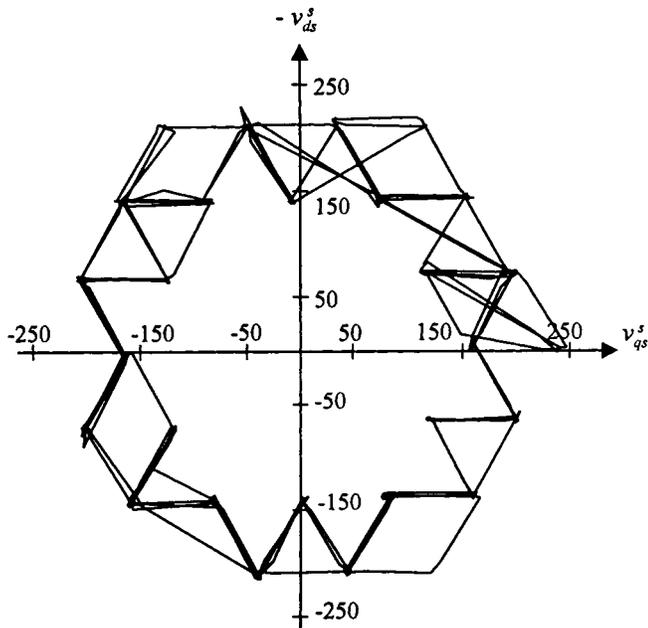
Fig. 10.   Voltage vectors utilized by hysteresis current regulation.

TABLE II
CONTROLLER PERFORMANCE MEASUREMENTS

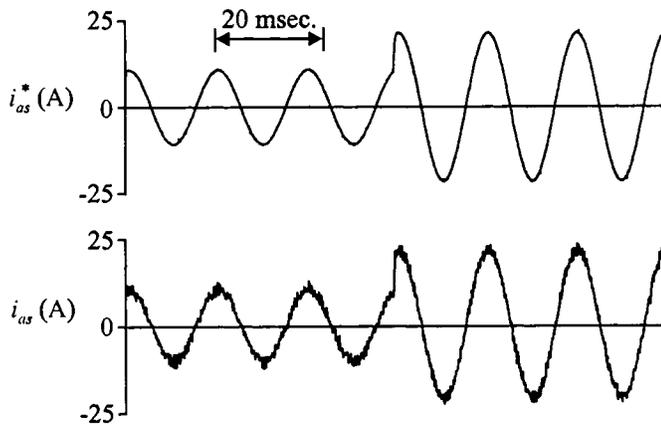| Table II. Controller performance measurements.		
	THD(v_{as})	f_{sw} (Hz)
SVM	23.7 %	600 / 400 / 600
Hysteresis	25.2 %	530 / 160 / 535

Fig. 11.   Hysteresis current regulation performance during a step change in commanded current.

than those of the SVM control although the voltage and current THD's are similar.

In order to demonstrate the high bandwidth feature of hysteresis current-regulated control the controller performance was tested with a step change in current command. Fig. 11 shows the a-phase commanded and measured current of the induction motor drive system when the current command is stepped from half rated value to full rated value (14.4 Arms). As can be seen, the control has excellent response to the step input.

VI. CONCLUSION

A new type of multi-level control is proposed which involves extending hysteresis current-regulation to the n-level converter. Although the control is implemented using analog circuitry (as compared to the digitally implemented SVM method), it has the advantage of conceptual simplicity. This is especially important for converters with a high number of voltage vectors. The control was verified experimentally using a four-level converter / induction machine drive and compared to the SVM technique. It was found that the hysteresis control had a slightly higher voltage THD but a lower switching frequency than the SVM control for the same amount of current THD. It was also shown that the proposed control has fast dynamic response to a step change in current command which is characteristic of two-level hysteresis current controllers.

ACKNOWLEDGMENT

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