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Recommended Citation
Choi, Jong Hyuni; Kim, Chang-Soo; Lim, Byung Cheon; and Jang, Jin, "A novel thin film transistor using double amorphous silicon active layer" (1998). Faculty Research & Creative Works. Paper 463.
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A Novel Thin Film Transistor Using Double Amorphous Silicon Active Layer

Jong Hyun Choi, Chang Soo Kim, Byung Cheon Lim, and Jin Jang

Abstract—We have fabricated a novel low off-state leakage current thin-film transistor (TFT) using a chlorine incorporated amorphous silicon [a-Si:H(Cl)] and amorphous silicon (a-Si:H) stacked active layer, in which conduction channel is formed in a-Si:H and a-Si:H(Cl) is photo-insensitive material. The off-state photo-leakage current of the a-Si:H(Cl)/a-Si:H TFT is much lower than that of a conventional a-Si:H TFT.

I. INTRODUCTION

Thin-film transistors (TFTs) including an active layer of hydro-genated amorphous silicon (a-Si:H) or polycrystalline silicon have been widely employed as the pixel-driving elements of a liquid crystal display (LCD). Particularly, the a-Si:H TFT is widely used in the production of large screen displays [1]. When employing a-Si:H TFT for multimedia displays which require a high intensity backlight compared to conventional notebook personal computers, the main issue is to reduce the off-state leakage current under light illumination.

A-Si:H has high photoconductivity which results in a high off-state leakage current for an a-Si:H TFT under backlight illumination [2].

Cl incorporated hydrogenated amorphous silicon [a-Si:H(Cl)] has been prepared by various deposition methods using SiH$_2$Cl$_2$ mixtures to improve film quality [3], to improve the stability [4], or to increase the deposition rate [5].

The off-state leakage current of a-Si:H TFT under light illumination is related with its photoconductivity. The photoconductivity of a-Si:H(Cl) is at least two orders of magnitude lower than that of undoped a-Si:H [6]. However, the performance of the a-Si:H(Cl) TFT’s was found to degrade with increasing [SiH$_2$Cl$_2$]/[SiH$_4$] ratio which was used to deposit the a-Si:H(Cl) [7]. The degradation

Manuscript received November 19, 1997; revised April 30, 1998. The review of this brief was arranged by Editor K. Shenai. This work was supported by the G-7 project of Korea and the Korea Science and Engineering Foundation through the Semiconductor Physics Research Center. The authors are with the Department of Physics, Kyung Hee University, Seoul 130-701, Korea (e-mail: jjang@kms.kunghee.ac.kr).
structure. It is noted that the a-Si:H TFT exhibited a field effect mobility of 0.5 cm²/Vs, and a threshold voltage of 3.80 V.

Fig. 3 shows the comparison of the $I_d$--$V_d$ characteristics between an a-Si:H TFT, an a-Si:H TFT, and conventional a-Si:H TFT under backlight illumination. The On/Off current ratios of an a-Si:H TFT, an a-Si:H TFT, and conventional a-Si:H TFT are $5.45 \times 10^{-2}$, $4.63 \times 10^{-7}$ and $1.18 \times 10^{-2}$, respectively. The on-current of the a-Si:H TFT is slightly less than that of a-Si:H TFT. However, the leakage current is much lower than that of a conventional a-Si:H TFT. It is noted that the a-Si:H TFT exhibited lowest photo-leakage currents, whereas the off-state dark leakage currents increase rapidly with decreasing gate voltage at $V_{gs} < -15$ V. The rapidly increasing off currents appear to be presumably due to the less density of states in the gap below the midgap of a-Si:H TFT.

Fig. 4 shows the field effect mobility and threshold voltage as a function of a-Si:H thickness for the a-Si:H TFT’s. The off-state drain current of an a-Si:H TFT decreases if the conductivity activation energy increases because the drift mobility of hole is much less than that of electron [9].

IV. CONCLUSION

We have fabricated low off-state leakage current TFT’s using a stack with Cl incorporated amorphous silicon [a-Si:H(Cl)] and amorphous silicon (a-Si:H) as the active layer. The field effect mobility and threshold voltage of the a-Si:H TFT’s are better than those of a-Si:H TFT’s. The a-Si:H(Cl)/a-Si:H TFT’s exhibited a field effect mobility of 0.45 cm²/Vs, a threshold voltage of 5.09 V, and an on/off current ratio of $>10^7$. The off-state leakage currents of a-Si:H(Cl)/a-Si:H TFT under front as well as backlight illumination are much lower than those of conventional a-Si:H TFT’s. By adopting a-Si:H(Cl)/a-Si:H as an active layer in a TFT, the photo-leakage current can be decreased with only a small degradation in field effect mobility.

REFERENCES


Improved Output ESD Protection by Dynamic Gate Floating Design

Hun-Hsien Chang and Ming-Dou Ker

Abstract—A dynamic gate floating design is proposed to improve ESD robustness of the CMOS output buffers with small drive capability. By using this novel design, the human-body-model (machine-model) ESD failure threshold of a 2-mA CMOS output buffer has been practically improved from 1 KV (100 V) to greater than 8 KV (1500 V) in a 0.35-μm CMOS process.

Index Terms—ESD, ESD protection, output buffer.

I. INTRODUCTION

Electrostatic discharge (ESD) robustness of CMOS IC’s had been found to be seriously degraded by the advanced deep-submicron CMOS technologies [1]–[3]. To improve ESD robustness of the output transistors, the ESD-implant process and the silicide-blocking process had been widely used in the deep-submicron CMOS technologies [3]–[5]. Besides the advanced process modifications to improve ESD robustness of the output buffers, the symmetrical layout structure had been emphasized to realize the large-dimension output transistors by ensuring the uniform turn-on phenomenon along the multiple fingers of the output transistor [6]. To further enhance the uniform turn-on phenomenon among the multiple fingers of the output transistors, a gate coupling design had been reported to achieve uniform ESD power distribution on the large-dimension output transistors [7]–[11]. But in the practical applications, the output buffers in a cell library have different drive capability specifications, for example, 2, 4, 8, …, 24 mA, etc. But, the cell layouts of the 2-mA output buffer, it also found to be seriously degraded by the advanced deep-submicron CMOS process [12].

Fig. 1. The output buffer with a small drive capability in a 0.35-μm CMOS process. The gate of the unused Mn2 (Mp2) is connected to VSS (VDD) through a small-dimension Mdn1 (Mdp1) to perform the traditional gate coupling effect for ESD protection.

In this paper, a dynamic gate floating design is proposed to improve ESD level of the output buffers with different drive capabilities in a 0.35-μm CMOS process [12].

II. OUTPUT ESD PROTECTION DESIGN

A. Traditional Gate Coupling Design

To enhance the turn-on uniformity of the output buffers, the poly gates of the unused NMOS (PMOS) in the output buffers are connected to VSS (VDD) through a small-dimension NMOS Mdn1 (PMOS Mdp1) [10], as shown in Fig. 1. The Mdn1 (Mdp1) cooperated with the parasitic drain-to-gate capacitance in the Mn2 (Mp2) performs the gate coupling effect to turn on the Mn2 (Mp2) during the ESD stress [9]–[11]. In the normal operating conditions, the gate of Mdp2 (Mn2) is connected to VDD (VSS) through the turned-on Mdp1 (Mdn1) to keep the Mp2 (Mn2) off. The output drive (sink) current is provided by the Mp1 (Mn1). For an output buffer with a smaller drive capability, such as only 2mA, the device dimension of the Mn1 (Mp1) is much smaller than that of the Mn2 (Mp2). In a 0.35-μm CMOS CMOS cell library, a 2-mA output buffer has the device dimension (W/L) of 30/0.5 (690/0.5) for both the Mn1 and Mp1. But, in the cell layout of the 2-mA output buffer, it also has the device dimension of 450/0.5 (690/0.5) for the Mn2 (Mp2). The gate to drain contact distance is the Mn2, Mp2, Mn1, and Mp1.

Fig. 2. The dynamic gate floating design to improve ESD level of the output buffers with small drive capability in a 0.35-μm CMOS process.