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A Study on Influence of Guard Band on Common-Mode Current Related to a Microstrip Line

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Abstract:
Influence of guard band on common-mode (CM) current related to a microstrip line (trace) has been studied experimentally and with FDTD simulation. As the guard band, copper tape is connected along the entire edge of the ground plane. It is cleared that a guard band parallel to and near a trace is most effective in suppressing the CM current. An empirical formula to quantify the relationship between the position of a trace and CM current with a guard band is proposed.

II. Experimental and Modeling Methods
II-A. PCB Geometry
The geometry of a PCB layout is illustrated in Fig. 1. The geometry of a PCB layout is illustrated in Fig. 1. The size of PCB is 150 mm length, 100 mm width, and 1.09 mm thickness of the dielectric substrate with $\varepsilon_r = 4.5$. The trace, with 0.508 mm width and 50 mm length was centered lengthwise on a dielectric substrate. Several different configurations in which the distance $d$, between the trace and the PCB edge, as shown in Table 1, were prepared for the measurements. As the guard band, copper tape is used and connected along the entire edge of the ground plane to upper layer through the side of the PCB. The width $w_{GB}$ of the guard band was 5 mm. The characteristic impedance of the case with guard band was the same as the case without guard band. The terminating resistance was the same value as the characteristic impedance determined from TDR measurements, as shown in Table 1. The PCB was driven by a 0.085"-semi-rigid coaxial cable running along the center of the PCB on the reverse-side. The coaxial cable extended 30 mm beyond the PCB edge and an SMA connector was used for the driving point of the signal trace.

II-B. Experimental Method
The CM current on the outer shield of the feed cable was measured using a current probe (Fischer F-2000), and a network analyzer (HP 8753D), as shown in Fig. 2 [6]. A 600 mm×600 mm aluminum plate was used to isolate the PCB from the cable dressing leading to the network analyzer. The $S_{21}$ with the location of Port 1 (the voltage source for the signal trace) and Port 2 (current probe on the semi-rigid cable) was measured in the frequency range from 50 MHz to 1 GHz. The calibration of the network analyzer and the current probe were done by using a shorted copper ring which encircled the current probe. The voltage at Port 2 is related to the CM current by $|V_2| = 50|I_{CM}|/2$, where the source impedance of the network analyzer is 50 ohm. The input voltage at Port 1 is $|V_1| = |V_2|/2$, where $V_2$ is the source voltage of the network analyzer. Since the source impedance is matched to the characteristic impedance of the cable. Since $|S_{21}|$ is the ratio of the voltage at Port 2 to the voltage at Port 1, the relationship between the $|S_{21}|$ and CM current is given by

$$|S_{21}| = \frac{50|I_{CM}|}{|V_2|}. \quad (2)$$

Equation (2) is used to compare experimental and numerical results.
Fig. 1 Geometry of PCB layout used in the experimentation.

Table 1 PCBs under test

<table>
<thead>
<tr>
<th>d1 [mm]</th>
<th>d1/(s)</th>
<th>guard band</th>
<th>Terminating resistor [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>d50</td>
<td>1.27</td>
<td>0.025</td>
<td>100</td>
</tr>
<tr>
<td>d100</td>
<td>2.54</td>
<td>0.051</td>
<td>100</td>
</tr>
<tr>
<td>d250</td>
<td>6.35</td>
<td>0.127</td>
<td>100</td>
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<tr>
<td>d300</td>
<td>7.62</td>
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<td>91</td>
</tr>
<tr>
<td>d400</td>
<td>10.16</td>
<td>0.203</td>
<td>91</td>
</tr>
<tr>
<td>d400GB</td>
<td>15.24</td>
<td>0.305</td>
<td>91</td>
</tr>
<tr>
<td>center</td>
<td>49.75</td>
<td>0.995</td>
<td>91</td>
</tr>
<tr>
<td>centerGB</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

II-C. Method of FDTD Modeling

The FDTD method [8] is used for simulating CM current on the PCB. Fig. 3 shows the computational domain, as a typical example. The cell size was Δx=0.254, Δy=2.5 and Δz=0.546 mm. PMLs (Perfectly Matched Layers) of eight cells deep, were used as the absorbing boundary condition. The total computational domain was 491x114x183 cells, in the x, y, and z dimensions, respectively. The time step was Δt=6.35x10⁻¹³ s from the Courant stability condition [8]. The trace, the ground plane, and aluminum plate were modeled as PEC (Perfect Electric Conductor). The aluminum plate was included as an infinite ground plane. The PCB substrate was modeled as a dielectric with two cells deep and relative permittivity εr=4.5. A sinusoidally modulated Gaussian pulse was used as the source with source resistance 50 Ω. The CM current was calculated by the loop integral of the magnetic field around the cable at the current probe position. To shorten the calculation time, the vector and parallel computation method for a super computer SX-4 (NEC) was developed [9].

III. Influence of the guard band on the CM current

At first, the PCB without guard band is discussed. The |S21| related to CM current is shown in Fig. 4. As the trace is moved closer to the PCB edge, |S21| increases. The curve is shifted nearly uniformly in magnitude over the considered frequency range. The difference between “center” and “d50” is approximately 12 dB. The calculated and measured results are in good agreement.

So far, a formula for the inductance $L_{CM} [\text{nH/cm}]$ of the PCB ground plane without guard band was derived analytically by Leone, as

$$L_{CM} = 4 \frac{h}{w} \sqrt{1 - 4(1-2h/w)(s/w)^2},$$  \hspace{1cm} (3)

where $w$ is the width of PCB, $h$ is thickness of the dielectric substrate, $s$ is the distance between the center of the PCB and the center of trace ($s = w/2 - w/2 - d_1$), $w_1$ is the width of trace and $d_1$ is distance between the trace and the PCB edge [10]. Using Eqs. (1) and (3), $|S_{21}|_{\text{cal}}$ dB, which is the normalized value to the $|S_{21}|_{\text{cal}}$ centered trace ($s=0$) and without GB" (center) case, is given by

$$|S_{21}|_{\text{cal}} = |S_{21}| - |S_{21}|_{\text{cal}}^{\text{h=ref}}$$

$$= 20 \log_{10} \frac{(h/h_{\text{ref}})(R_{\text{ref}}/R)}{\sqrt{1 - 4(1-2h/w)(s/w)^2}},$$  \hspace{1cm} (4)

where $h_{\text{ref}}$ is reference thickness, i.e., 1.09 mm in this study.
$R$ is terminating resistance, and $r_{ref}$ that of the “center” case with $h_{ref}$.

Using PCBs shown in Fig. 1 and Table 1, the effect of the guard band (GB) is compared with the case without the guard band by measurement and FDTD modeling. In order to study the effect of the guard band position, four configurations with GB, GB1, GB2, and GB3, as shown in Fig. 5, were modeled with the FDTD method, where the width $w_{GB}$ of guard band was 5 mm. As an example, the measured and calculated results for the “$d_1=6.35$ mm” case are shown in Fig. 6. The calculated and measured results are in good agreement. The $|S_{21}|$ in the cases with the GB1 and GB2 is almost the same as the case with GB which is connected along the all edges, and these curves overlay. On the other hand, the GB3 has no effect in suppressing $|S_{21}|$. Consequently, the results of the cases with GB2 and GB3 are omitted in Fig. 6. These results indicate that the guard band parallel to and near a trace is most effective in suppressing the CM current.

Empirical expressions to quantify the relationship between the position of the trace and CM current for the case with a guard band can be developed from the FDTD modeling. The cross-sectional dimensions of a part of the PCB with the guard band, related to the formulation, is shown in Fig. 7. To investigate the effect of the guard band with the position of the signal trace, the width of the GB1, i.e. $w_{GB}$, was varied with 0, 2.5 and 5.0 mm. In Fig. 7, $w_{GB}=0$ mm means that there is a vertical metallic part of guard band on the PCB edge, but with no horizontal metallic part on the top of the PCB. In addition, the thickness of the dielectric substrate $h$ was varied with 1.05, 1.64 and 2.18 mm. The signal trace was terminated in a matched load $Z_0$.

![Fig. 5 Position of the guard band on the PCB.](image)

The guard band effect $\text{GBE}[\text{dB}]$, which is the difference between the $|S_{21}|$ with GB1 (|$S_{21}|_{GB}$) and $|S_{21}|$ without the guard band (|$S_{21}|_{GB}$), is defined herein as

$$\text{GBE} = |S_{21}|_{GB} - |S_{21}|_{GB}. \quad (5)$$

As an example, $\text{GBE}$ in the case of “$d_1=6.35$ mm, $w_{GB}=5.0$ mm”, i.e., “$d_{250GB}$”, is shown in Fig. 8. Since the $\text{GBE}$ is approximately constant over the considered frequency range, the average value in the considered frequency range is used as $\text{GBE}$ value. Using the distance $d_2$ between the trace and GB1, and $h$, the relationship between $\text{GBE}$ and $d_2/h$ is shown in Fig. 9. The $\text{GBE}$ can be expressed as an empirical equation with parameters determined with a correlation coefficient of 0.99 by the least squares method,

$$\text{GBE} \approx 3.46 \left( \frac{d_2}{h} \right)^{-0.92}, \quad (6)$$

where $d_2$ is the distance between the trace and the edge of GB1 ($d_2 = d_1 - w_{GB}$), and $w_{GB}$ is the width of the guard band. The solid line in Fig. 9 is least squares curve given by Eq. (6). As $d_2$ decreases and/or $h$ increases, the $\text{GBE}$ increases significantly.

Now, the guard band effect $\text{GBE}$ is considered in $|S_{21}|_{\text{GB norm}}$. Using Eq.(4)~(6), the $|S_{21}|_{\text{GB norm}}$ is given as an empirical equation

$$|S_{21}|_{\text{GB norm}} = |S_{21}|_{\text{norm}} - \text{GBE} = 20 \log_{10} \left( \frac{(h/h_{ref})/(\text{ref}(R))}{\sqrt{1 + (1 - 2h/w)(s/w)^2}} \right) - 3.46 \left( \frac{d_2}{h} \right)^{-0.92} \quad (7)$$

The relationship between normalized $|S_{21}|$ and $d_1$ is shown in Fig. 10. In the case of “$h=1.05$ mm”, the normalized $|S_{21}|$ is not calculated for $6.35 \leq d_1 \leq 7.62$ mm, because the terminating resistor $R$ in the case with $d_1 \geq 7.62$ mm is different from that with $d_1 \leq 6.35$ mm, as shown in Table 1. As $d_1$ decreases and/or $h$ increases, the normalized $|S_{21}|$ in the case

![Fig. 6 An example of $|S_{21}|$ in the case with and without the guard band with 5 mm width ($d_1=6.35$ mm).](image)

![Fig. 7 Cross-section of PCB showing the relevant dimensions.](image)

![Fig. 8 GBE vs. frequency (ex. $d_1=6.35$ mm, $w_{GB}=5$ mm).](image)
without the guard band increases. On the other hand, the normalized $|S_{21}|$ in the case with a guard band has a peak and then decreases as $d_1$ is smaller. This indicates that the guard band allows for a trace to be routed near a PCB edge. The calculated results (lines in Fig. 10) using Eq. (4) and (7) agree well with the FDTD calculated results (symbols). This indicates the effect of the guard band to suppress the CM current can be estimated using Eq. (7). Therefore, a guard band will be effective for high-density PCB packaging with high-speed traces.

IV. Conclusions

Influence of guard band on CM current related to a trace was studied experimental and FDTD modeling. The guard band is effective in suppressing the CM current, and allows for a trace to be routed near a PCB edge. An empirical formula should be useful for developing EMI design guidelines.

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